

*Technical Summary**MPC860TTS/D
Rev. 0.1, 12/2001**MPC860T PowerQUICC™
Technical Summary*

The MPC860T Fast Ethernet communication controller is an enhanced version of the MPC860 PowerQUICC family. In addition to all existing MPC860MH capabilities, the MPC860T includes an additional 10/100-Mbps Ethernet channel.

Like the other MPC860 devices, the MPC860T can be used in a variety of controller applications, excelling particularly in communications and networking products, such as routers that provide WAN to LAN functionality. The MPC860T, with the addition of the 10/100-Mbps Ethernet channel, adds Fast Ethernet to the already broad list of communications support.

The MPC860T integrates three separate processing blocks. The first two, common with all MPC860 devices, are (1) a high-performance embedded MPC860T Core, which is used as a general-purpose processor for application programming and (2) a RISC processor embedded in the communications processor module (CPM), which is designed to provide the communications protocol processing provided by the MPC860MH. The third block is a 10/100-Mbps Fast Ethernet controller with integrated FIFOs and bursting DMA. The MPC860T's Fast Ethernet controller is implemented independently, providing high-performance Fast Ethernet connectivity without affecting the performance of the CPM. All of the performance and functionality of the MPC860MH is fully supported, including Ethernet.

Additionally, as the CPM of the MPC860T is based on the CPM of the MPC860MH, support for the QMC protocol is also provided. This enables the MPC860T to provide protocol processing (through HDLC or transparent mode) for 64 time-division-multiplexed channels when the MPC860T is operated at 50 MHz. This support for multichannel protocol processing and 10/100-Mbps Ethernet in one chip makes the MPC860T ideal for products such as high-performance, low-cost remote access routers.

1.1 MPC860T PowerQUICC Key Features

The key features of the MPC860T PowerQUICC are summarized as follows:

- 10/100-Mbps Ethernet support
 - Full compliance with the IEEE 802.3u standard for 10/100-Mbps
 - Support for three different physical interfaces

MPC860T PowerQUICC Key Features

- 100-Mbps 802.3 media-independent interface (MII)
- 10-Mbps 802.3 media-independent interface
- 10-Mbps 7-wire interface
- Support for half-duplex 100-Mbps operation (at 33-MHz system clock rate and above)
- Support for full-duplex 100-Mbps operation (at 50-MHz system clock rate and above)
- Large on-chip transmit and receive FIFOs to support a variety of bus latencies
- Retransmission from transmit FIFO following a collision
- Automatic internal flushing of the receive FIFO for runts and collisions
- Off-chip buffer descriptor rings of user-definable size that allow nearly unlimited flexibility in management of transmit and receive buffer memory
- 10/100-Mbps media access control (MAC) features
 - Address recognition
 - Broadcast
 - Single station address
 - Promiscuous mode
 - Multicast hashing
 - Full support of the media-independent interface
 - Interrupt modes
 - Per-frame
 - Per-buffer (selectable buffer interrupt functionality using the I bit is not supported)
 - Automatic interrupt vector generation for receive and transmit events

Categories: transmit interrupt, receive interrupt, non-time critical interrupt
 - Ethernet channel bursts data to/from external memory
- Embedded MPC860T Core with 87 MIPS at 66 MHz (using Dhrystone 2.1)
 - Single-issue, 32-bit version of the embedded MPC860T Core (fully compatible with the PowerPC user instruction set architecture; refer to the Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture, REV 2(MPCFPE32B/AD) for more information) with 32- x 32-bit fixed-point registers
 - Embedded core performs branch folding and branch prediction with conditional prefetch, but without conditional execution
 - 4-Kbyte data cache and 4-Kbyte instruction cache, each with an MMU
 - Instruction and data caches are two-way, set associative, physical address, 4-word line burst, least recently used (LRU) replacement, lockable on cache line granularity
 - MMUs with 32-entry, fully-associative instruction and data TLBs
 - MMUs support multiple page sizes of 4 Kbytes, 16 Kbytes, 256 Kbytes, 512 Kbytes, and 8 Kbytes; 16 virtual address spaces and 8 protection groups
 - Advanced on-chip-emulation debug mode
 - Up to 32-bit data bus (dynamic bus sizing of 8, 16, and 32 bits provided through memory controller)
 - 32 address lines

- Complete static design (0- to 66-MHz operation)
- System integration unit (SIU)
 - Bus monitor
 - Spurious interrupt monitor
 - Software watchdog
 - Periodic interrupt timer
 - Low-power stop mode
 - Clock synthesizer
 - Decrementer defined by the PowerPC Architecture
 - Time base and RTC defined by the PowerPC Architecture
 - Reset controller
 - IEEE 1149.1 test access port (JTAG)
 - Memory controller (eight bank)
 - Contains complete dynamic random-access memory (DRAM) controller
 - Each bank may be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
 - Up to 15 wait states programmable per memory bank
 - Glueless interface to DRAM single in-line memory modules (SIMMs), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), Flash EPROM, etc.
 - DRAM controller programmable to support most size and speed memory interfaces
 - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, one $\overline{\text{OE}}$ line
 - Boot chip select available at reset (options for 8-, 16-, or 32-bit memory)
 - Variable block sizes, 32 Kbytes to 256 Mbytes
 - Selectable write protection
 - On-chip bus arbitration logic
 - General-purpose timers
 - Four 16-bit timers or two 32-bit timers
 - Gate mode can enable/disable counting
 - Interrupt may be masked on reference match and event capture
 - Interrupts
 - Seven external interrupt request (IRQ) lines
 - 12 port pins with interrupt capability
 - 16 internal interrupt sources
 - Programmable priority between SCCs (serial communication controllers)
 - Programmable highest priority request
 - PCMCIA interface
 - Master (socket) interface, release 2.1 compliant
 - Supports two independent PCMCIA sockets

MPC860T PowerQUICC Key Features

- 8 memory or I/O windows supported
- Communications Processor Module (CPM)
 - Supports all functionality and performance of MPC860MH
 - RISC processor
 - Communication-specific commands (for example, graceful stop transmit, close receive buffer descriptor, RxBD)
 - Up to 384 buffer descriptors
 - Supports continuous mode transmission and reception on all serial channels
 - Up to 5 Kbytes of dual-port RAM
 - 16 serial DMA (SDMA) channels
 - Three parallel I/O registers with open-drain capability
 - Four baud rate generators
 - Independent (may be connected to any SCC or SMC)
 - Baud rate changes allowed during operation
 - Autobaud support option
 - Four SCCs (serial communication controllers)
 - QMC microcode for protocol processing of 64 time-division-multiplexed channels
 - Ethernet/IEEE 802.3u on SCC1–4, supporting full 10-Mbps operation
 - HDLC/SDLC™ (all channels supported at 2 Mbps)
 - HDLC bus (implements an HDLC-based local area network (LAN))
 - Asynchronous HDLC supports PPP (point-to-point protocol)
 - AppleTalk™
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Serial infrared (IrDA)
 - Binary synchronous communication (BISYNC)
 - Totally transparent (bit streams)
 - Totally transparent (frame based with optional cyclic redundancy check (CRC))
 - QMC microcode features
 - Up to 64 independent communication channels on a single SCC
 - Arbitrary mapping of 0–31 channels to any of 0–31 TDM time slots
 - Supports either transparent or HDLC protocols for each channel
 - Independent transmit and receive buffer descriptors and event/interrupt reporting for each channel
 - Running QMC microcode independently on multiple SCCs allows even more channels (for example, 64 at 50-MHz system frequency)
 - Two SMCs (serial management channels)
 - UART
 - Transparent

- General circuit interface (GCI) controller
- May be connected to the time-division-multiplexed (TDM) channels
- One SPI (serial peripheral interface)
 - Supports master and slave modes
 - Supports multimaster operation on the same bus
- One I²C (inter-integrated circuit) port
 - Supports master and slave modes
 - Multimaster environment support
- Time slot assigner
 - Allows SCCs and SMCs to run in multiplexed and/or nonmultiplexed operation
 - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
 - 1- or 8-bit resolution
 - Allows independent transmit and receive routing, frame syncs, clocking
 - Allows dynamic changes
 - May be internally connected to six serial channels (four SCCs and two SMCs)
- Parallel interface port
 - Centronics™ interface support
 - Supports fast connection between compatible ports on MPC860 or MC68360
- Low power support
 - Full-on—all units fully powered
 - Doze—core functional units disabled except time base, decrementer, PLL, memory controller, RTC, and CPM in low-power standby
 - Sleep—all units disabled except RTC and PIT, PLL active for fast wake-up
 - Deep sleep—all units disabled including PLL except RTC and PIT
 - Low-power STOP mode provides lowest power dissipation
- Debug interface
 - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data
 - Supports conditions: = <>
 - Each watchpoint can generate a breakpoint internally
- 3.3-V operation with 5-V TTL compatibility
- 357-pin ball grid array (BGA) package

1.2 MPC860T Architecture Overview

The MPC860T PowerQUICC integrates the embedded MPC860T Core with high-performance, low-power peripherals to extend the Motorola data communications family of embedded processors into high-end communications and networking products.

The MPC860T PowerQUICC is comprised of four modules connected to the 32-bit internal bus: the embedded MPC860T Core, the system integration unit (SIU), the communication processor module (CPM), and the Fast Ethernet controller (FEC). The MPC860T PowerQUICC block diagram is shown in Figure 1.

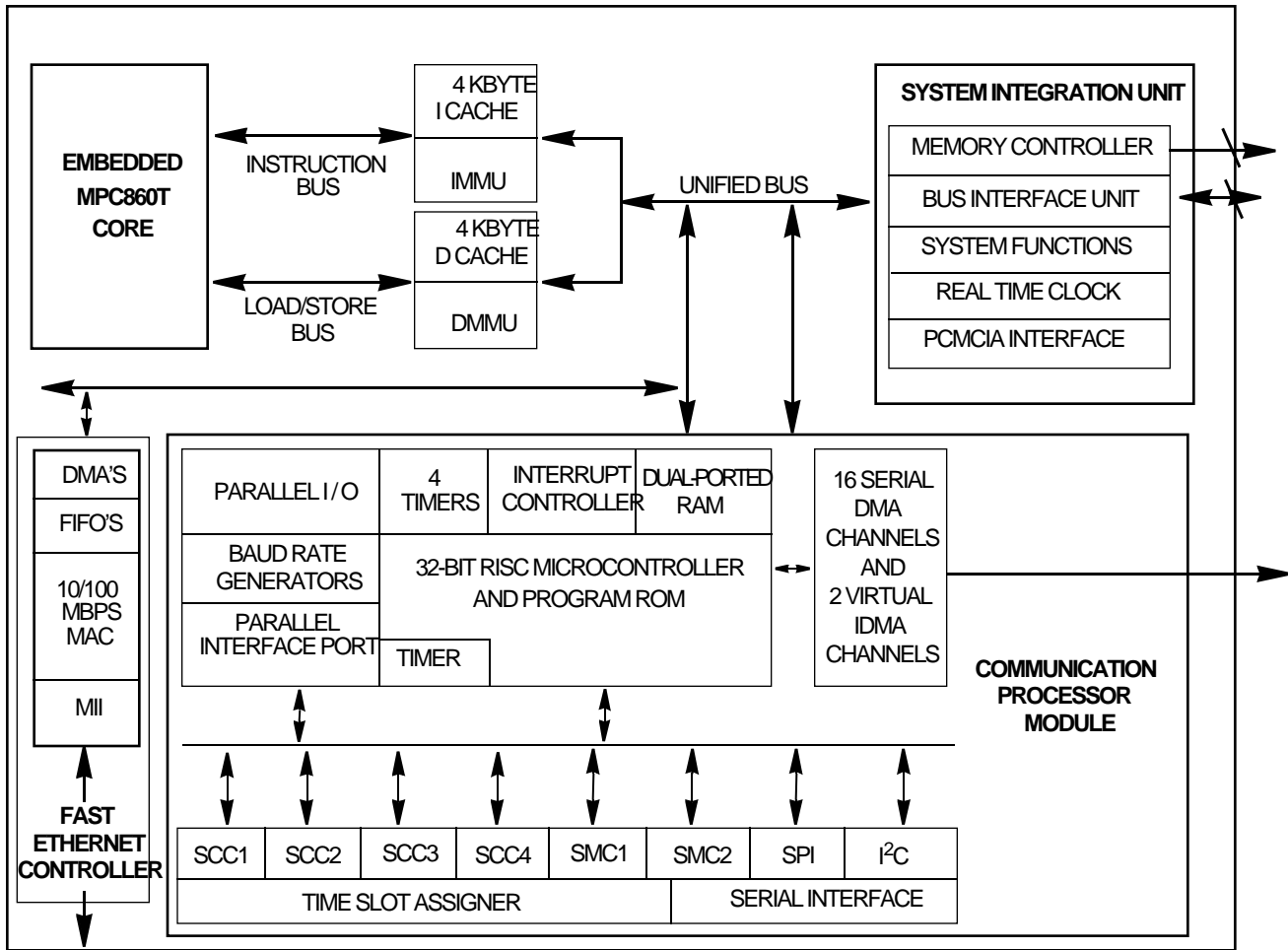


Figure 1. . MPC860T PowerQUICC Block Diagram

1.2.1 Embedded MPC860T Core

The embedded MPC860T Core is compliant with the PowerPC user instruction set architecture; refer to the *The Programming Environments Manual for 32-Bit Implementations of the PowerPC Architecture*, Rev. 2 for more information. The embedded MPC860T Core is a fully-static design that consists of two functional units—the integer unit and the load/store unit. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits. The core uses a two-instruction load/store queue, a four-instruction prefetch queue, and a six-instruction history buffer. The core performs branch folding and branch prediction with conditional prefetch, but without conditional execution. The embedded MPC860T Core can operate on 32-bit external operands with one bus cycle.

The MPC860 integer unit supports 32- x 32-bit fixed-point general-purpose registers. It can execute one integer instruction each clock cycle. Each element in the integer unit is clocked only when valid data is

present in the data queue ready for operation. This assures that the power consumption of the device is held to the absolute minimum required to perform an operation.

The embedded MPC860T Core is integrated with MMUs as well as 4-Kbyte instruction and data caches. Each MMU provides a 32-entry, fully-associative instruction and data TLB, with multiple page sizes of: 4 Kbytes, 16 Kbytes, 512 Kbytes, 256 Kbytes, and 8 Mbytes. It supports 16 virtual address spaces with 8 protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The instruction cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with no added latency for miss. It has four words per line, and supports burst linefill using least recently used (LRU) replacement. The cache may be locked on a per-line basis for application-critical routines.

The data cache is 4 Kbytes, two-way, set associative with physical addressing. It allows single-cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst linefill using LRU replacement. The cache may be locked on a per-line basis for application-critical routines. The data cache can be programmed to support copy-back or write-through via the MMU. The cache-inhibit mode can be programmed per MMU page.

The embedded MPC860T core with its instruction and data caches delivers approximately 87 MIPS at 66 MHz, using Dhrystone 2.1, based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

The embedded MPC860T Core provides a much improved debug interface that operates without causing any degradation in the speed of user operations. This interface supports six watchpoint signals that are used to detect software events. Internally the MPC860T has eight comparators, four of which operate on the effective address on the address bus. The remaining four comparators are split, with two comparators operating on the effective address on the data bus, and two comparators operating on the data on the data bus. The embedded MPC860T Core can compare using =, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

1.2.2 Fast Ethernet Controller (FEC)

The Fast Ethernet controller on the MPC860T PowerQUICC is compliant with the IEEE 802.3u specification for 10-Mbps and 100-Mbps connectivity. Full-duplex 100-Mbps operation is supported at system clock rates of 50 MHz and higher. A 33-MHz system clock supports 10-Mbps operation or half-duplex 100-Mbps operation.

The Fast Ethernet controller provides greatly reduced bus utilization through the use of bursting DMA. Optimization of bus utilization allows the MPC860T to be used in systems with low-cost memories such as fast page mode DRAM.

Transmit and receive FIFOs further reduce bus utilization by localizing all collisions to the Fast Ethernet controller. On the transmit side, a full collision window of transmit frame data is maintained in the FIFO, eliminating the need for repeated DMA over the system bus in the event of a collision. On the receive side, a full collision window of data is received before any receive data is transferred into system memory, allowing the FIFO to be flushed in the event of a runt or collided frame, with no DMA activity. However, external memory for data buffers and buffer descriptors is required; on-chip FIFOs are only designed to compensate for collisions and for system bus latency.

Independent transmit and receive buffer descriptor rings located in external memory allow nearly unlimited flexibility in memory management of transmit and receive data frames. Locating buffer descriptors in

external memory has two advantages—first, external memory (i.e., DRAM) is low cost; secondly, descriptor rings in external memory have no inherent size limitations, allowing the memory management to be optimized according to specific system needs.

1.2.3 System Interface Unit (SIU)

The SIU on the MPC860T PowerQUICC integrates general-purpose features useful in almost any 32-bit processor system, enhancing the performance provided by the system integration module (SIM) on the MC68360 QUICC device.

Although the embedded MPC860T core is always a 32-bit device internally, it may be configured to operate with an 8-, 16- or 32-bit data bus. Regardless of the choice of the system bus size, dynamic bus sizing is supported. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, reset control, decremter, time base and real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SDRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock access. The memory controller supports bursting and variable memory block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–15 wait states for each bank of memory and can use address type matching to qualify each memory bank access. It also provides four byte-enable signals for varying width devices, one output enable signal, and one boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks are defined in depths of 256 and 512 Kbytes, and 1, 2, 4, 8, 16, 32, and 64 Mbytes for all port sizes. In addition, memory depth is defined as 64 Kbytes and 128 Kbytes for 8-bit memory or 128 Mbytes and 256 Mbytes for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC860T supports a glueless interface to one bank of DRAM; external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking up to seven refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

1.2.3.1 PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is compliant with release 2.1. The interface supports up to two independent PCMCIA sockets requiring only external transceivers/buffers. The interface provides eight memory or I/O windows where each window is allocated to a particular socket. If only one PCMCIA port is being used, the unused PCMCIA port may be used as general-purpose input with interrupt capability.

1.2.3.2 Power Management

The MPC860 PowerQUICC family supports a wide range of power management features including full-on, doze, sleep, deep sleep, and low-power stop. In full-on mode the MPC860 processor is fully powered with all internal units operating at the full speed of the processor. A programmable clock divider allows the OS to reduce the operational frequency of the processor. Doze mode disables core functional units other than the time base, decremter, PLL, memory controller, RTC, and places the CPM in low-power standby mode. Sleep mode disables everything except the RTC and PIT, leaving the PLL active for quick wake-up. The deep sleep mode disables the PLL for lower power but slower wake-up. Low-power stop disables all logic

in the processor except the minimum logic required to restart the device, providing the lowest power consumption but requiring the longest wake-up time.

1.2.3.3 Communications Processor Module (CPM)

The MPC860 PowerQUICC family, like the earlier generation MC68360 QUICC, implements a dual-processor architecture. This dual-processor architecture provides both a high-performance, general-purpose processor for application programming use as well as a special-purpose communications processor module (CPM) uniquely designed for communications needs.

The CPM contains features that allow the PowerQUICC to excel in communications and networking products. These features may be divided into three subgroups:

- Communications processor (CP)
- Sixteen independent serial DMA (SDMA) controllers
- Four general-purpose timers

The CP provides the communication features of the MPC860 PowerQUICC family. Included are a RISC processor, four serial communication controllers (SCC), two serial management controllers (SMC), one serial peripheral interface (SPI), one I²C Interface, 5 Kbytes of dual-port RAM, an interrupt controller, a time slot assigner, three parallel ports, a parallel interface port, four independent baud rate generators, and sixteen serial DMA channels to support the SCCs, SMCs, SPI, and I²C.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on the MC68360 and still support the internal cascading of two timers to form a 32-bit timer.

The PowerQUICC family maintains the best features of the MC68360 QUICC, while making changes required to provide for the increased flexibility, integration, and performance requested by customers demanding the performance of the PowerPC architecture. Because the CPM architectural approach remains intact between the PowerQUICC family and the MC68360 QUICC, a user of the MC68360 QUICC can easily become familiar with the PowerQUICC.

Additionally, like the MC68MH360, QUICC32, and the MPC860MH, the MPC860T supports the QMC microcode, enabling it to provide protocol processing for multiple time-division-multiplexed channels over a single SCC.

1.2.3.4 The QMC Microcode

The standard MPC860 can handle one logical channel performing the protocol framework for each of its serial channels. This logical channel is used in time-division-multiplexed interfaces. In contrast, the QMC microcode emulates up to 64 serial controllers that can operate in either HDLC mode or transparent mode within one single SCC.

Refer to the *QMC Supplement to MC68360 and MPC860 User's Manuals* for more details about the features and operation of the QMC microcode.

1.2.4 Software Compatibility Issues

The following list summarizes the major software differences between the MC68360 QUICC and the

MPC860 PowerQUICC family:

- Since the MPC860 PowerQUICC family uses an embedded MPC860T core, code written for the MC68360 must be recompiled for the PowerPC instruction set. Code that accesses the MC68360 peripherals requires only minor modifications for use with the MPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different, and, therefore, code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers that also support the PowerPC architecture.
- When porting code from the MC68360 CPM to the MPC860 CPM, the software writer will find new options for hardware breakpoint on CPU commands, addresses, and serial requests that are useful for software debugging. Support for single-step operation with all the registers of the CPM visible makes software development for the CPM on the MPC860T processor even simpler.

1.3 PowerQUICC Glueless System Design

A fundamental design goal of the MPC860 PowerQUICC family is ease of interface to other system components. Figure 2 shows a system configuration that offers one EPROM, one Flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

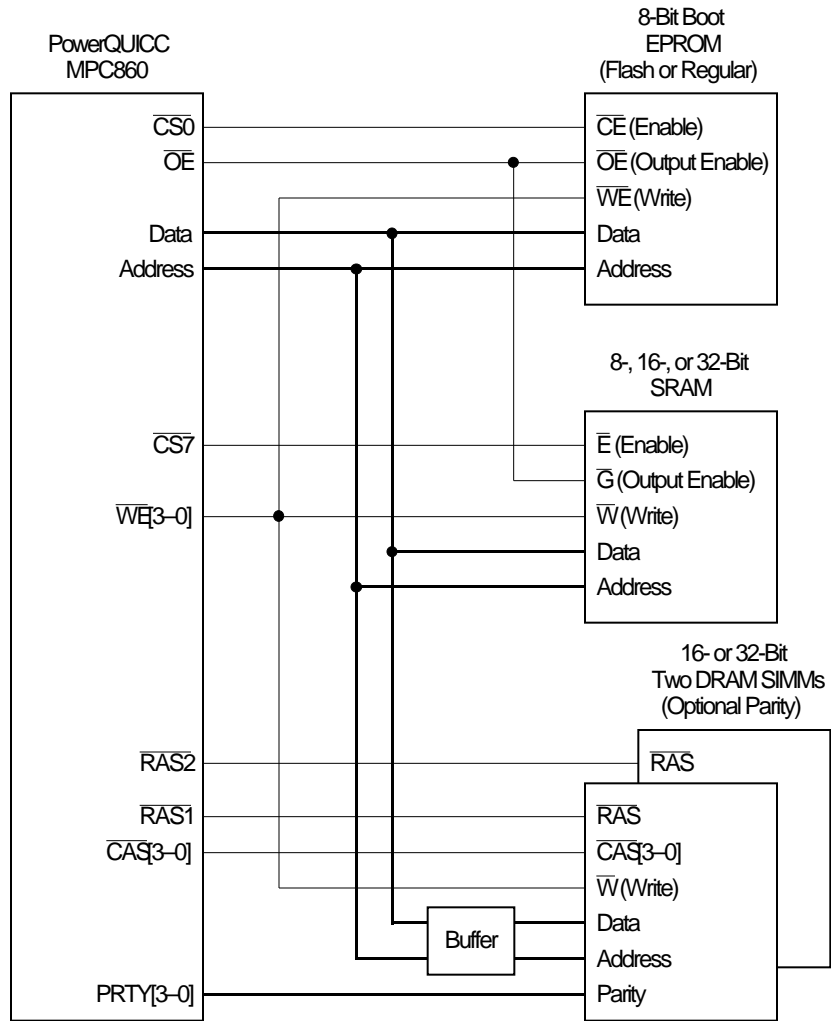


Figure 1. MPC860T System Configuration

Figure 3 shows the glueless connection of the MPC860T serial channels to physical layer framers and transceivers.

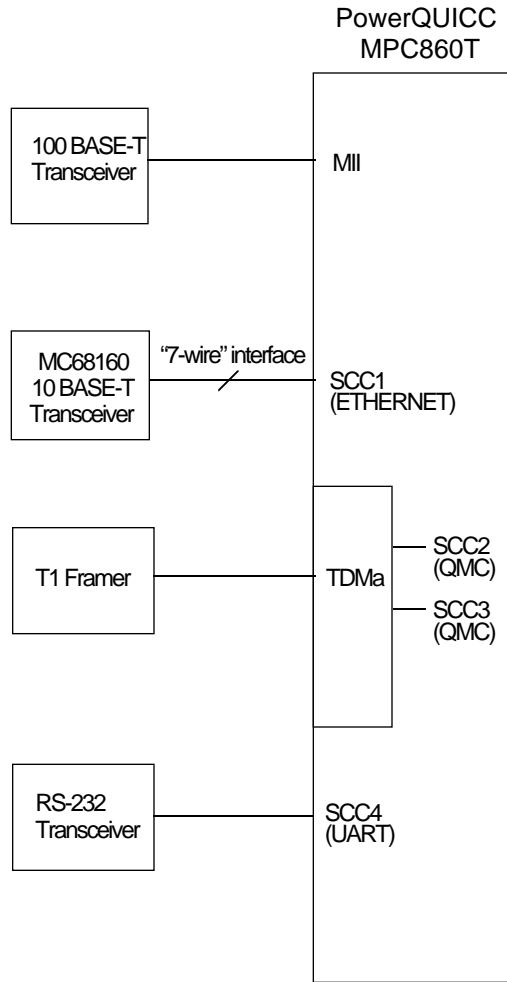


Figure 2. MPC860T Serial Configuration

1.4 Ordering Information

Table 1. identifies the packages and operating frequencies available for the MPC860T.

Table 1. . MPC860T Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number
Ball grid array (ZP suffix)	33	0°C to 70°C	MPC860TZP33
	50	0°C to 70°C	MPC860TZP50
	66	0°C to 70°C	MPC860TZP66
Ball grid array (CZP suffix)	TBD	-40°C to 95°C Junction temp.	TBD

For additional information, see the documents listed in Table 2..

Table 2. . Reference Documents

Document Title	Order Number	Contents
<i>MPC860T Fast Ethernet Controller Supplement to the MPC860 PowerQUICC User's Manual</i>	A preliminary version is available on the Motorola NetComm website	Contains detailed information for design
<i>QMC Supplement to MC68360 and MPC860 User's Manuals</i>	QMCSUPPLEMENT/AD	Supports MC68MH360, MPC860MH and MPC860DH devices
<i>MPC860 PowerQUICC User's Manual</i>	MPC860UM/AD	Detailed information for design

Table 3. Document Revision History

Revision	Date	Changes
0.1	12/2001	Revised for new template, added this revision table.



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