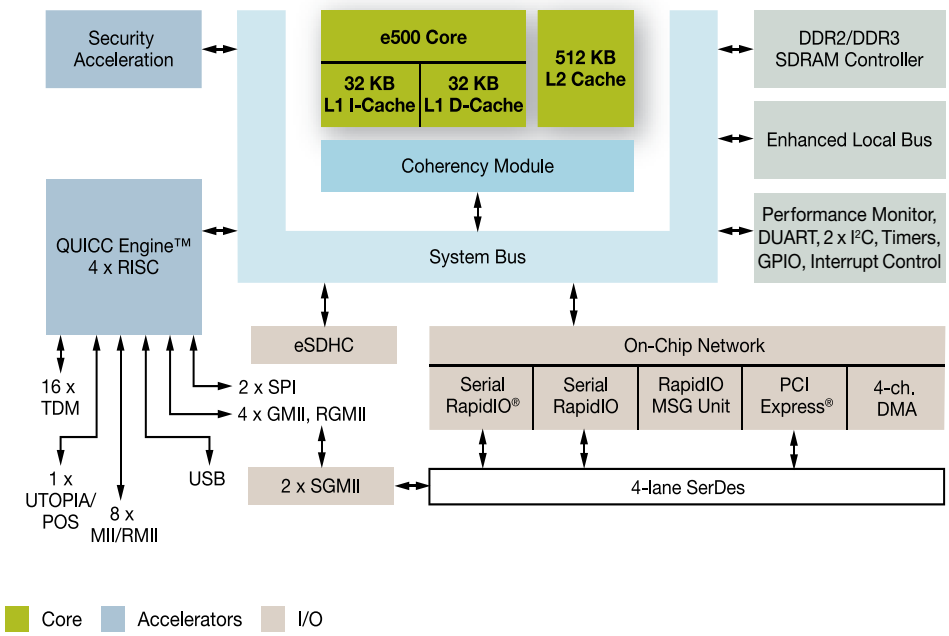
MPC8569E PowerQUICC® III Processor

Overview

The MPC8569E PowerQUICC® III family is designed to address the increasing performance requirements for broadband access equipment including 3G/WiMAX/LTE base stations, radio network controllers, gateways and ATM/TDM/IP equipment. The MPC8569E helps facilitate both IP and multi-protocol solutions by combining a high-performance e500 processor core, built on Power Architecture® technology and scaling up to 1.33 GHz, with a flexible communications engine and high-speed system interfaces.

The MPC8569E is designed to enable customers to handle many functions in a single chip solution that otherwise would require multiple devices. Ultimately, this high level of integration provides savings in cost, power and board space. The MPC8569E provides multi-protocol support for both protocol termination and interworking for a wide range of communication protocols, including ATM, POS, Ethernet, PPP, HDLC and TDM—allowing the flexibility necessary for broadband access devices. Four Gigabit Ethernet ports, PCI Express® and Serial RapidIO® interconnect technology enables high-speed links to industry-wide switches, field-programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) and digital signal processors (DSPs). An optional integrated security engine supports common encryption algorithms, including the SNOW 3G algorithm needed for LTE wireless security.

MPC8569E Block Diagram



Key Features

- High level of integration and performance, simplifying board design
- Consistent programming model across the PowerQUICC III family of processors
- Flexible system-on-chip (SoC) platform helps improve time to market
- 45 nm silicon-on-insulator (SOI) technology
- Enhanced high-performance e500 core with 32 KB D/I cache
- 512 KB L2 cache
- High internal processing bandwidth
- Integrated DDR2/DDR3 memory controllers
- Four integrated Gigabit Ethernet controllers
- Advanced QUICC Engine™ technology supports a wide range of protocols and associated interworking
- Flexible high-speed interconnect interfaces
  - Serial RapidIO interconnect technology
  - PCI Express support
- Enhanced local bus interface supporting NAND flash control machine
- Optional integrated security engine (indicated by an E in the device number)

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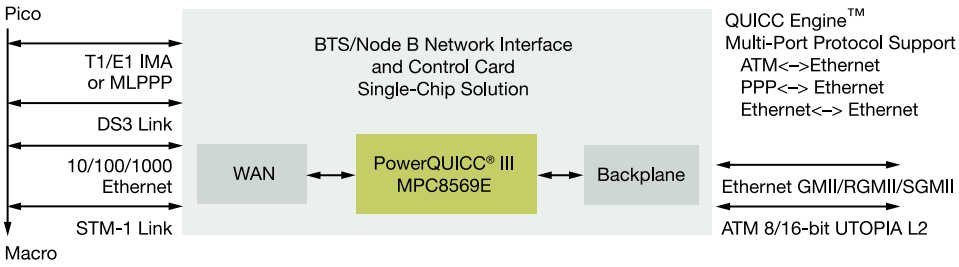
Technical Specifications

- Embedded e500 core, scaling up to 1.33 GHz
  - 2799 MIPS at 1.33 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
  - Double-precision embedded floating point
  - Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction
  - L2 cache—512 KB (8-way set associative)
- Integrated DDR memory controller with full ECC support

Wireless Node B Network Interface Cards (NIC) Block Diagram



MPC8569E Processor Highlights	
Core	e500, built on Power Architecture® technology
CPU Speed	800 MHz, 1.0, 1.2, 1.33 GHz
L1 I/D Cache	32 KB
L2 Cache	512 KB
Memory Controller	1 x 64-bit DDR2/DDR3 or 2 x 32-bit DDR2/DDR3 supporting data rates 533 Mbps–800 Mbps
Local Bus	16-bit
System Interfaces	Serial RapidIO®, PCI Express® (x4)
QUICC Engine™	
• 4 RISC	Up to 667 MHz
• Memory	256 KB Instruction RAM, 128 KB Multi-user RAM
• Ethernet	4 x 10/100/1000, 8 x 10/100
• ATM (AAL0,1,2,5)	1 x UTOPIA-L2, 124 M-PHY
• Packet over SONET (POS)	1 x POSPHY-L2, 31 M-PHY
• 8 TDMs (256 channels of HDLC)	16 x T1/E1, 8 x T3/E3
• Protocol Termination and Interworking	Yes
• USB	Full/low speed
• IEEE® 1588 v2	
• 2 x SPI	
• Security Engine	SEC 3.01
Additional Interfaces	DUART, 2 x I²C, GPIO
Interrupt Controller	Yes
Package	783 FC-PBGA, 29 mm x 29 mm

- Optional integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9, SNOW and ARC-4 (indicated with an E in the device number)
- QUICC Engine technology
  - Protocol Support:
    - ATM SAR up to 622 Mbps (OC-12) full duplex
    - PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPPmux termination and interworking
    - IP termination support for IPv4
    - ATM (AAL2/AAL5) to Ethernet (IP), Ethernet to Ethernet (IP) interworking
    - Extensive support for Ethernet RMON/MIB statistics
    - 256 channels of HDLC/Transparent or 256 channels of SS7
  - Serial Interfaces:
    - One UL2/POS-PHY interfaces
    - Four 10/100/1000 Mbps Ethernet interfaces using GMII, RGMII or SGMII
    - Up to eight 10/100 Mbps Ethernet interfaces using MII, RMII or SMII
    - Up to sixteen T1/E1/J1 interfaces or eight T3/E3 interfaces
    - Dual SPI interfaces
    - Full/low speed USB
- Serial RapidIO and PCI Express high-speed interconnect interfaces
- On-chip network switch fabric
- 166 MHz, 32-bit, 3.3V I/O, enhanced local bus with memory controller
- Enhanced Secured Digital Host Controller (eSDHC) used for SD/MMC card interface
- Integrated four-channel DMA controller
- Dual I²C and Dual Universal Asynchronous Receiver/Transmitter (DUART) support
- Programmable interrupt controller (PIC)
- General Purpose I/O (GPIO)
- IEEE 1149.1 JTAG test access port
- 1.0V core voltage with 3.3V, 2.5V, 1.8V, 1.5V and 1.0V I/O
- 783-pin FC-PBGA package, 29 mm x 29 mm

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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