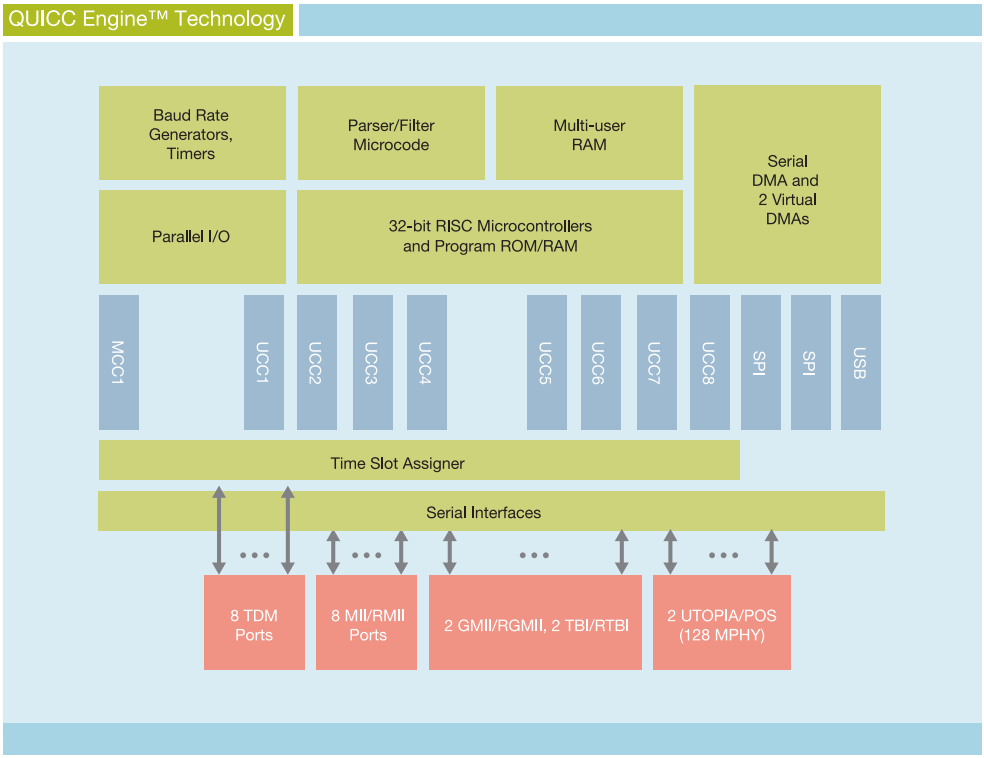
Introducing Freescale's QUICC Engine™ Technology

Overview

The QUICC Engine™ technology is an evolutionary step forward for Freescale Semiconductor's Communications Processor Module (CPM), a hallmark of the PowerQUICC™ family of communications processors built on Power Architecture™ technology. The QUICC Engine features a scalable number of embedded RISC engines that provide a range of performance points that cover customer premises equipment to the edge of the network, and in some instances, to the core of the network.

The initial QUICC Engine includes two optimized RISC processors, each initially scaling up to 500 MHz and supporting a wide range of protocols, while providing high data aggregate throughput of 1.2 Gbps interworking. In addition, Freescale plans to expand its shrink-wrapped protocol software support with further enhancements that include interworking, switching, parsing and IP forwarding, as well as improvements in Freescale's existing termination suite of protocol support. The QUICC Engine supports OC-12 to Gigabit Ethernet interworking throughput of 1.2 Gbps (2.34 Mpps), or in excess of 2 Gbps Layer 2 termination (3.9 Mpps) based on 64 byte packets.

Eight unified communications controllers (UCCs) provide support for Fast Ethernet, Gigabit Ethernet, high-level data link control (HDLC) and asynchronous transfer mode (ATM)/Packet over Sonet (POS) at up to OC-12 speeds. Eight time-division multiplexers (TDMs) enable connection to eight T1/E1 or eight clear channel T3/E3 lines. In addition to the UCCs, the QUICC Engine can support multiple multi-channel communications controllers (MCCs), although only one is offered today. The QUICC Engine allows for exceptional flexibility and includes an integrated Ethernet L2 switch, as well as a host of advanced protocol support.



To simplify the transition from current PowerQUICC designs, the advanced QUICC Engine technology maintains a high degree of software compatibility with previous-generation PowerQUICC designs. This backward compatibility helps to ease migration issues, reduce development costs and speed time to market.

The QUICC Engine technology also supports direct memory access via low latency serial direct memory access controllers, which allows it to connect to SDRAM and DDR memory support. This provides quick access to low-latency memory for parameters, buffer descriptors and data.

QUICC Engine technology is designed to handle a wide range of communications interfaces supporting a combination of ATM, POS, Ethernet, HDLC and transparent communications protocols, such as MII, RMII, GMII, RGMII, TBI, RTBI, NMSI, UTOPIA, UTOPIA MPHY, POS-PHY, TDM, UART, BISYNC, serial peripheral interface (SPI) and Universal Serial Bus (USB) interface (USB 2.0 full-/low-speed compatible).

QUICC Engine technology incorporates many advanced features that make it suitable for today's and tomorrow's broadband wired and wireless access equipment, as well as small and medium enterprise networking equipment. Target applications include multi-tenant units (MTUs), digital subscriber line access multiplexers (DSLAMs), wireless base stations, multi and fixed subscriber access nodes, multi-service provisioning platforms and routers.

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Typical Applications

- DSL infrastructure
  - DSLAMs
  - MTUs
- Wireless infrastructure
  - Base transceiver station (BTS)
  - Base station controller (BSC)
  - Radio network controller (RNC)
  - NodeB
- Small and medium enterprise (SME) routers
  - Intrusion detection/protection system (IDS/IPS)
  - Secure VPN
  - Firewall
- Add/drop multiplexers and digital cross connects
- Integrated voice routers and digital IP-based private automatic branch exchange (PABX)
- Multi-service access nodes (MSAN)
- Passive optical networks (PON)
- IEEE® 802.16 WiMAX Super Access points and base stations
- Industrial and general purpose networking

Technical Specifications

- QUICC Engine operating at 200 MHz to 500 MHz
- Two 32-bit RISC controllers for flexible support of the communications peripherals
  - Enhancements in the RISC microarchitecture
  - Improved instruction set
  - Multiple hardware accelerators
  - Pipelined packet processing
  - High level of tolerance to maximum latency accesses to memory
  - Deep programmable first in, first outs (FIFOs)
  - QUICC Engine frequency is independent of the system bus frequency
  - Arbitration mechanism is fully optimized for communications protocols and interfaces
- Serial DMA channel for receive and transmit on all serial channels
- QUICC Engine peripheral request interface for Integrated Security, PCI, IEEE Std 1588™
- Eight unified communications controllers supporting the following protocols and interfaces (Also see Table 1 for protocol comparison.):
  - 10/100/1000 Mbps Ethernet
  - Support for IEEE Std 1588 protocol
  - ATM SAR supporting up to 622 Mbps per second AAL5, AAL2, AAL1, AAL0, TM 4.0 CBR, VBR, UBR traffic types, up to 64 KB external connections
  - Inverse multiplexing for ATM (IMA)
  - POS up to 622 Mbps
  - Transparent
  - HDLC
  - Multi-link, multi-class PPP
  - HDLC bus
  - UART
  - BISYNC
  - User programmable FIFO size
  - One multi-channel communications controller (MCC), supporting:
    - 256 TDM channels
    - Transparent and HDLC mode per channel
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
  - Two UTOPIA/POS interfaces supporting up to 128 MPHY each
  - Eight TDM interfaces supporting
    - Aggregate bandwidth of 64 kbps per channel and 256 channels total
    - Maximum of 16 Mbps and 256 channels on a single TDM link
    - 2,048 bytes of SI RAM (1,024 entries)
    - Eight programmable strobes
    - Bit or byte resolution
    - Independent transmit and receive routing, frame synchronization
    - T1, CEPT, T1/E1, T3/E3, pulse-code modulation highway, ISDN primary/basic rate, Freescale interchip digital link (IDL) and user-defined TDM serial interfaces
  - Sixteen independent baud rate generators and 30 clock pins for supplying clocks to UCC, MCC serial channels
  - Four independent 16-bit timers that can be interconnected as two 32-bit timers
  - Two serial peripheral interface (SPI) ports can be configured as an Ethernet management port for management data input/output (MDIO), while the other can be configured for low-cost serial peripherals; the SPI also has a CPU mode that can be configured by the CPU and not through the QUICC Engine
  - Two SPIs—SPI2 is dedicated to Ethernet PHY management
  - USB interface (USB 2.0 full-/low-speed compatible)

QUICC Engine™ and CPM Technical Comparison		
Feature/Capability	**CPM**	**QUICC Engine**
Number of RISC Engines	1	2 in 8360E family (scalable SoC methodology: 1, 2 and 4-core designs possible)
Asynchronous Clocking	No	Yes
Clock Frequency	Up to 333 MHz	Scales from 200 MHz to 500 MHz
DDR Memory Support	No	Yes
Layer 2 Support	Yes	Yes
Layer 3 Support	No	Yes
Major Interfaces/Protocols	2 UTOPIA: OC-3 ATM, 31 MPHY each 3 MII/RMII: 10/100 Ethernet 8 TDMs	2 UTOPIA: OC-12 ATM/POS, 128 MPHY each 8 MII/RMII: 10/100 Ethernet, 2 GMII: 10/100/1000 Ethernet 8 TDMs
Interworking	No	Yes, including forwarding, switching and parsing; offloads these tasks from CPU
Communication Peripheral Architecture	2 MCCs: 128 channels of HDLC each 3 FCCs: ATM, Fast Ethernet, Transparent 4 SCCs: 10 Base-T, UART and other slow-speed serial interfaces	1 MCC: 256 channels of HDLC 8 unified communications controllers (UCCs): ATM, Fast Ethernet, Gigabit Ethernet, Transparent and the slower SCC based protocols
Performance	Up to 700 Mbps Layer 2 termination	Up to 1.2 Gbps interworking (2.34 Mpps) Up to 2 Gbps termination (3.9 Mpps)
User Configurability and Programmability	Not supported	Software configuration tools and drivers available **www.freescale.com/quiccengine** for Open QUICC Engine program overview

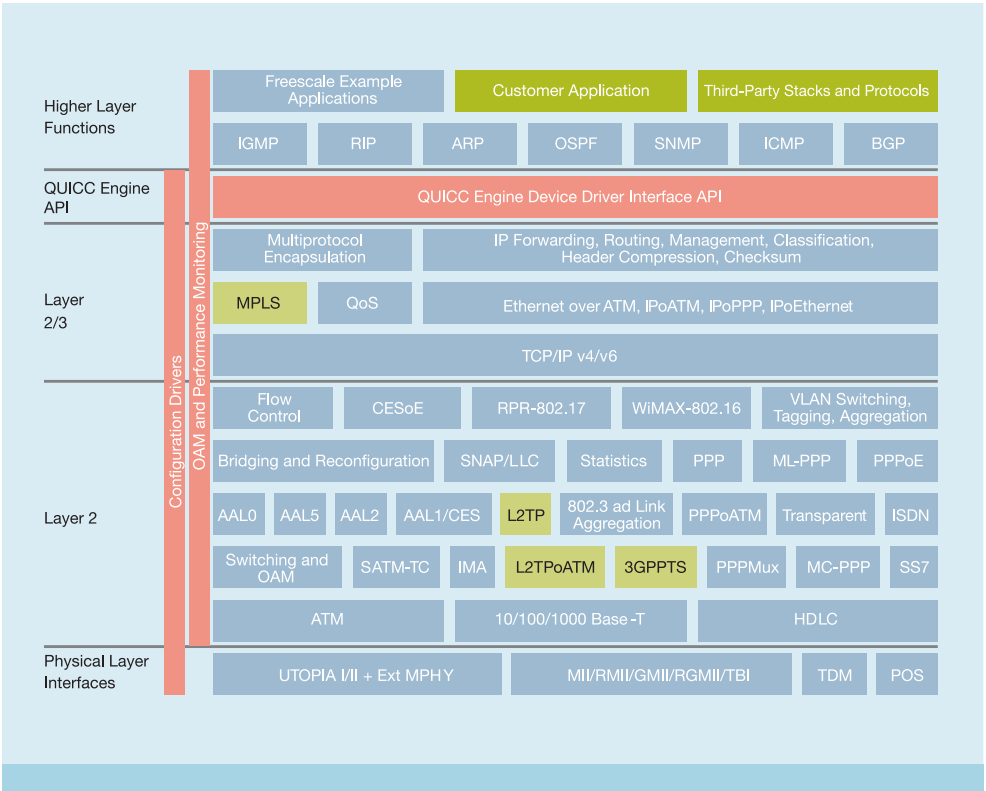
Architectural Scalability through System-on-Chip Design Methodology

The QUICC Engine uses Freescale's scalable system-on-chip (SoC) design methodology, enabling a portable piece of technology that may be used in a variety of products in a variety of configurations. QUICC Engine technology performance scales by using a multi-RISC core-scaling factor that is able to run multiple tasks concurrently. In addition, it scales in terms of frequency and technology that also enables varying levels of performance.

For more cost-sensitive applications aimed at retail and customer premises equipment, the QUICC Engine can be configured as a single RISC or dual RISC communications engine. For higher performance access, infrastructure and edge applications, it can be configured as a dual RISC communications engine and has the capacity to scale to a multi-RISC core architecture. The initial QUICC Engine is designed to support dual RISC cores implemented on the MPC8360 PowerQUICC II Pro integrated communications processor.

Scalability also is available in terms of the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC. However, with the flexibility of the SoC design methodology used for the QUICC Engine, these numbers can be scaled in both directions to support optimized mix and match of communications channels to give the right balance of price/performance, depending on the targeted application.

Software for Product Implementations of the QUICC Engine™ Technology



Software Support

The QUICC Engine technology will build upon Freescale's shrink-wrapped software protocol support for PowerQUICC processors and provide enhancements for interworking, parsing, switching and forwarding. The QUICC Engine will also be supported by a full set of configurable driver software and initialization support.

Freescale also simplifies development and speeds time to market with the CodeWarrior® QUICC Engine Utility—a GUI tool that speeds and simplifies initialization and configuration of drivers and communications protocols managed by QUICC Engine technology. The tool provides an easy-to-use environment for handling common QUICC Engine initialization tasks. Key features include:

- Automatic protocol conflict notification
- Common default values
- Point-and-click protocol selection and implementation
- Immediate access to pertinent documentation via mouse-over functionality and drop-down menus

The QUICC Engine also has a wealth of third-party software support from Freescale's Design Alliance Program, including third-party protocol and signaling stack suppliers, real-time operating systems support and a variety of applications software support. All of this builds upon the existing industry-standard PowerQUICC family support program.

Key Advantages

- High-performance, low-power and cost-effective communications processor solution
  - Convergence for packet-based networks
  - Compatibility with current PowerQUICC offerings
  - Cost-effective solution at the chip and system level
- Advanced QUICC Engine technology supporting a wide range of functionality
  - Interworking
  - Forwarding
  - Parsing
  - Switching
- DDR memory support interfaces
- Low risk of transitioning from legacy to IP-based systems
- Quick time to market enabled by software compatibility with current PowerQUICC offerings
- Low bill of material (BOM) cost

Interworking

With the potential to offer three revenue streams from a single IP packet network, the triple play of voice, video and data is the goal of every telecom operator. IP is the key enabler, and in time, it will be universal. Until then, equipment has to interoperate between circuit- and packet-switched networks and between many standards and protocols. The interoperability between standard protocols is referred to as interworking.

The QUICC Engine technology supports ATM to Ethernet interworking, without CPU intervention in support of the industry standard RFC2684 specification. In addition, the QUICC Engine can support MC/MLPPP to Ethernet interworking. It is able to perform powerful table lookup functions including multiple fields from Layers 2 to 4 without CPU intervention.

In terms of performance, the dual-RISC QUICC Engine is designed to support a throughput of up to 1.2 Gbps interworking, or 2.34 Mpps based on 64 byte packets.

Learn More: For more information about QUICC Engine and products that incorporate it or other Freescale communications processor products, please visit **www.freescale.com/QUICCEngine**.

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