ERRATA SHEET

Date: **2009 Apr 9**
Document Release: **Version 4.0**
Device Affected: **LPC2929**

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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Document revision history

Rev	Date	Description
4.0	2009 April 9	Corrected revision identifier for EEPROM.1
3.0	2009 April 1	Added EEPROM.1
2.0	2009 February 12	Updated ADC0.1 and ESD.1
1.0	2009 January 15	First version

Identification

The typical LPC2929 devices have the following top-side marking:

LPC2929xxx

xxxxxxx

xxxYYWWR

The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2929:

Revision Identifier (R)	Comment
‘0’	Second device revision
‘(blank)’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
EEPROM.1	The LPC2929 EEPROM was not trimmed at ESORT.	(blank), 0
ADC0.1	Missing Codes	(blank)

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
ESD.1	The LPC2929 does not meet the NXP QRS ESD requirements on the V_{ddosc} pin. The V_{ddosc} pin fails ESD HBM at 500 V.	(blank)

Errata Notes

Notes	Short Description	Device Revision the note applies to
N/A	N/A	N/A

Functional problems

EEPROM.1 The LPC2929 EEPROM was not trimmed at ESORT.

Introduction: Program, erase, and readback of data from the EEPROM is not reliable at the specified 375 kHz speed.

Problem: Devices with date codes on or before 0909 exhibit this issue (actual package marking ZSG09090). For products with newer date codes the EEPROM are correctly trimmed.

Work around: Use devices with date codes after 0909.

ADC0.1 Missing Codes

Introduction: The LPC2929 has a 10-bit ADC with a 5.0 V measurement range providing a total of up to 24 analog inputs with conversion times as low as 2.44 μs per channel (F_{ADC} = 4.5 MHz). Each channel provides a compare function to minimize interrupts.

Problem: On devices with date codes before 0905 and for F_{ADC} > 2.5 MHz, the 5 V ADC shows missing codes.

Work around: Limit the F_{ADCmax} for ADC0 to 2.0 MHz.

AC/DC Deviations

ESD.1 The LPC2929 does not meet the NXP QRS ESD requirements on the V_{ddosc} pin.

Introduction: The LPC2929 is rated for 2 kV ESD HBM. The V_{ddosc} pin is the power supply pin for the oscillator circuit.

Problem: On devices with date codes before 0905, the LPC2929 does not meet the required 2 kV ESD HBM specification.

Work around: Observe proper ESD handling precautions for the LPC2929.