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Engineering Bulletin

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Differences Between the DSP56301, DSP56311, and DSP56321

This engineering bulletin discusses the differences between the DSP56301, DSP56311, and DSP56321 devices.

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1 Summary of Differences

Table 1 summarizes the differences between the device families.

Table 1. Summary of DSP56301/DSP56311/DSP56321 Differences

Feature	DSP56301	DSP56311	DSP56321
Core Voltage	3.3 V	1.8 V	1.6 V
I/O Voltage	3.3 V	3.3 V	3.3 V
Max Core Frequency	80/100 MHz	150 MHz	200/220/240/275 MHz
Performance	Up to 100 MMACS	• Up to 150 MMACS • Up to 300 MMACS with EFCOP	• Up to 275 MMACS • Up to 550 MMACs with EFCOP
Packaging	208-pin TQFP 252-pin MAP-BGA	196-pin MAP-BGA	196-pin MAP-BGA
Program RAM	4 K × 24 bits	32 K × 24 bits	32 K × 24 bits
X Data RAM	2K × 24 bits	48 K × 24 bits	80 K × 24 bits
Y Data RAM	2K × 24 bits	48 K × 24 bits	80 K × 24 bits
Instruction Cache	1 K × 24 bits	1 K × 24 bits	1 K × 24 bits
Bootstrap ROM	3 K × 24 bits	192 × 24 bits	192 × 24 bits
Supported External Memory Devices	• SRAM • DRAM	• SRAM • DRAM	SRAM
External Memory Expansion	• 16 M × 24 bits Program • Two 16 M × 24 bits Data	• 256 K × 24 bits Program • Two 256 K × 24 bits Data	• 256 K × 24 bits Program • Two 256 K × 24 bits Data
DSP56300 Core	• Single clock cycle per instruction • Object-code compatible with the DSP56000 • 24-bit addressing • Barrel shifter • Six DMA channels • Debug support including OnCE, JTAG and TAP		
Coprocessor	None-	EFCOP	EFCOP
PLL	PLL and clock generator	PLL and clock generator	Clock generator with integrated DPLL
Peripherals	• Two enhanced synchronous serial interfaces (ESSI) • Serial communication interface (SCI) with baud rate generator • Triple timer module		
Host Interface	32-bit parallel PCI/Universal Bus Host Interface (HI32)	8-bit parallel HI08	8-bit parallel HI08

Table 1. Summary of DSP56301/DSP56311/DSP56321 Differences

Feature	DSP56301	DSP56311	DSP56321
General-Purpose IOs	42 GPIOs	34 GPIOs	34 GPIOs
Bootstrap Modes	• Byte-wide memory • SCI • Expanded mode • Serial EEPROM via SCI • Host modes – DSP-to-DSP – 16-bit UB – 8-bit UB – PCI target	• Byte-wide memory • SCI • Expanded mode • Host modes – ISA/DSP563xx – HC11 – 8051 – MC68302	• Byte-wide memory • SCI • Expanded mode • Host modes – ISA/DSP563xx – HC11 – 8051 – MC68302

2 Core and I/O Voltages

The DSP56301 requires 3.3 V for both the core and I/O voltage supplies. The following input pins are 5 V-tolerant:

- MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$ and MODD/$\overline{\text{IRQD}}$ pins
- PINIT/$\overline{\text{NMI}}$
- All JTAG, ESSI, SCI, Timer and HI32 pins

The DSP56311 and DSP56321 have separate core and I/O power supplies. The DSP56311 requires 1.8 V and 3.3 V for the core and I/O voltage supplies, respectively. The DSP56321 also requires 3.3 V for the I/O supply, but has a lower core voltage requirement of 1.6 V.

3 Core Frequency and Performance

The DSP56301 is available in 80 MHz and 100 MHz devices to provide 80 million-MACs-per-second (MMACS) and 100 MMACs performance.

The DSP56311 offers 150 MMACS performance with a core frequency of 150 MHz. Using the Enhanced Filter Coprocessor (EFCOP), performance can be increased to 300 MMACS.

The DSP56321 is available in different frequencies: 200 MHz, 220 MHz, 240 MHz and 275 MHz. It offers performance up to 275 MMACS or 550 MMACS with EFCOP filtering.

4 Packaging

The DSP56301 is available in 208-pin Thin Quad Flat Pack (TQFP) or 252-pin Molded Array Process-Ball Grid Array (MAP-GBA).

Both the DSP56311 and DSP56321 are available in 196-pin MAP-BGA package. These devices are pin-compatible.

5 Internal Memories

The sizes of the program RAM, instruction cache, X and Y data RAMs are programmable in all DSP563xx devices. The DSP56301, DSP56311 and DSP56321 have 8K × 24 bits, 128K × 24 bits, and 192 K × 24 bits of combined program and data RAM, respectively.

The DSP56301 has 3K × 24 bits of on-chip bootstrap ROM. Both the DSP56311 and DSP56321 have 192 × 24 bits of bootstrap ROM.

All three devices include a 1K × 24 bit instruction cache. If the instruction cache is not required, the memory space can be allocated as part of the program RAM in all three devices.

6 External Memory Expansion

The DSP56301 supports glueless interface to SRAM devices and DRAMs. Memory can be expanded up to 16 M x 24 bits for program and two 16 M × 24 bits for data memory expansion.

The DSP56311 supports glueless interface to SRAM devices. DRAM support is limited to 100 MHz. The DSP56321 only supports SRAM devices. Both devices can expand memory up to 256 K × 24 bits for program and two 256 K × 24 bits for data memory.

7 Coprocessor

The DSP56311 and DSP56321 include the Enhanced Filter Coprocessor (EFCOP) which is an internal filtering and echo-cancellation coprocessor. The EFCOP runs in parallel to the DSP core which provides increased performance. It supports various filter modes, including real and complex FIR, direct forms 1 and 2 IIR filter, adaptive filters, and others. The EFCOP runs at the same frequency as the core.

The DSP56301 does not include any filtering coprocessor.

8 PLL and Clocks

The DSP56321 uses a clock generator (CLKGEN) module with an integrated Digital Phase-Lock Loop (DPLL) circuit. This module is different from the PLL and clock generator provided in the standard DSP56300 core that is included in the DSP56301 and DSP56311.

The DSP56321 CLKGEN uses two internal registers, DPLL Static Control Register (DSCR) and DPLL Clock Control Register (PCTL) to direct the operation of the on-chip DPLL. The DSCR should be initialized before enabling the DPLL in the PCTL register.

9 Peripherals

The DSP56301, DSP5631 and DSP56321 feature the following identical peripherals:

- Two enhanced synchronous serial interfaces (ESSI) for full-duplex serial communication with codecs, microprocessors, and other DSPs
- Serial communication interface (SCI) with baud rate generator for full-duplex communication with microprocessors, other DSPs, modems, RS-232, RS-422

- Triple timer module for use as timed pulse generators or pulse-width modulators

10 Host Interface

The DSP56301 features a 32-bit parallel host interface (HI32) that can directly connect to the Peripheral Component Interconnect (PCI) bus revision 2.1 and the Universal Bus (UB) interface. In PCI mode, the HI32 is a dedicated initiator/target parallel port with 32-bit wide data path. In UB mode, the HI32 is a slave-only parallel port with 24-bit wide data path. In UB mode, the HI32 can also connect to 8-bit, 16-bit (ISA/EISA), and 24-bit (Port A bus of DSP563xx) data buses.

The DSP56311 and DSP56321 have the same byte-wide, full-duplex, parallel host interface (HI08). The HI08 operates asynchronously to the DSP core and host clocks and operates as a slave device. It provides glueless interface to various industry-standard devices, including Freescale HC11, Hitachi H8 and 8051 family of devices.

11 General-Purpose I/Os

The DSP563xx devices provide bidirectional signals that can be configured as GPIO signals or as dedicated peripheral signals. There are no dedicated GPIO signals. The DSP56301 has 42 GPIO signals, which are also used by the HI32, ESSI, SCI and Timer.

Both the DSP56311 and DSP56321 have 34 GPIOs, which are also used by the HI08, ESSI, SCI and Timer. After reset, these signals are configured as GPIO.

12 Bootstrap Modes

The DSP56301, DSP56311 and DSP56321 bootstrap program can load any program RAM segment from an external byte-wide EPROM, the SCI, or the host port. All three devices can also boot in expanded mode, in which the bootstrap ROM is bypassed and the DSP fetches instructions beginning at a specified address.

The bootstrap mode differences lie in the host modes. The DSP56301 can load program RAM segment from other DSP56301 devices in DSP-to-DSP mode. It can also load program from the host interface in the Universal Bus mode in either 8-bit or 16-bit mode or in the 32-bit PCI mode.

The DSP56311 and DSP56321 can load program RAM segment from the HI08 in the ISA, HC11, 8051 and MSC68302 modes.

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