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Changes in Process Technologies: Hardware and Software Design Implications for the DSP56300 Family

Competitive designs for wireless infrastructure applications require faster DSPs with reduced power requirements. To meet this industry demand, the Freescale DSP56300 family DSPs are based on continually evolving fabrication process technologies. This document describes the differences between DSP56300 family derivatives that use the Freescale Communication Design Rules (CDR) process technology and derivatives that use the Freescale High-Performance (HiP) process technology. Migration of DSP56300 family members from the CDR to the HiP4 process affects internal memory block size, voltage, operating frequency, and Port A timings. Further migration from HiP4 to HiP7 affects voltage, operating frequency, and Port A timings as well as completely eliminating support for DRAM.

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1 Summary of Differences

Table 1 summarizes the process-related differences presented in this document for DSP56300 family derivatives using the CDR and HiP4 process technologies and identifies related trends for future process technologies.

Table 1. Differences between CDR, HiP4, and HiP7 Processes

Feature	CDR	HiP4	HiP7
Voltage	2.5 V core 3.3 V I/O	1.8 V core 3.3 V I/O	1.6 V core 3.3 V I/O
Operating Frequency	100 MHz maximum	160 MHz maximum	275 MHz maximum
Port A Timings:			
• DRAM Access	Supported up to 100 MHz	Supported up to 100 MHz	Not supported
• SRAM Timings	Supported up to 100 MHz	Supported with added wait states	Supported with added wait states
• Synchronous Timings	Referenced to CLKOUT	CLKOUT not supported	CLKOUT not supported
• Arbitration Timings	Referenced to CLKOUT	CLKOUT not supported; asynchronous bus arbitration mode supported	CLKOUT not supported; asynchronous bus arbitration mode supported
• Address Trace Mode	Supported	Not supported	Not supported
Memory Block Size	256 x 24-bit words	1024 x 24-bit words	1024 x 24-bit words

2 Voltage

DSP56300 family members using the CDR2 process may have a power single power supply source operating at 3.3 V or a dual power system using a 2.5 V core supply and a 3.3 V I/O supply. All HiP4 and HiP7 devices have a split supply with 3.3 V I/O power as described in **Table 1** above.

3 Operating Frequency

DSP56300 family derivatives that use the CDR process technology operate at a maximum frequency of 100 MHz. HiP4 derivatives operate at up to 160 MHz. HiP7 devices operate at up to 275 MHz.

4 Port A Timings

Speed increases resulting from the application of new process technologies will affect all Port A timings as follows:

- *DRAM Access Support.* DRAM accesses are supported with DSP56300 family derivatives that use the CDR process technology at speeds up to 100 MHz. DRAM access is supported in HiP4 devices s up to 100 MHz. DRAM accessed is not supported by HiP7 process devices.
- *SRAM Timings.* SRAM accesses are supported with DSP56300 family derivatives that use the CDR process technology at speeds up to 100 MHz. HiP4 and HiP7 process DSP56300 family derivatives require additional wait states for SRAM access.

- *Synchronous Timings and Arbitration Timings*. DSP56300 family members that use the CDR process technology rely on CLKOUT as a reference signal for synchronous timings and arbitration timings. The CLKOUT output pin provides a 50 percent duty cycle output clock synchronized to the internal processor clock when the Phase Lock Loop (PLL) is enabled and locked. At speeds made possible by HiP4 and HiP7 process technologies, CLKOUT produces a low-amplitude waveform that is not usable externally by other devices. One alternative is the use of the Asynchronous Bus Arbitration mode enabled by the ABE bit in the Operating Mode Register (OMR[13]). When set, the ABE bit eliminates the setup and hold time requirements with respect to CLKOUT for $\overline{BB}$ and $\overline{BG}$.
- *Address Trace Mod*e. Address Trace mode, when available and enabled by setting the ATE bit in the Operating Mode register of DSP56300 family derivatives that use the CDR process technology, allows users to determine the address of internal memory accesses. Specifically, when ATE is set, BCLK serves as a sampling signal and results in output of the memory access address on the address lines. In derivatives that use the HiP4 or HiP7 process, neither BCLK nor the Address Trace Mode are supported.

5 Memory Block Size

DSP56300 derivatives manufactured through the HiP4 or HiP7 process technology use an internal memory block size of 1024 × 24-bit words compared to 256 x 24-bit words used by CDR derivatives. This change in size affects DMA/core contention (and EFCOP/core contention for derivatives, such as the DSP56307, that have an enhanced filter coprocessor). In CDR derivatives, the internal RAM is divided into 256-word blocks. A situation of contention exists if the core and DMA access the same block of 256 words. If both the core and DMA access the same block, then the core always has priority, and the DMA is delayed until a free slot is available. If the core and DMA access different blocks, they do not interfere with one another; each continues to operate at its maximum speed. Memory block boundaries are located at 256 word addresses. This same situation applies to HiP4 or HiP7 derivatives, except that contention exists if the core and DMA access the same block of 1024 words. Memory block boundaries are located at 1 K word addresses. To avoid DMA/core contention, DMA and core accesses must address different 1024-word blocks. **Figure 1** shows two examples of core and DMA accesses to different 256-word blocks in the DSP56307 (no contention) and the resulting effect of these same accesses in a HiP4 or HiP7 derivative.

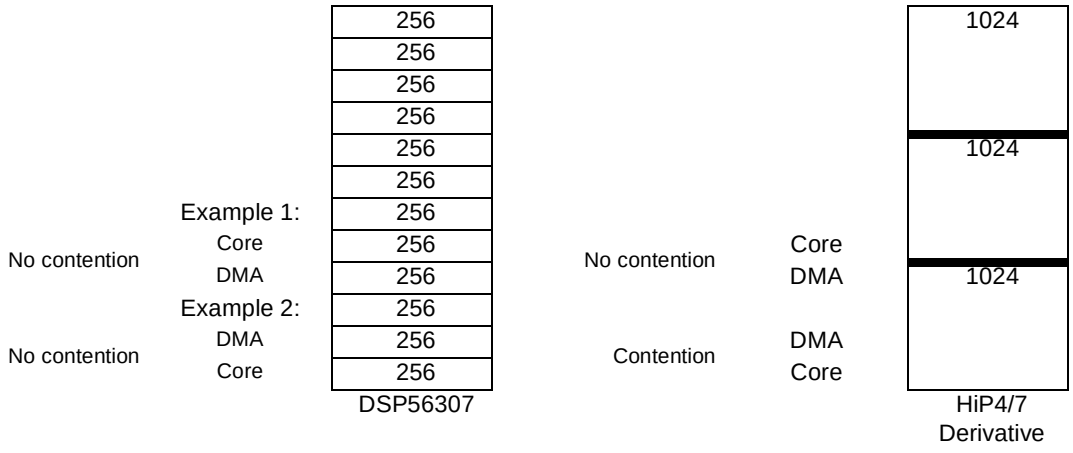

Figure 1. Memory Contention Scenarios

The same change in block size applies to EFCOP/core contention in derivatives that contain an EFCOP. Unlike Core/DMA contention, EFCOP/core contention may result in faulty data output in the Filter Data Output Register. For example, in the DSP56307, contention occurs if the EFCOP and core attempt to access the same 256 word block. In HiP4 and HiP7 derivatives, contention occurs if the EFCOP and core attempt to access the same 1 K word block. All derivatives with an EFCOP include the Data/Coefficient Transfer Contention (FCONT) bit in the EFCOP Control Status Register that allows programmers to detect when EFCOP/core contention occurs.