VR5500

Configuration report for VR5500 OTP program ID: V1

Rev 1.0 — 16 December 2019 **Report**

1 General description

The VR5500 is an automotive high voltage multi-output power supply integrated circuit, with focus on Radio, V2X and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

Note: All parametric information is maintained in VR5500 datasheet

2 Features and benefits

• 60 V DC maximum input voltage for 12 V and 24 V applications
• VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
• Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
• Low voltage integrated synchronous BUCK2 converter. Configurable output voltage and current capability up to 3.6 A peak. Multi-phase capability with BUCK1 to extend the current capability up to 7.2 A peak on a single rail. Static voltage scaling capability.
• Low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
• BOOST converter with integrated low-side switch. Configurable output voltage and max input current up to 1.5 A peak.
• EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
• Two linear voltage regulators for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
• OFF mode with very low sleep current (10 µA typ)
• Two input pins for wake-up detection and battery voltage sensing
• Device control via I2C interface with CRC
• Power synchronization pin to operate two VR5500 devices or VR5500 plus an external PMIC
• Three voltage monitoring circuits, dedicated interface for MCU monitoring, power good, reset and interrupt outputs
• Configuration by OTP programming. Prototype enablement to support custom setting

3 Applications

- Radio
- V2x
- Infotainment

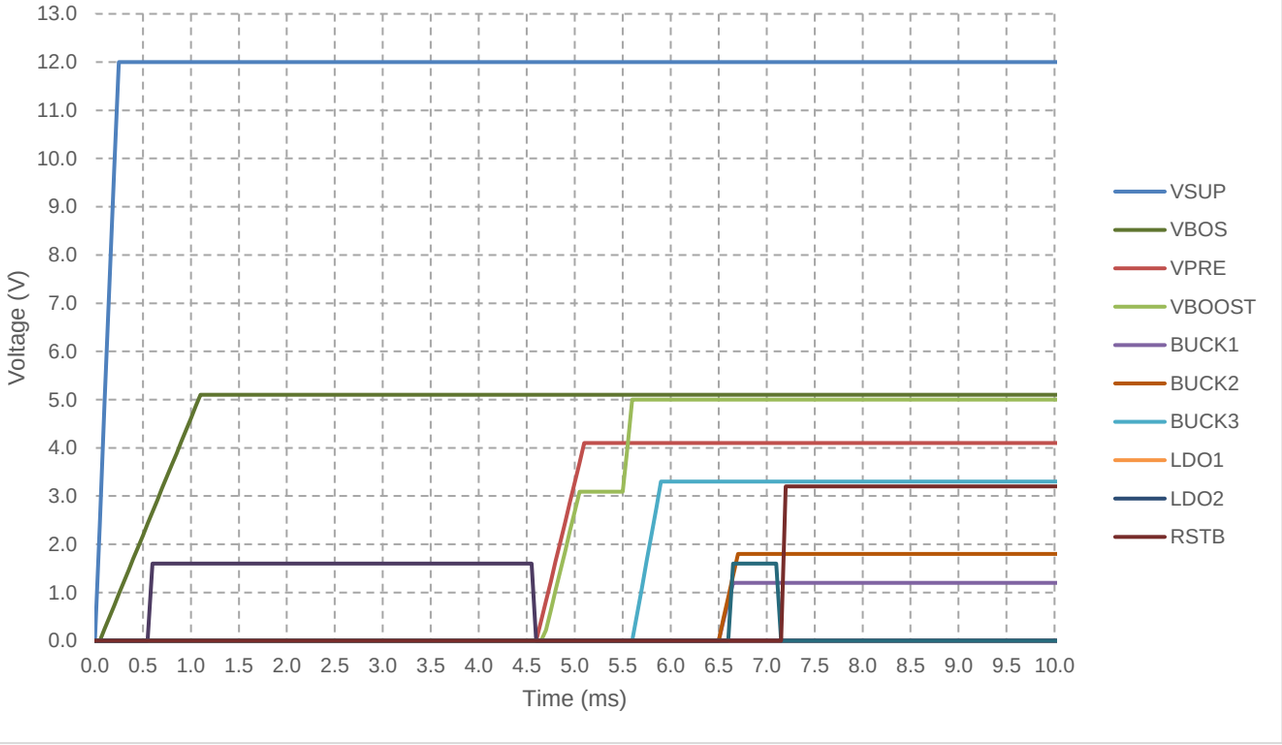
4 Ordering information

Table 1. Ordering Information

Type number[1]	Package		
	Name	Description	Version
MC33VR5500V1ES	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-23

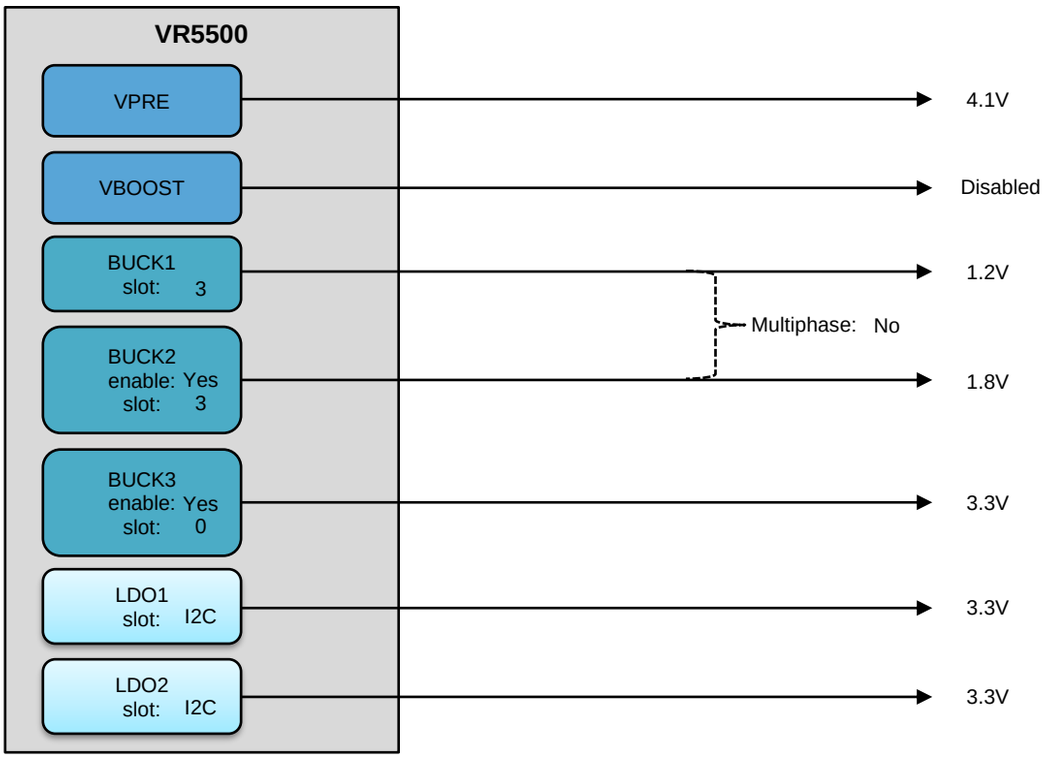
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



Note: VBOS is set at 5.1 V and RSTB at 3.2 V or 4.9 V to differentiate from regulators on the graph

6 Hardware configuration diagram



7 OTP configuration

Table 2. Main OTP configuration

Functional block	Feature	OTP selection
VPRE	Output voltage	4.1V
	Slope compensation	60mV/µs
	Current limitation	80mV
	High Side slew rate	PU/PD/130mA
	Low Side slew rate	PU/PD/900mA
	Switching frequency	455KHz
	Phase shifting	delay 0
	Turn OFF delay	32ms
	VPRE mode	Force PWM

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
VBOOST	Enabled	No
	Output voltage	5.00V
	Slope compensation	160mV/µs
	Slew rate	500V/µs
	Compensation resistor	500Kohms
	Compensation capacitor	125pF
	Switching frequency	2.22MHz
	Phase shifting	delay 0
	Behavior in case of TSD	BOOST Shutdown
BUCK1	Output voltage	1.2V
	Inductor	1µH
	Current limitation	4.5A
	Compensation network	65 GM
	Switching frequency	2.22MHz
	Phase shifting	delay 1
	Behavior in case of TSD	BUCK1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 3
	Soft start ramp	7.81mV/µs
BUCK2	Enabled	Yes
	Output voltage	1.8V
	Inductor	1µH
	Current limitation	2.6A
	Compensation network	65 GM
	Switching frequency	2.22MHz
	Multiphase with Buck1	No
	Phase shifting	delay 2
	Behavior in case of TSD	BUCK2 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 3
	Soft start ramp	7.81mV/µs

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
BUCK3	Enabled	Yes
	Output voltage	3.3V
	Inductor	1µH
	Current limitation	2.6A
	Compensation resistor	Default
	Gain control	Default
	Switching frequency	2.22MHz
	Phase shifting	delay 3
	Behavior in case of TSD	BUCK3 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 0
	Soft start ramp	10.41mV/µs
LDO1	Output voltage	3.3V
	Current limitation	150mA
	Behavior in case of TSD	LDO1 Shutdown
	Power sequencing slot	Regulator does not Start (Enabled by I2C)
LDO2	Output voltage	3.3V
	Current limitation	150mA
	Behavior in case of TSD	LDO2 Shutdown
	Power sequencing slot	Regulator does not Start (Enabled by I2C)
Miscellaneous	Power up/down slot duration	250µs
	PSYNC	1x VR5500 and 1x ext. PMIC
	PLL enabled	Yes
	Deep Fail Safe (autoretry)	x15
	VSUP power-up threshold	4.9V for Vpre < 4.5V
	Regulator assigned to VDDIO	BUCK3
	I2C address	0x20
	Device ID	00000001

Table 3. Fail-safe OTP configuration

Functional block	Feature	OTP selection
VCOREMON	Monitoring Voltage	1.2V
	OVTH	110%
	UVTH	95%
	OV_DGLT	45µs
	UV_DGLT	25µs
	SVS_CLAMP	No SVS

Table 3. Fail-safe OTP configuration (continued)

Functional block	Feature	OTP selection
VDDIOMON	Monitoring Voltage	3.3V
	OVTH	112%
	UVTH	88%
	OV_DGLT	45µs
	UV_DGLT	25µs
VMON1	OVTH	110%
	UVTH	95%
	OV_DGLT	45µs
	UV_DGLT	25µs
PGOOD	VCOREMON	No
	VDDIOMON	No
	VMON1	No
	RSTB	No
VMON1 Enable	VMON1	No
I2C	I2C address	0x21

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Date of release: 16 December 2019
Document identifier: R_VR5500V1