

# MPF5200AMBA4ES – NXP Standard

## Configuration report for PF5200-ASILB OTP program ID: A4 rev C

Rev. 1.0 - 17/09/2021

Report

### 1 General description

The PF5200 integrates multiple high performance buck regulators. It can operate as a stand-alone point-of-load regulator IC, or as a companion chip to a larger PMIC.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states.

### 2 Features and benefits

- Two high efficiency buck converters
- Watchdog timer/monitor
- Monitoring circuit to fit ASIL B safety level
- One-time programmable device configuration
- 3.4 MHz I2C communication interface
- 32-pin FC-QFN package with wettable flank

### 3 Applications

- Automotive Infotainment
- High-end consumer and industrial

### 4 Ordering information

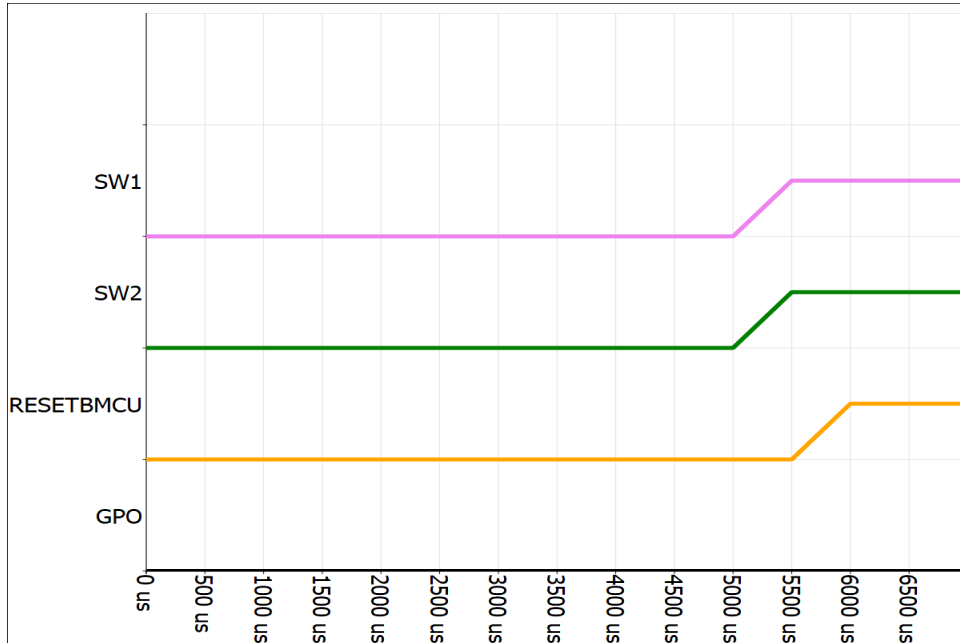
Table 1. Ordering information

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
MPF5200AMBA4ES	PQFN32	Plastic thermal enhanced very thin quad flat pack; no leads, wettable flank, 32 terminals, 0.5 mm pitch, 5 mm x 5 mm x 0.68 mm body	SOT2039 - 1(SC)

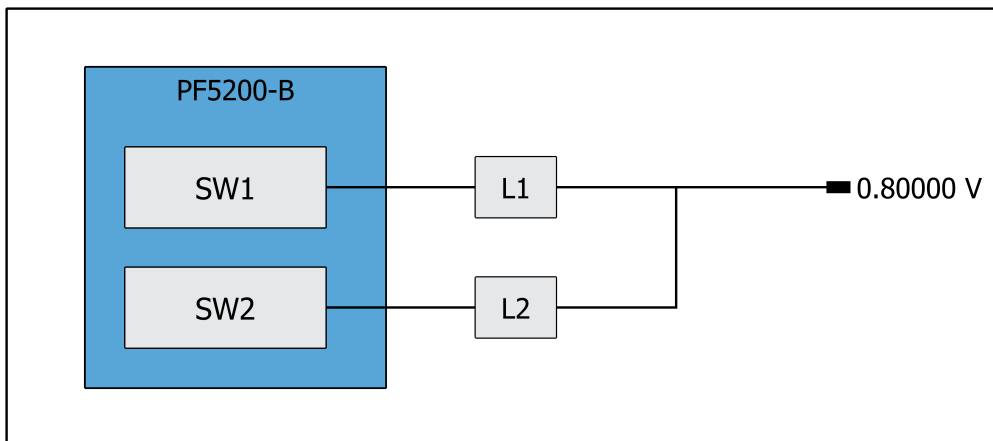
[1] To order parts in tape and reel, add the R2 suffix to the part number.



## 5 Power-up sequence summary



## 6 Hardware configuration diagram



## 7 OTP configuration

See PF5200 datasheet for parametric details. The OTP configuration summary for A4 sequence ID is provided in Tables below.

**Table 2. Device OTP configuration**

Functional block	Feature	OTP selection
System Configuration	I2C address	0x08(Default)
	I2C CRC	Enabled
	I2C secure write	Enabled
	VIN_OVLO Mode	Enabled
	VIN_OVLO shutdown	Device shuts down upon a VIN_OVLO
	Maximum fault counter	Disabled
	Fault timer	1 ms
	Fail safe state	Disabled(Follow FS State condition)
	Max FS counter	2 Events
	FS self-clear timer	1 Minute
	Bandgap comparator	Enabled (Interruption Only)
I/O CONFIGURATION	Power on event detection	Level sensitive
	PWRON debounce	Falling Edge - 32 ms and Rising Edge - 32 ms
	TRESET behavior	Shutdown
	TRESET time	2 s
	PGOOD pin operation	PGOOD mode
	PG check on power up	PG gates RESETBMCU
	EWARN delay	100 $\mu$ s
	XFAIL operation	Enabled

Configuration report for PF5200-ASILB OTP program ID: A4 rev C

Watchdog Monitoring	WD timer	Disabled
	WD window duration	1 ms
	WD clear window	Cleared within 100% timer
	WD expire number	Event on step 1
	Maximum WD event counter	1 Event
Clock Management	Nominal switching frequency	2.250 MHz
	SYNC mode	Enabled
	SYNCIN range	2000KHz to 2500KHz
	SYNCOUT enable	Disabled
	Frequency spread spectrum	Disabled
	FSS range	+/-10%

Table 3. Power Sequencer configuration

Functional block	Feature	OTP selection
Power Up Sequence	Sequence time base	500 µs
	SW1 sequence slot	Slot 10
	SW2 sequence slot	Slot 10
	RESETBMCU sequence slot	Slot 11
	PGOOD sequence slot	OFF
Power Down Sequence	Power down mode	Sequential
	SW1 Power down group	Group 4
	SW2 Power down group	Group 4
	RESETBMCU Power down	Group 4
	PGOOD Power down group	Group 4
	Power down delay	No delay

Configuration report for PF5200-ASILB OTP program ID: A4 rev C

Power down delay	Group 1 power down delay	120 $\mu$ s
	Group 2 power down delay	120 $\mu$ s
	Group 3 power down delay	120 $\mu$ s
	Group 4 power down delay	120 $\mu$ s
	RESETBMCU group delay	No delay

Table 4. SW Regulator configuration

Functional block	Feature	OTP selection
SW1	Output voltage	0.80000 V
	UV detection threshold	95 %
	OV detection threshold	105 %
	Current limit	11.0 A
	Output inductor	0.47 $\mu$ H
	Switching phase	0°
	PGOOD mode	Enabled
	SW1 OV Bypass	Protective behavior enabled
	SW1 UV Bypass	Protective behavior enabled
	SW1 ILIM Bypass	Protective behavior enabled
	DVS ramp	7.03/4.69 mV/ $\mu$ s
	SW1 gain margin	48.75 GM
SW2	Output voltage	0.80000 V
	UV detection threshold	95 %
	OV detection threshold	105 %
	Current limit	11.0 A
	Output inductor	0.47 $\mu$ H

## Configuration report for PF5200-ASILB OTP program ID: A4 rev C

	Switching phase	180°
	PGOOD mode	Enabled
	SW2 OV Bypass	Protective behavior enabled
	SW2 UV Bypass	Protective behavior enabled
	SW2 ILIM Bypass	Protective behavior enabled
	DVS ramp	7.03/4.69 mV/μs
	SW2 gain margin	48.75 GM
SW Miscellaneous	Switching Mode	PWM
	SW1 multi-phase selector	SW1/SW2 dual phase

**Table 5. PROGRAM ID**

Functional block	Feature	OTP selection
PROGRAM ID	Program ID High	A
	Program ID Low	4

## 8 Legal information

### 8.1 Definitions

**Draft** - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Limited warranty and liability** - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem

which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors here by expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Suitability for use in automotive applications** - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Export control** - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** - A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

### 8.2 Trademarks

**Notice:** All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** - is a trademark of NXP B.V.

## Contents

---

1 General description .....	1
2 Features and benefits .....	1
3 Applications .....	1
4 Ordering information .....	1
5 Power up sequence summary .....	2
6 Hardware configuration diagram .....	2
7 OTP configuration .....	3
8 Legal information .....	7

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2021 .

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 17/09/2021

Document identifier: R\_MPF5200AMBA4ES