

# PN5190B1

NFC frontend

Rev. 3.8 — 20 November 2023

Product data sheet

## 1 General description

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This document describes the functionality and electrical specification of the high-power NFC-IC PN5190B1, silicon version B1, using firmware or V2.0 or higher.

Additional documents supporting a design-in of the PN5190B1 are available from NXP, this additional design-in information is not part of this document.

The PN5190B1 supports highly innovative and unique features which do not require any host controller interaction. These features include dynamic power control (DPC), adaptive waveform control (AWC), and fully automatic EMD error handling.

The independence of real-time host controller interactions makes this product a good fit for systems which operate a pre-emptive multitasking OS like Linux or Android.

In this document, the term „MIFARE card“ refers to a contactless card using an IC out of the MIFARE Classic, MIFARE Plus, MIFARE Ultralight or MIFARE DESFire product family.



## 2 Features and benefits

### 2.1 RF functionality

- As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this NFC frontend IC utilizes an outstanding modulation and demodulation concept completely integrated for relevant 13.56 MHz based contactless communication methods and protocols.

PN5190B1 supports communication with all products of the MIFARE product-based card family including MIFARE Ultralight, MIFARE Classic 1K/4K, MIFARE DESFire EV1/EV2 and MIFARE Plus cards CRYPTO implemented in hardware for R/W of all NXP MIFARE product-based cards (includes intellectual-property licensing rights for NXP ISO/IEC 14443-A, Innovatron ISO/IEC 14443-B, and NXP MIFARE products).

The PN5190B1 frontend IC supports the following RF operating modes:

#### 2.1.1 ISO/IEC14443-A

- Reader/writer mode supporting ISO/IEC 14443-A R/W up to 848 kbit/s

#### 2.1.2 ISO/IEC14443-B

- Reader/writer mode supporting ISO/IEC 14443-B up to 848 kBit/s

#### 2.1.3 FeliCa

- Reader/writer mode supporting FeliCa 212 kBit/s and 424 kBit/s (without crypto)

#### 2.1.4 Tag type reading

- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B, type 5)

#### 2.1.5 MIFARE card reading

- Reader/writer communication mode for the MIFARE card family including MIFARE Classic

#### 2.1.6 ISO/IEC 15693

- Reader/writer mode supporting ISO/IEC 15693 (ICODE)
- Proprietary data rates based on ISO/IEC15693 with 106 kbit and 212 kbit/s (for NXP NTAG 5 communication)

#### 2.1.7 ISO/IEC 18000-3 Mode 3

- Reader/writer mode supporting ISO/IEC 18000-3 Mode 3

#### 2.1.8 ISO/IEC 18092

- ISO/IEC 18092 (NFC-IP1)

#### 2.1.9 ISO/IEC 21481

- ISO/IEC 21481 (NFC-IP-2)

#### 2.1.10 Peer to peer

- P2P Passive 106 kbit/s TO 424 kbit/s, Initiator and Target

- P2P Active 106 kbit/s TO 424 kbit/s, Initiator and Target
- Proprietary passive communication for type A up to 848 kbit/s
- Functionality according to ISO/IEC 21481 (NFC-IP-2)

### 2.1.11 Card emulation

- ISO/IEC4443-A card mode from 106 Kbit/s up to 848 Kbit/s (PICC) with active load modulation for increased communication range.

## 2.2 Host interface

- One host interface based on SPI is implemented:
  - SPI interface with data rates up to 15 Mbit/s with MOSI, MISO, NSS and SCK signals
  - Interrupt request line to inform host controller on events
  - Independent TX and RX buffer for RF data with size of 1024 bytes each

## 2.3 Integrated DC-DC

- The PN5190B1 implements an integrated DC-DC which can be used to supply the transmitter. Since the supply voltage of the transmitter LDO can be up to 6.0 Volts, this simplifies the design of the power supply. A single supply concept for the RF system, e.g. with single 3.3 V supply, is possible and allows making use of the maximum RF output power by providing a maximum transmitter supply voltage. The integrated DC-DC is used by the dynamic power control (DPC) to reduce the maximum power dissipation of the chip. The usage of the DC-DC is optional. For applications making use of the low-power card detection, the DC-DC is available. For applications using the ultra low-power card detection (ULPCD), the DC-DC cannot be used.

### **3 Applications**

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- Payment
- Physical access
- eGov

## 4 Firmware versions

Firmware versions covered by this data sheet:

### Version 2.00:

- This version cannot be replaced by FW versions using smaller version numbers (e.g. replacing FW2.0 by FW1.9 is not possible)
- This FW version is not available on volume production devices, but can be installed by the user. Before using this firmware in Peer to Peer target mode, for better communication stability the EEPROM address 0x292 (default A6E813C0) shall be initialized with the value (A6E813C1 - 0x292:0xC1 0x203: 0x13 0x294:0xE8 0x295:0xA6). This setting has no influence on reader or card emulation modes.

### Version 2.01:

- This version is functionally equivalent to Version FW2.0 but offers updated EEPROM Settings compared to FW2.0
- This version cannot be replaced by FW versions using smaller version numbers (e.g. replacing FW2.1 by FW1.9 is not possible)
- This FW version is installed by default on volume production devices of PN5190 B1
- This FW and all upcoming FW versions use the EEPROM Setting at address 0x292 = A6E813C1 to configure the Peer to Peer target mode for better communication stability.

### Version 2.02:

- Skipped, not available

### Version 2.03:

- This FW version is not available on volume production devices, but can be installed by the user
- The GPIO1 (general-purpose input/output) pin can be enabled to wake up an external DC-DC from power down for the VDDPA supply during LPCD.
- Updated Type-A 106 antenna-specific Protocol register settings for EMVCo to solve few EMVCo Card activation failures during fast card movement within the Field.
- PN5190 FW updated to handle SWITCH\_MODE\_NORMAL (Abort) scenarios even when Functional CMD and SWITCH\_MODE\_NORMAL CMD are sent to back within 10 microseconds
- Introduced a new DPC\_CONFIG register to handle Dynamic Enable/Disable of DPC without depending on the DPC setting from EEPROM User Area.
- Card Mode (SWITCH\_MODE\_AUTOCOLL Command) support with Ultra Low-Power standby feature (in Autonomous mode with Standby mode) along with the existing Low-Power standby configuration using EEPROM settings.
- various updates to increase the configuration flexibility for FeliCa communication:
  - Updated PN5190 FW to indicate Length Error when received FeliCa response is greater than 28 Bytes when RX\_MULTIPLE is Enabled
  - Updated PN5190 FW to indicate correct numbers of received bytes when RETRIEVE\_RF\_DATA is used to retrieve FeliCa response packets received when RX\_MULTIPLE is Enabled.
  - Updated to fix the issue of EXCHANGE\_RF\_DATA returning with success even before Receiving RF Response on few ICs upon POR.
  - Updated PN5190 FW to clear all pending Interrupt Status bits before performing RF Exchange to fix TX Failure observed when FeliCa response is received around FDT timeout.

- Added a new feature to extend RX Guard Timer in Integer multiple of 'dwRXIRQ\_GuardTime' EEPROM timeout configuration to extend RX Guard Timeout beyond 1.048 sec.

### Version 2.04:

Skipped, not available

### Version 2.05:

- Xtal error during boot generates error event in boot status now
- New features:
  1. Extended CONFIGURE\_TESTBUS\_ANALOG
  2. New CONFIGURE\_MULTIPLE\_TESTBUS\_DIGITAL
  3. New FastFieldOn bit in System Config register 0000h
- New registers added:
  1. TIMER0\_OUTPUT
  2. TIMER1\_OUTPUT
  3. TIMER2\_CONFIG
  4. TIMER2\_RELOAD
  5. TIMER2\_OUTPUT
- Improved setting for DPC\_GUARD\_TIME (087h): The default setting changed from 0x64 to 0xFF

### Version 2.06:

- Added a new command: GET\_CRC\_USER\_AREA[0x29]: This command is used to calculate the CRC for the complete User area including the Protocol area. This command helps the user to ensure the integrity of the RF and analog settings by detecting manipulation of this area and eases the version control of dedicated configurations during development.
- Modified SOF timing: In this FW version, the protocol settings of Type B106 had been improved for the SOF / EOF timing, and by this provides better results during EMVCo L1 analog test.

### Version 2.07:

- This version is available on the product programmed during production on product version PN5190B1.
- Fixed an issue where in commands UPDATE\_RF\_CONFIGURUATION and GET\_RF\_CONFIGURATION commands when used for TX index 0x0F (ISO180003m3\_TARI\_18.88us) and 0x10 (ISO180003m3\_TARI\_9.44us).
- Fixed an issue of not-restoring the analog TX settings when switching from reader mode to card mode. Removing of type-b detection during Autocoll. Supporting only Type-A and Type-F detection as part of an Autocoll procedure.
- Added a new EEPROM configuration: ENABLE\_ULFO\_TRIM\_CALIBRATION (0xCEC).
- Deprecated the P2P active communication target mode functionality.

## 5 Quick reference data

Table 1. Quick reference data

| Symbol          | Parameter   | Conditions   | Min  | Typ | Max  | Unit    |
|-----------------|---|--|------|-----|------|---------|
| $V_{DD(VBAT)}$  | supply voltage on pin VBAT (analog and digital supply)            | $V_{BAT} \geq V_{DDIO}$  | 2.4  | -   | 5.5  | V       |
| $V_{DD(VDDIO)}$ | supply voltage on pin VDDIO (supply for host interface and GPIOs) | 1.8 V supply   | 1.62 | -   | 1.98 | V       |
|                 |   | 3.3 V supply   | 2.4  | -   | 3.6  | V       |
| $I_{pd}$        | power down current  | $V_{DD(VDDPA)} = V_{DD(VDDIO)} = V_{DD(VDD)} = 3.0$ V; hard power down state; pin VEN set LOW, $T_{amb} = 25$ °C, External supply by VDDIO | -    | 40  | 105  | $\mu$ A |
| $I_{stb}$       | standby current   | $T_{amb} = 25$ °C  | -    | 45  | 110  | $\mu$ A |
| $I_{ULPCD}$     | average ultra-low-power card detection current                    | $T_{amb} = 25$ °C, $V_{DD(VDDPA)} = V_{DD(VDDIO)} = V_{DD(VDD)} = 3.0$ V, 330 ms Polling interval, 50 R antenna matching                   | -    | 22  | -    | $\mu$ A |
| $I_{DD(VDDPA)}$ | supply current on pin VDDPA                                       | supplied via VUP_TX (TX_LDO active)  | -    | -   | 350  | mA      |
|                 |   | supplied without DC-DC and TXLDO active  | -    | -   | 400  | mA      |
| $P_{(PA)}$      | Transmitter output power  | supplied via VUP_TX (TX_LDO active)  | -    | -   | 2.0  | W       |
|                 |   | supplied without DC-DC and TXLDO active  | -    | -   | 2.3  | W       |
| $T_{amb}$       | ambient operating temperature                                     | in still air with exposed pins soldered on a 4 layer JEDEC PCB,  | -40  | -   | +85  | °C      |
|                 |   | in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V  | -40  | -   | +105 | °C      |
| $T_{stg}$       | storage temperature   | no supply voltage applied  | -55  | -   | +150 | °C      |
| $T_{j\_max}$    | maximum junction temperature                                      | -  | -    | -   | +125 | °C      |

## 6 Ordering information

Table 2. Ordering information

| Type number      | Package |  |           |
|------------------|---------|--|-----------|
|                  | Name    | Description  | Version   |
| PN5190B1HN/C121Y | VFLGA40 | very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 6000 pcs, the ending Y in the product name is indicating the packing "reel"<br>Initialized with FW 2.1, supports encrypted firmware download                 | SOT2062-1 |
| PN5190B1HN/C121E | VFLGA40 | very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one tray, bakeable, MSL=3. Minimum order quantity = 490 pcs, the ending E in the product name is indicating the packing "single tray"<br>Initialized with FW 2.1, supports encrypted firmware download | SOT2062-1 |
| PN5190B1HN/C127Y | VFLGA40 | very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one reel, MSL=3. Minimum order quantity = 6000 pcs, the ending Y in the product name is indicating the packing "reel"<br>Initialized with FW 2.7, supports encrypted firmware download                 | SOT2062-1 |
| PN5190B1HN/C127E | VFLGA40 | very thin fine-pitch land grid array package, 40 terminals, 0.4 mm pitch, 5 mm x 5 mm x 0.8 mm body; delivered in one tray, bakeable, MSL=3. Minimum order quantity = 490 pcs, the ending E in the product name is indicating the packing "single tray"<br>Initialized with FW 2.7, supports encrypted firmware download | SOT2062-1 |
| PN5190B1EV/C121Y | VFBGA64 | plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br>The ending Y in the product name is indicating the packing "reel"<br>Initialized with FW 2.1, supports encrypted firmware download                       | SOT1307-2 |
| PN5190B1EV/C121E | VFBGA64 | plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 490 pcs<br>The ending E in the product name is indicating the packing "single tray"<br>Initialized with FW 2.1, supports encrypted firmware download                 | SOT1307-2 |
| PN5190B1EV/C127Y | VFBGA64 | plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs<br>The ending Y in the product name is indicating the packing "reel"<br>Initialized with FW 2.7, supports encrypted firmware download                       | SOT1307-2 |
| PN5190B1EV/C127E | VFBGA64 | plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm, delivered in one tray, MSL = 3. Minimum order quantity = 490 pcs<br>The ending E in the product name is indicating the packing "single tray"<br>Initialized with FW 2.7, supports encrypted firmware download                 | SOT1307-2 |



7 Block diagram with VFBGA64 connections

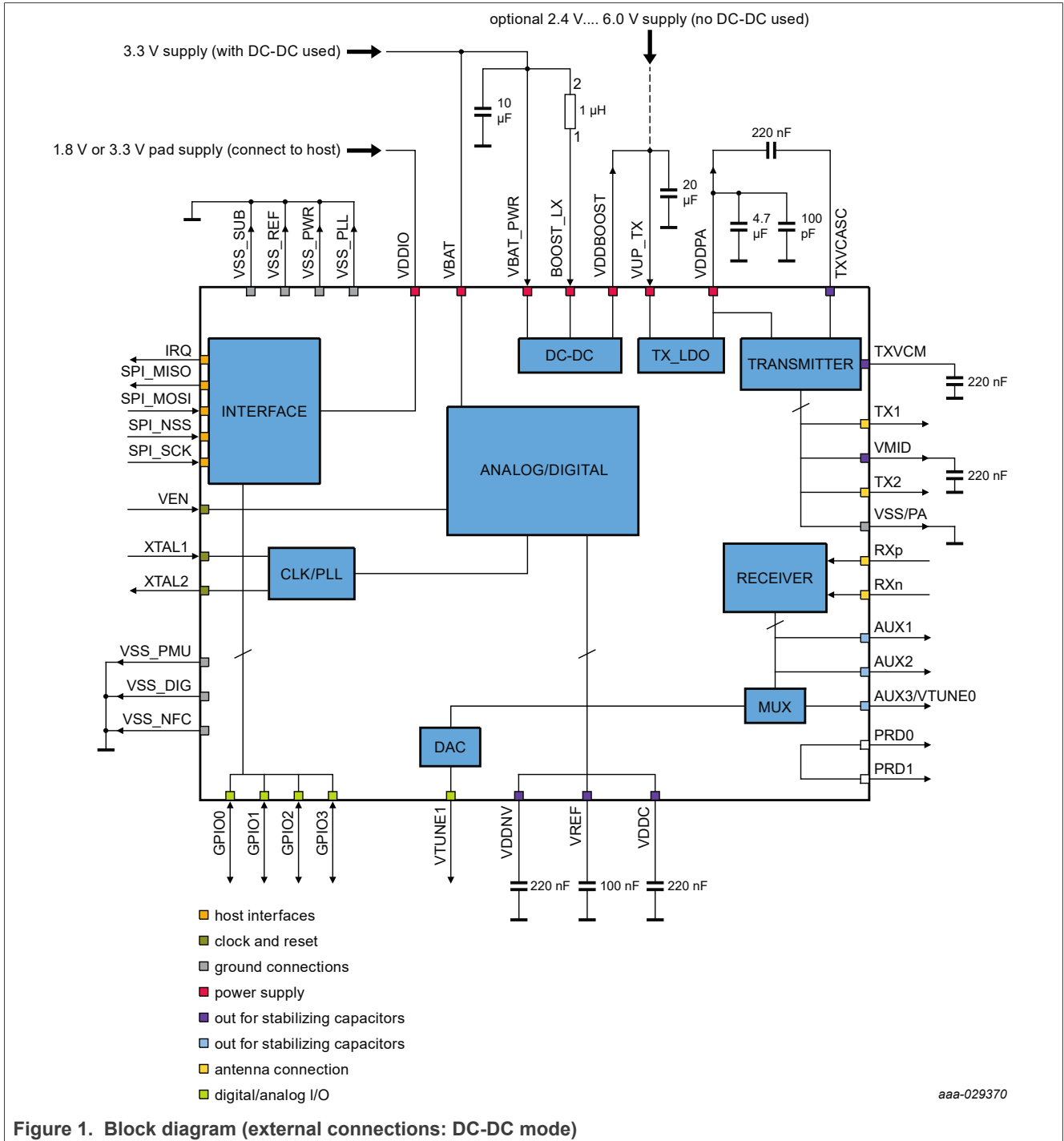


Figure 1. Block diagram (external connections: DC-DC mode)

## 8 Pinning information

### 8.1 Pin description VFBGA64

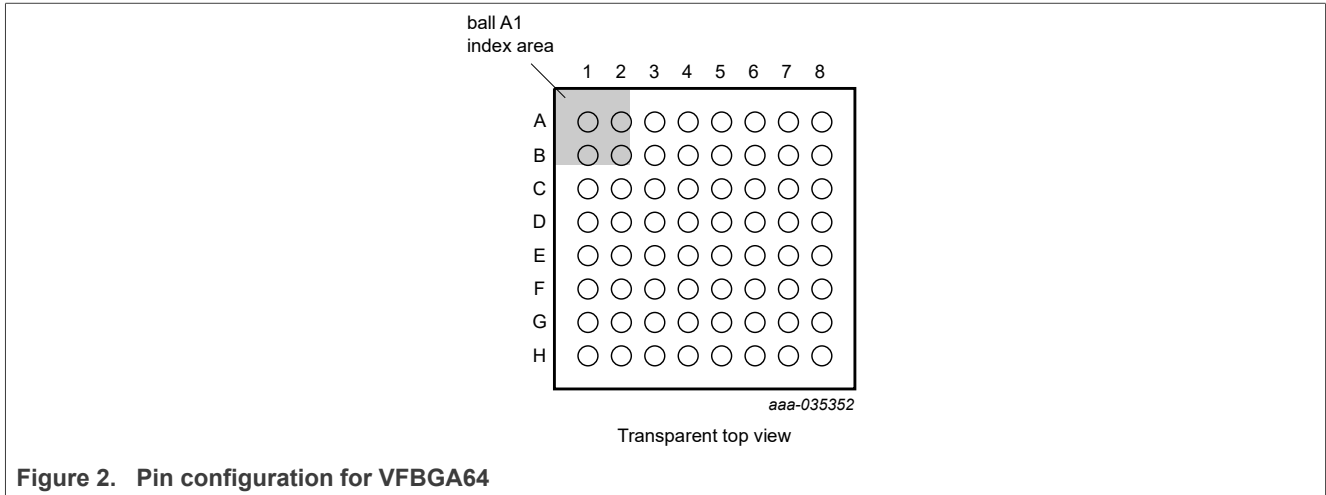


Table 3. Pin description VFBGA64

| Pin Number            | Symbol  | Type       | Description  |
|-----------------------|---------|------------|--|
| <b>Host Interface</b> |         |            |  |
| E6                    | ATX_A   | Output     | SPI target <sup>[1]</sup> data output  |
| E5                    | ATX_B   | Input      | SPI clock input  |
| D6                    | ATX_C   | Input      | SPI target select input  |
| D5                    | ATX_D   | Input      | SPI target data input  |
| B7                    | IRQ     | Output     | Host communication/ event interrupt signal   |
| F8                    | XTAL1   | Input      | Crystal / system clock input   |
| G8                    | XTAL2   | Output     | Clock output (amplifier-inverted signal output) for crystal  |
| B3                    | VEN     | Input      | Hardware reset, low active (independent from V <sub>VDDIO</sub> )<br>Avoid a floating or unexpected toggling of the pin. |
| <b>Supply pins</b>    |         |            |  |
| H2                    | VSS_PA  | Supply GND | Transmitter ground   |
| G3                    | VSS_PLL | Supply GND | PLL ground (low noise)   |
| A2                    | VSS_PWR | Supply GND | DC-DC boost ground   |
| D3                    | VSS_REF | Supply GND | PMU ground   |
| B2, E3                | VSS_SUB | Supply GND | Substrate ground   |
| C3                    | VSS_PMU | Supply GND | PMU ground   |
| F4                    | VSS_DIG | Supply GND | Digital ground   |
| F3                    | VSS_NFC | Supply GND | NFC ground   |
| E1                    | VBAT    | Supply     | System supply, used to supply the analog and digital blocks, memory and internal voltage references                      |

Table 3. Pin description VFBGA64...continued

| Pin Number                               | Symbol         | Type             | Description  |
|--|----------------|------------------|--|
| A8                                       | VDDIO          | Supply           | I/O pads power supply  |
| G1                                       | VDDPA          | Supply           | Transmitter supply   |
| F1                                       | VUP_TX         | Supply           | Input supply voltage for transmitter LDO   |
| B1                                       | VDDBOOST       | Supply           | DC-DC boost supply   |
| A1                                       | BOOST_LX       | Output           | Boost inductance loopback, to be connected to boost inductor   |
| A3                                       | VBATPWR        | Supply           | To be connected to boost inductor and transmitter power supply   |
| <b>Outputs for stabilizing cap</b>       |                |                  |  |
| A4                                       | VDDNV          | Output           | Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap  |
| D2                                       | VREF           | Output           | High quiescent reference voltage, to be connected to ground via 100 nF blocking cap  |
| C1                                       | VDDC           | Output           | Power supply for Digital Core, to be connected to ground via 220 nF blocking cap   |
| G2                                       | TXVCM          | Output           | Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap   |
| F2                                       | TXVCASC        | Output           | TX decoupling cap, to be connected to VDDPA  |
| H6                                       | VMID           | Output           | Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) by 100 nF blocking cap |
| <b>RF Debug signals</b>                  |                |                  |  |
| G7                                       | AUX_1          | Output           | Test bus 1   |
| F7                                       | AUX_2          | Output           | Test bus 2   |
| H8                                       | AUX_3 / VTUNE0 | Output           | Test bus 3 / VTUNE0 (digital-to-analog output 0)   |
| <b>Antenna connections</b>               |                |                  |  |
| H5                                       | RXP            | Input            | Receiver input "Positive"  |
| H4                                       | RXN            | Input            | Receiver input "Negative"  |
| H1                                       | TX1            | Output           | Antenna driver output 1  |
| H3                                       | TX2            | Output           | Antenna driver output 2  |
| <b>Analog/Digital inputs and outputs</b> |                |                  |  |
| H7                                       | VTUNE1         | Output           | Digital-to-analog output 1   |
| E8                                       | GPIO0          | Input/<br>Output | General Purpose Output 0   |
| D8                                       | GPIO1          | Input/<br>Output | General Purpose Output 1   |
| E7                                       | GPIO2          | Input/<br>Output | General Purpose Output 2   |
| D7                                       | GPIO3          | Input/<br>Output | General Purpose Input/Output 3<br>If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.                            |

Table 3. Pin description VFBGA64...continued

| Pin Number                                | Symbol       | Type             | Description  |
|---|--------------|------------------|--|
| <b>Security feature</b>                   |              |                  |  |
| B4  | PRD1         | Input/<br>Output | Package removal detection, internally connected to PRD2  |
| G4  | PRD2         | Input/<br>Output | Package removal detection, internally connected to PRD1  |
| <b>Pins connected on PN76 family only</b> |              |                  |  |
| A5  | PVDD_OUT     | Output           | Do not connect   |
| A6  | I2CM_SDA     | Input/Output     | Do not connect   |
| A7  | DWL_REQ      | Input            | Recommended: Do not connect - entering secure firmware download by command.<br>If connected, this pin allows to enter the Secure firmware download mode if set high during hardware reset. |
| B5  | GPIO5        | Input/Output     | Do not connect   |
| B6  | I2CM_SCL     | Input            | Do not connect   |
| B8  | SWDIO        | Input/Output     | Do not connect   |
| C2  | TEST         | Input/Output     | Internal test pin. Do not connect  |
| C4  | ISO_INT_AUX  | Input/Output     | Do not connect   |
| C5  | GPIO4        | Input/Output     | Do not connect   |
| C6  | HOST_IF_SEL1 | Input            | Do not connect   |
| C7  | HOST_IF_SEL0 | Input            | Do not connect   |
| C8  | SWD_CLK      | Input            | Do not connect   |
| D1  | USB_VBUS     | Input            | Do not connect   |
| D4  | ISO_IO_AUX   | Input/Output     | Do not connect   |
| E2  | AD1          | Input            | Do not connect   |
| E4  | ISO_CLK_AUX  | Input            | Do not connect   |
| F5  | SPIM_MOSI    | Input            | Do not connect   |
| F6  | SPIM_MISO    | Output           | Do not connect   |
| G5  | SPIM_SCLK    | Input            | Do not connect   |
| G6  | SPIM_NSS     | Input            | Do not connect   |

[1] Updated the terms "master/slave" to "controller/target" to align with the recommendation of the NXP - I<sup>2</sup>C and JEDEC SPI standards organization

For good RF performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

8.2 Pin description VFLGA40

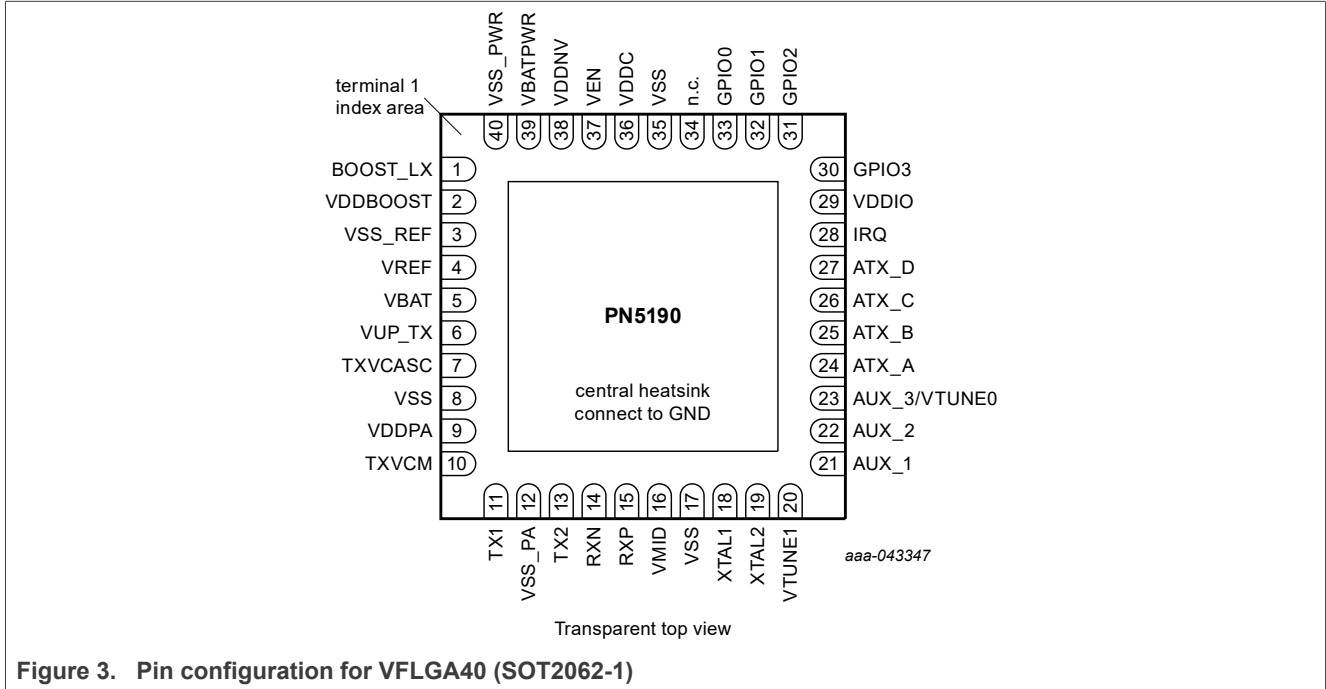


Table 4. Pin description VFLGA40

| Pin Number | Symbol   | Type       | Description   |
|------------|----------|------------|---|
| 1          | BOOST_LX | Output     | Boost inductance loopback, to be connected to boost inductor pin 1                                  |
| 2          | VDDBOOST | Supply     | Boosted supply voltage output   |
| 3          | VSS_REF  | Supply GND | PMU ground  |
| 4          | VREF     | Output     | High quiescent reference voltage, to be connected to ground via 100 nF blocking cap                 |
| 5          | VBAT     | Supply     | System supply, used to supply the analog and digital blocks, memory and internal voltage references |
| 6          | VUP_TX   | Supply     | Input supply voltage for transmitter LDO  |
| 7          | TXVCASC  | Output     | TX decoupling cap, to be connected to VDDPA   |
| 8          | VSS      | Supply GND | Ground  |
| 9          | VDDPA    | Supply     | Transmitter supply  |
| 10         | TXVCM    | Output     | Transmitter voltage common mode, to be connected to ground via 220 nF blocking cap                  |
| 11         | TX1      | Output     | Antenna driver output 1   |
| 12         | VSS_PA   | Supply GND | Transmitter ground  |
| 13         | TX2      | Output     | Antenna driver output 2   |
| 14         | RXN      | Input      | Receiver Input "Negative"   |
| 15         | RXP      | Input      | Receiver input "Positive"   |

Table 4. Pin description VFLGA40...continued

| Pin Number | Symbol         | Type         | Description   |
|------------|----------------|--------------|---|
| 16         | VMID           | Output       | Stabilizing capacitor connection output, to be connected to electrical symmetry point of antenna (typically antenna ground) |
| 17         | VSS            | Supply GND   | Ground  |
| 18         | XTAL1          | Input        | Crystal / System clock input  |
| 19         | XTAL2          | Output       | Clock output (amplifier-inverted signal output) for crystal   |
| 20         | VTUNE1         | Output       | Digital-to-analog output 0  |
| 21         | AUX_1          | Output       | Test bus 1  |
| 22         | AUX_2          | Output       | Test bus 2  |
| 23         | AUX_3 / VTUNE0 | Output       | Test bus 3 / VTUNE0 digital-to-analog output 1  |
| 24         | ATX_A          | Output       | SPI target data output  |
| 25         | ATX_B          | Input        | SPI clock input   |
| 26         | ATX_C          | Input        | SPI target select input   |
| 27         | ATX_D          | Input        | SPI target data input   |
| 28         | IRQ            | Output       | Host communication/ event Interrupt signal  |
| 29         | VDDIO          | Supply       | I/O pads power supply   |
| 30         | GPIO3          | Input/Output | General Purpose Input/Output 3 -<br>If ULPCD is used, GPIO3 cannot be used for any other purpose than aborting the ULPCD.   |
| 31         | GPIO2          | Input/Output | General Purpose General Purpose Output 2  |
| 32         | GPIO1          | Input/Output | General Purpose General Purpose Output 1  |
| 33         | GPIO0          | Input/Output | General Purpose General Purpose Output 0  |
| 34         | n.c.           | -            | -   |
| 35         | VSS            | Supply GND   | Ground  |
| 36         | VDDC           | Output       | Power supply for Digital Core, to be connected to ground via 220 nF blocking cap  |
| 37         | VEN            | Input        | Hardware reset, low active (independent from $V_{PVD}$ )<br>Avoid a floating or unexpected toggling of the pin.             |
| 38         | VDDNV          | Output       | Non-volatile memory power supply, to be connected to ground via 220 nF blocking cap   |
| 39         | VBAT_PWR       | Supply       | To be connected to boost inductor pin 2 and transmitter power supply  |
| 40         | VSS_PWR        | Supply GND   | DC-DC boost ground  |

For best performance, all blocking capacitors shall be placed on the same side of the PCB, traces from pin to capacitor shall be as short as possible.

Compared to the BGA package, all ground connections named VSS are connected on the leadframe of the package. Therefore general VSS pins do exist, pins are not distinguished by function like on the BGA package type e.g. VSS\_PMU. The exceptions are the pins VSS\_PWR, VSS\_PA and VSS\_REF.

All Supply GND connections shall be connected by low-ohmic connections on the PCB.

## 9 Functional description

### 9.1 Functional overview

The PN5190B1 is an NFC frontend with high transmitter output power. It implements the RF functionality like an antenna driving and receiver circuitry and all the low-level functionality to realize an NFC Forum and EMVCo compliant reader.

#### Connection to host controller

The PN5190B1 connects to a host microcontroller with a fast SPI interface (15 Mbit/s) for configuration, NFC data exchange and high-level NFC protocol implementation. An optimized TLV-based framing is supported to reduce the command handling overhead on the host controller and to reduce command-response latencies.

#### Clock supply

The PN5190B1 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. Alternatively, an internal PLL allows using an accurate external clock source of either 24 MHz, 32 MHz and 48 MHz (configured in EEPROM register CLK\_INPUT\_FREQ, 0012h)). This allows saving the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies.

#### Integrated DC-DC

The integrated DC-DC allows a single supply voltage while delivering maximum RF output power. Dependent on the application target either a direct transmitter supply or a transmitter supply by the integrated DC-DC can be chosen. The usage of the integrated DC-DC is the preferred choice for a stable RF performance, even in case of a de-charged battery. Optimized usage of a battery charge can be achieved by directly connecting the transmitters to the supply. The DC-DC is controlled by the Dynamic Power Control 2.0 to keep the power dissipation of the chip minimized in antenna loading cases which require a reduction of the RF output power.

The DC-DC is a step-up converter and is able to deliver an output voltage from approx. 2.8 V up to 6.0 V. The targeted output voltage can be configured by software.

The DC-DC clock is synchronized with the clock of the receiver - this avoids the typical performance reduction by DC-DC noise which can be seen in systems using external DC-DCs.

#### Transmitter LDO (TX\_LDO)

The Transmitter output drivers are supplied by a transmitter LDO which reduces external noise and is used for the DPC functionality to lower the supply voltage of the transmitters. The high granularity of 100 mV for setting the TX\_LDO output voltage together with a sophisticated control loop and true current measurement ensures that a DPC regulation is not accidentally treated as received data.

#### Low-power card detection

The low-power card detection (LPCD) allows saving battery charge during polling for NFC counterparts like cards and mobile phones. In general, the low-power card detection provides a functionality, which allows to power down the reader for a certain amount of time to save energy. After some time, the reader becomes active again to poll for cards. If no card is detected, the reader can go back to the power down state. During the polling time, a host controller can be set to a power-saving mode. An interrupt request from the PN5190B1 allows waking up the host controller in case an antenna detuning by a card or cell phone had been detected.

Two modes for the low-power card detection are available:

- LPCD (software based) which allows maximum detection range. For detecting a card presence, I/Q channel information is used.
- ULPCD (hardware based) which offers maximum current savings. For detecting a card presence, only the amplitude information is used.

### Dynamic power control 2.0

The next generation Dynamic Power Control (DPC2.0) with true transmitter current measurement works autonomous without host interaction. Avoiding additional host controller processing load is important for time critical applications like payment. A fast control response time of less than 1 ms allows using optimized antenna matchings.

### Adaptive wave shape control

The Adaptive Wave Shape Control (AWC) helps to keep the waveshapes within specification limits, even in case of antenna detuning. This simplifies the time-consuming antenna matching procedure and does not require any matching compromises to be taken.

### Receiver signal level control

The receiver signal chain consists of an automatic controller RF input attenuator and a true Baseband Amplifier (BBA). This feature delivers an outstanding communication range with tags, labels, cards and mobile phones.

### RF Debugging

Comprehensive and innovative debug features are implemented to support the NFC reader development even for difficult and non-standard compliant cards and mobile phones. An Integrated Chip scope allows performing a non-intrusive debugging of receiver signals without the need of connecting additional wires to the chip. Capturing of chip-internal signals is done by configuring flexible trigger conditions, sampled internal data is stored in RAM memory, transferred by SPI to a host microcontroller and visualized on a PC by the NFC Cockpit development tool. A virtual comfort interface (VCOM) is supported by the NFC cockpit tool, which allows to use the NFC cockpit together with any host microcontroller. Analog debug signals (AUX1, AUX2) are available as well and allow the connection of an Oscilloscope for analog and digital signal debugging.

The receiver signal processing is optimized to cope with noisy environments. This is beneficial, especially in case a TFT display or DC-DCs are part of the NFC system.

### Automatic EMD error handling

An automatic EMD handling performed without host interaction relaxes the timing requirements on the Host Controller. Automatic EMD error handling according to ISO/IEC14443 and EMVCo 3.0 is supported. In addition, the EMD error handling is widely configurable, which allows adaptations in case of future possible specification changes.

### Automatic antenna tuning

Two analog outputs are available to connect variable capacitors for automatic antenna tuning (AAT). The automatic antenna tuning allows compensating for production tolerances or changing environments like surrounding metal. This is especially beneficial for applications which make use of OEM NFC Modules which are finally used in an unknown environment. The automatic antenna tuning is performed command triggered.

### Firmware update

The PN5190B1 supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set, but a framing which is not different from the standard host interface commands used for NFC operation of the device. In Secure Firmware update mode, the PN5190B1 requires no dedicated physical handling of the SPI interface lines. The firmware download does not require any additional hardware pin to be handled, instead the download mode is activated by a command, followed by a hardware reset. After booting from reset, the PN5190B1 will be in download mode.

### Register configuration

Internal registers of the PN5190B1 store volatile configuration data and accessible by the host interface. The internal registers are reset to configurable initial values in case of powerON, hardware-reset and standby.



The configuration for dedicated RF protocols and antenna-dependent configuration is defined in non-volatile memory. This configuration is typically done only once during production, and is performed by a command issued from the host microcontroller.

### EEPROM configuration

Non-Volatile EEPROM memory of the PN5190B1 is used to store configuration data that needs to be preserved in case the PN5190B1 is not connected to any supply voltage. The configuration for dedicated RF protocols and antenna-dependent configuration is defined in this non-volatile memory and copied to volatile registers by a host interface command. In addition, other configuration data which needs to be preserved during power supply disconnect is stored in this EEPROM memory as well. Examples for this are configurations for DPC, LPCD and ULPCD configurations.

### RF configuration

The PN5190B1 allows a fast RF protocol selection based on the command Load\_RF\_configuraton and pre-defined user configuration data in non-volatile memory (EEPROM).

On the one hand, the configuration of modulation-related parameters can be done (e.f. selection of ISO/IEC14443-A), on the other hand antenna-specific parameters can be configured.

For more information, see [\[1\]](#).

## 9.2 Endianness

The endianness describes the order of bytes or bits within a binary representation of a value in the memory, which can be a register or EEPROM.

"Array size" defines the number of elements of "type size". Type size can be uint8 (8 bit), uint16 (16 bit) or uint32 (32 bit).

The location of byte-sized data (8 bit) with an array size of 2 is as follows:

Value hex: 0x1234

address x: 12

address x+1: 34

The location of word-sized data (16 bit) is as follows:

Value hex: 0x1234

address x: 34

address x+1: 12

The location of word-sized data (16 bit) in an array size of 2 is as follows:

The placement of the array is large endian, the placement of nibbles of the variable is small endian.

Value hex: 0xAABBCCDD

address x: BB

address x+1: AA

address x+2: DD

address x+3: CC

The location of double word-sized data (32 bit) is as follows:

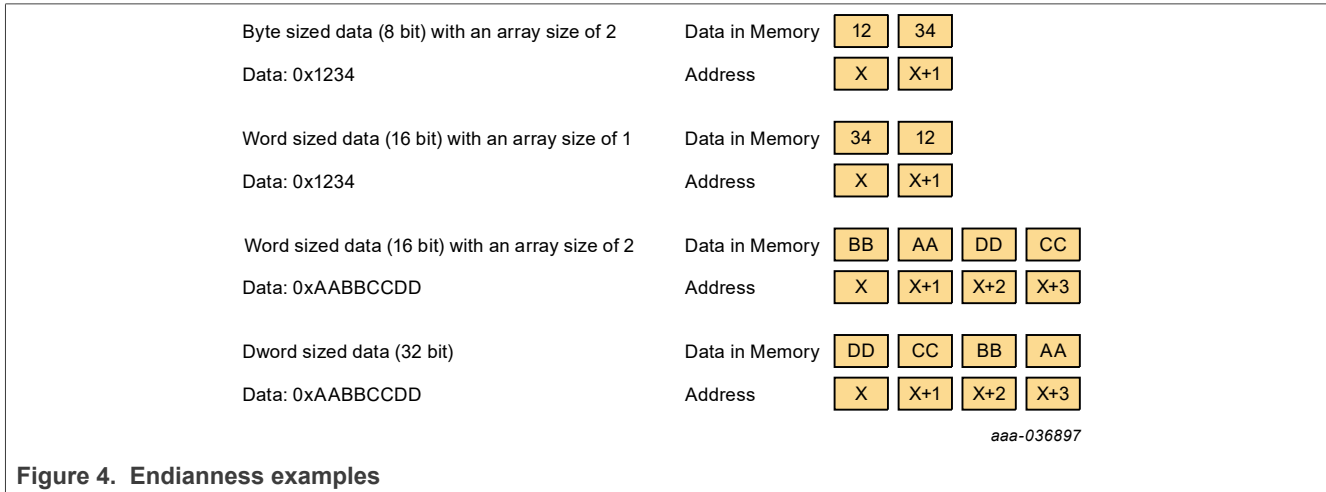
Value hex: 0xAABBCCDD

address x: DD

address x+1: CC

address x+2: BB

address x+3: AA



Data from the EEPROM is read in little-endian format - LSB first. This means that the byte at the lower address is read first.

### 9.3 Initial calibration

The PN5190B1 requires a calibration before the RF field is switched on for the first time with unloaded condition.

"Unloaded" means: Without any additional metal in proximity of the antenna, except for the NFC reader components itself.

During development of new readers, this calibration shall be done each time the antenna design, antenna matching, or EMC filter is modified.

The calibration sequence is the following:

Write EEPROM CfgNovCal (0xC83) – 0x40

Write REGISTER TX\_NOV\_CALIBRATE\_AND\_STORE (addr: 0x5d) - 0x01

Write EEPROM CfgNovCal (0xC83) – 0x42

### 9.4 System power states

The PN5190B1 can operate in different power states. The functionality and current consumption is dependent on the actual system power state.

Power states can be changed by the level on the pin VEN and by connecting/disconnecting the power supply of VBAT. Power state change will also be triggered by certain events - VDDIO Loss, overcurrent detection, overtemperature.

In addition, state changes are triggered possible by host commands.

Disconnecting and connecting the power supply on VBAT restarts the PN5190B1 always in Active State after releasing the pin VEN (transition low to high).

A transition of low to high on pin VEN restarts the PN5190B1 always in Active State.

The following power states are supported:

| Power state     | Description   | typical current consumption        |
|-----------------|---|------------------------------------|
| Power OFF       | The NFC system (supply pin VBAT, RF transmitter) is not supplied by a battery/system PMU. Other domains might be supplied (for example, I/O pad interface on pin VDDIO).<br>In all other power states, the Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in power off mode.<br>Device is not functional  | -                                  |
| PMU OFF         | The NFC system is disabled by the host via a low signal on pin VEN. No internal clocks of the PN5190B1 are active. Entry to PMU OFF can also be triggered by power loss on VDDIO. Wake-up events to change PMU OFF state: Power reset on pin VBAT, VEN rising edge, RX ULPCD detect, ULP abort signal on PIN3, VDDIO restore.   | 5 µA                               |
| ULP standby     | The host can set the PN5190B1 into Ultra-low power card detection state (ULP Standby state) via programming of the ULPCD bit (Switch mode command).<br>In the ULP standby state, the PN5190B1 is able to activate the transmitter and receiver after defined time (expiry of wake-up timer) to detect the card. If a card is not detected, the transmitter and receiver is deactivated and the wake-up timer restarted. Power consumption of ULP Standby mode is much lower than Hard power down State and standby State. Only the wake-up timer is active during ULP standby state<br>Wake-up events: Power reset on pin VBAT, VEN rising edge, GPIO3 level, Card detected.<br>Variant 1: Configurable wake-up timer allows system to boot into active<br>Variant 2: Configurable wake-up timer allows checking regularly for a card in the field. | Variant 1: 5 µA<br>Variant2: 22 µA |
| Hard power down | The NFC system is disabled by the Host system via the reset/enable signal on VEN or by detecting an external condition (for example, battery voltage monitor). The power dissipation is reduced to a minimum. No power dissipation or leakage is expected on the different interfaces. Low-power resources are enabled (VDDC_LP, VHV_LP, LQ_REF, LQ-BIAS). LFO clock is available. PCRM is supplied and is running in low-power state. I/Os are supplied by VDDC_HP. Wake-up events: Power reset on pin VBAT, VEN rising edge, RX ULP detect  | 40 µA                              |
| Standby         | The NFC system can be switched into a low-power mode to minimize power dissipation. The RF functionality is not available in this case. The state of external interfaces is maintained properly. PMU operates in low-power state. Wake-up counter clock is available. PCRM is supplied and running in low-power mode. I/Os are supplied by VDDC_LP. PMU FSM in PCRM manages the transition in power state. Wake-up sources: Activity on host IF, SWPM communication, ULPDET, LPDET, wake-up counter, power loss on VDDIO, GPIO, RxPROT, No High Temp on TX and so on.   | 45 µA                              |
| Suspend         | All power sources are available. LFO and HFO clocks are available. CPU subsystem clock sources are gated, except for the LFO. I/Os are available.   | 2.5 mA                             |

| Power state | Description   | typical current consumption       |
|-------------|---|-----------------------------------|
| Active      | The PN5190B1 is able to process internal or external events or data. All external power supply sources and the external clock need to be available, and all internal clocks are active. | 20 mA (system without RF current) |

## 9.5 Power supply

The device allows to configure different power supply options for the transmitter power amplifier. To make use of them, a combination of external connections and chip internal configurations needs to be done. The following supply options are available:

- Internal VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX\_LDO). In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX\_LDO is adding an improved rejection of noise on the supply lines.
- Direct VDDPA configuration: This configuration is recommended for applications which require highest efficiency, like battery supplied devices. In this configuration, a battery can be connected directly to the transmitter supply avoiding the voltage drop of approximately 0.3 V caused by the TX\_LDO. A clean supply voltage without noise is required to achieve a good RF performance. In this configuration the DPC, current measurement and overcurrent protection is not available.

### 9.5.1 System power supply overview

The PN5190B1 is using three different supplies each for the following functional blocks:

1. Supply for the host interface and GPIO's (VDDIO)
2. Supply for the analog and digital blocks (VBAT/VBAT\_PWR)
3. Supply of the RF drivers (VDDPA), DC-DC (VBAT\_PWR) and TX\_LDO (VUP)

The functionality of the GPIO's, Host Interface and internal analog and digital blocks is independent from the supply of the RF Driver. This allows to configure a dedicated transmitter supply configuration at any time. Care shall be taken to switch on the RF field only after the transmitter-related power supply had been configured according to the external physical supply connections (VDDPA, VBAT\_PWR, VUP).

The power supply configuration is configured in EEPROM and therefore will not get lost in case of power supply loss or reset of the chip. Typically, this configuration is only performed once during the production of a reader.

RF field shall not be turned on without setting the correct power supply configuration in the EEPROM.

**Note:** The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in Power off mode.

### 9.5.2 Connecting blocking capacitors

Some pins are connected to blocking supply capacitors. PCB traces to these capacitors need to be as short as possible, and a low-ohmic grounding of the GND-side of the capacitors is required for optimized RF performance.

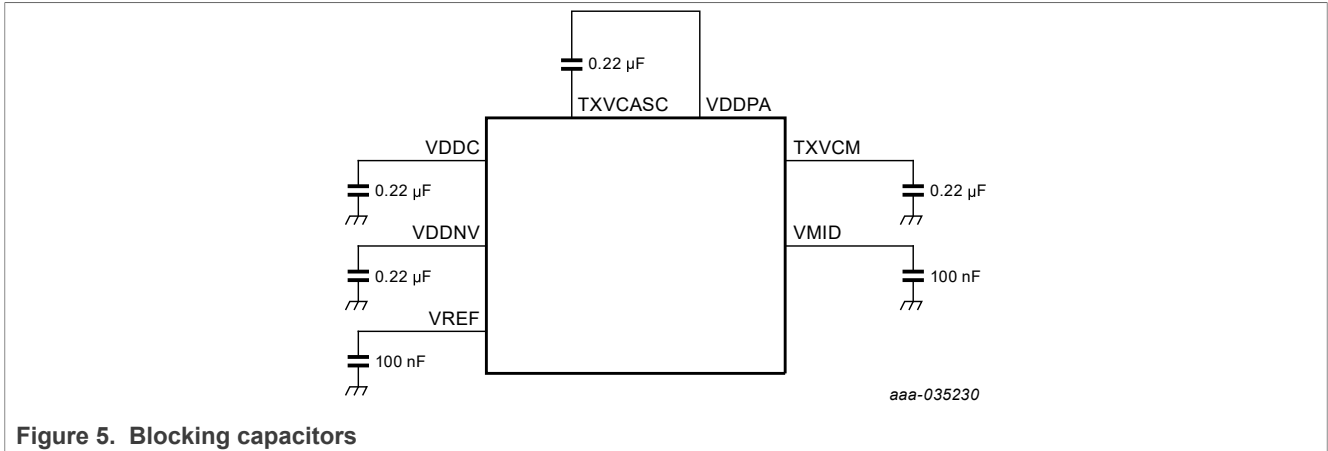


Figure 5. Blocking capacitors

### 9.5.3 Transmitter power supply

The PN5190B1 is configured by EEPROM for the different power supply options.

The following EEPROM Addresses are used to configure the power supply of the transmitter:

DCDC\_PWR\_CONFIG (0000h) - Enables/disables and configures the DC-DC according to the external supply connections.

TX\_LDO\_CONFIG (address 0002h) - Enables/disables and configures the TX\_LDO.

TX\_LDO\_VDDPA\_HIGH (address 0006h) - initial out voltage when DPC is used.

TX\_LDO\_VDDPA\_LOW (address 0007h) - lowest VDDPA when DPC is used.

TX\_LDO\_VDDPA\_MAX\_RDR (address 0008h) - maximum voltage to be set in reader mode used by DPC.

TX\_LDO\_VDDPA\_MAX\_CARD (address 0009h) - VDDPA maximum voltage to be set in card mode used by DPC.

No specific registers are required to configure the pad supply (VDDIO) or the supply for the analog and digital blocks (VUP).

#### 9.5.3.1 TX\_LDO transmitter supply

TX\_LDO supplied VDDPA configuration: The TX power amplifier is supplied by the internal voltage regulator (TX\_LDO).

In this configuration the DPC, current measurement and overcurrent protection is available. In addition, the TX\_LDO is adding an improved rejection of noise on the supply lines.

A decoupling cap is required on VDDPA pin.

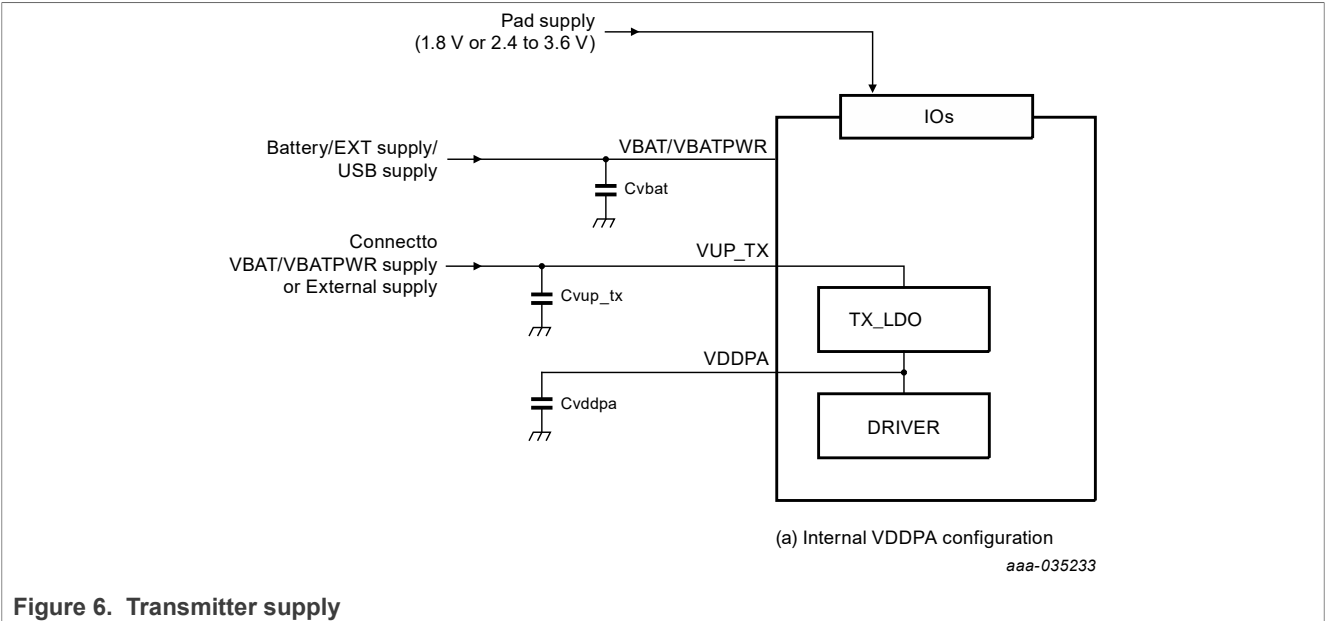


Figure 6. Transmitter supply

### 9.5.3.2 Direct transmitter supply

Direct VDDPA configuration:

TX\_LDO must be configured OFF by SW configuration. VUP\_TX and VDDPA connected to VBAT/VBATPWR.

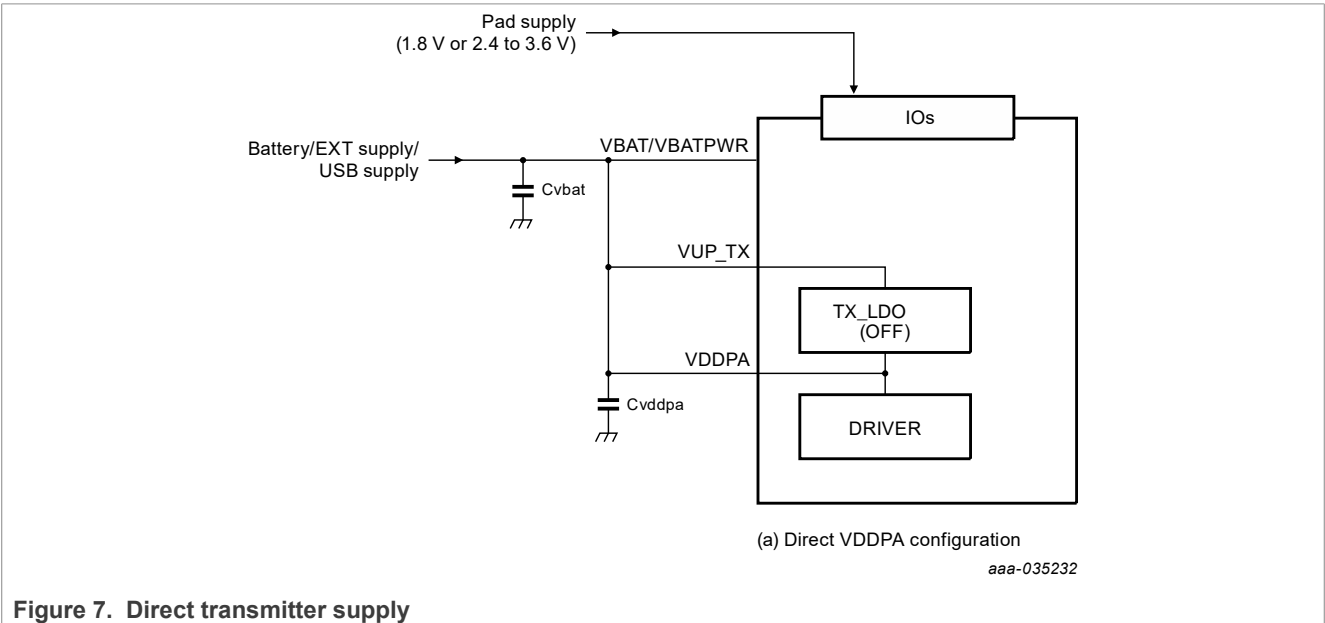


Figure 7. Direct transmitter supply

9.5.3.3 DC-DC (boost) supply

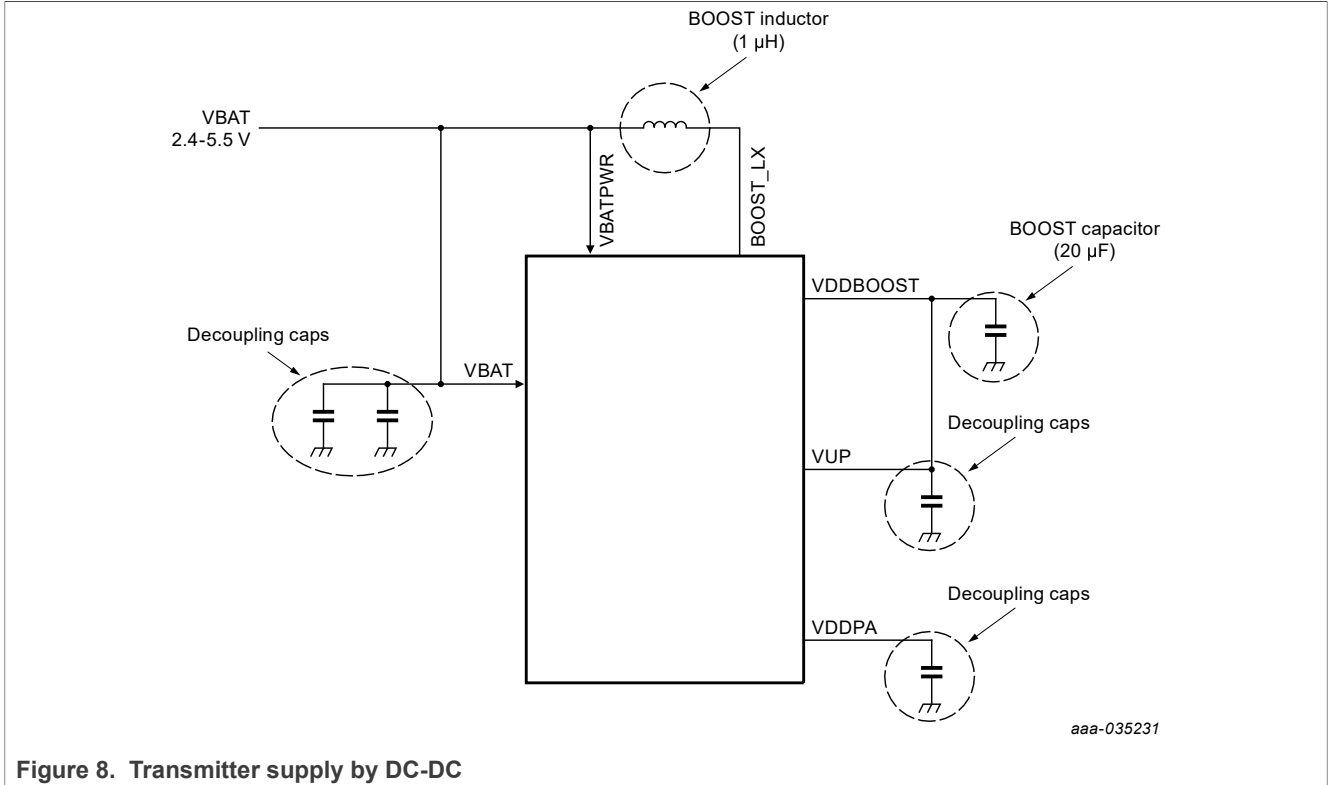


Figure 8. Transmitter supply by DC-DC

9.5.3.4 Configuration example 1: TX\_LDO transmitter supply - DC-DC active

VBAT is connected to VBATPWR.

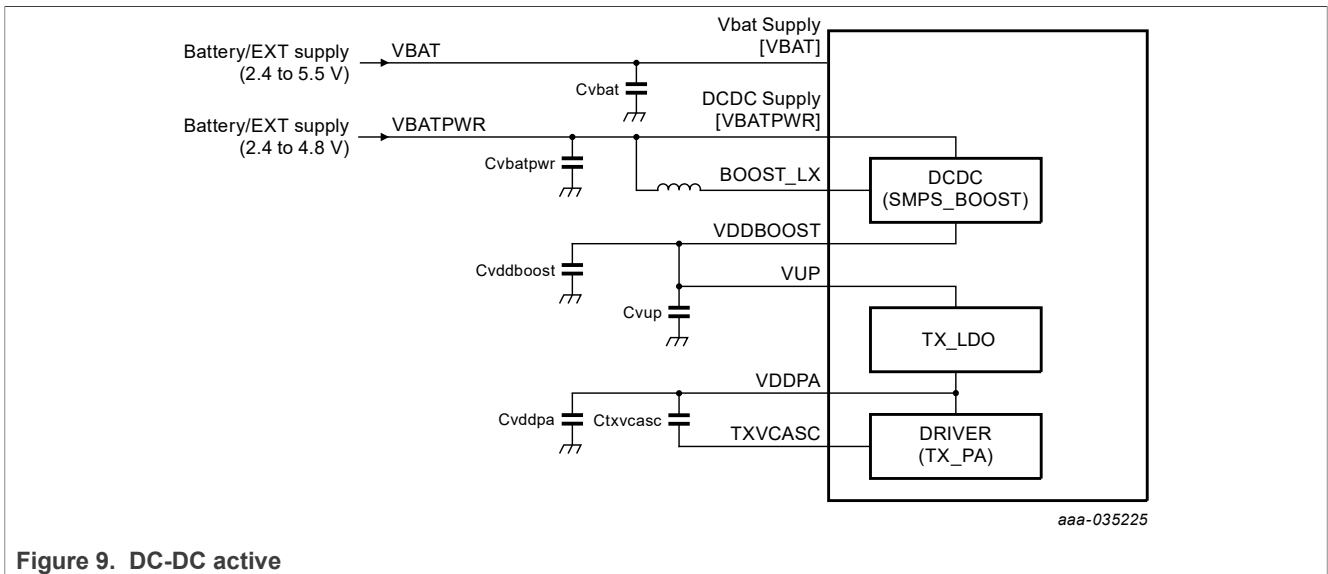


Figure 9. DC-DC active

9.5.3.5 Configuration example 2: TX\_LDO transmitter supply - DC-DC bypassed

VBAT is connected to VBATPWR.

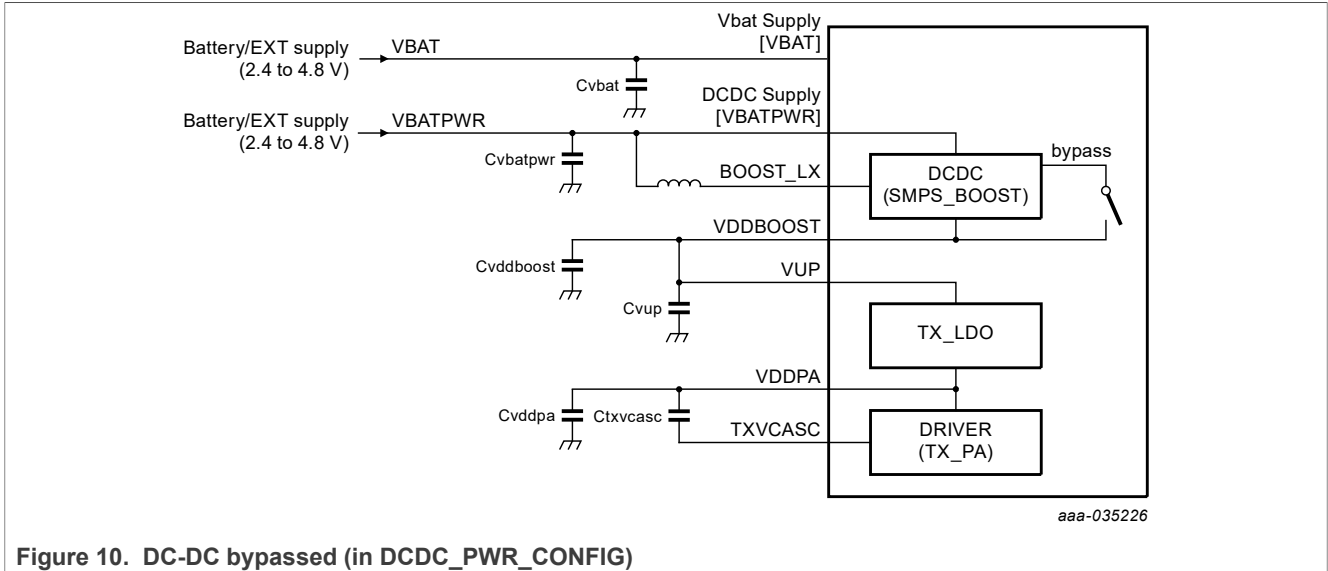


Figure 10. DC-DC bypassed (in DCDC\_PWR\_CONFIG)

9.5.3.6 Configuration example 3: TX\_LDO transmitter supply connected to VBAT - no DC-DC

VBAT is connected to VBATPWR.

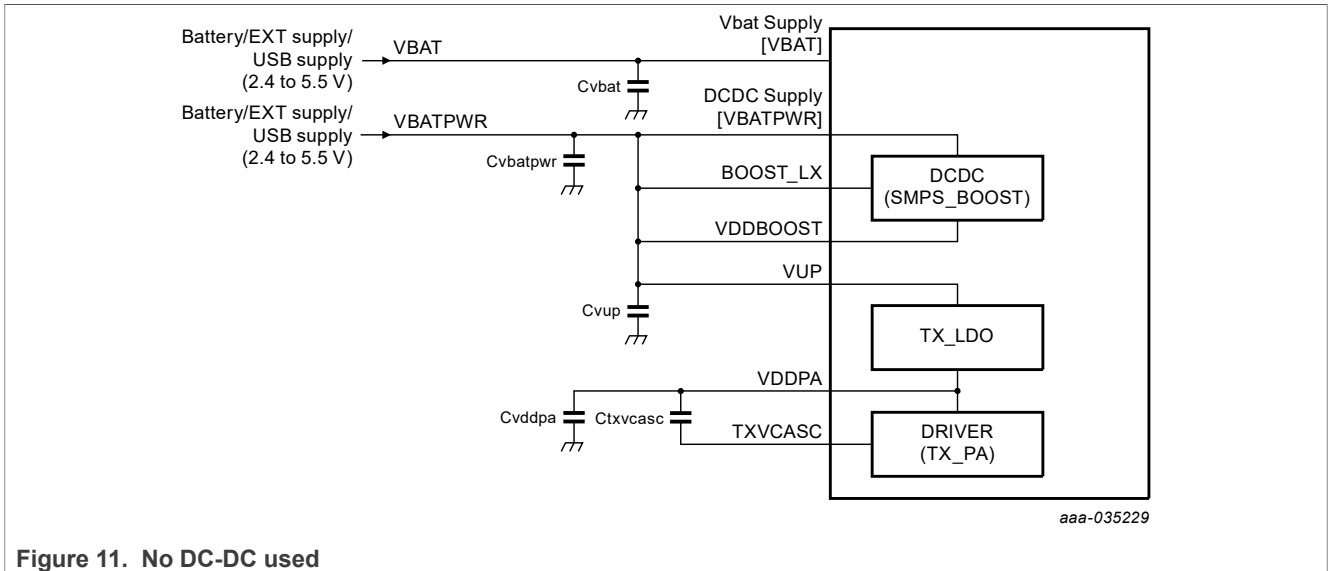


Figure 11. No DC-DC used



9.5.3.7 Configuration example 4: TX\_LDO supplied independent from VBAT - no DC-DC

VBAT is connected to VBATPWR.

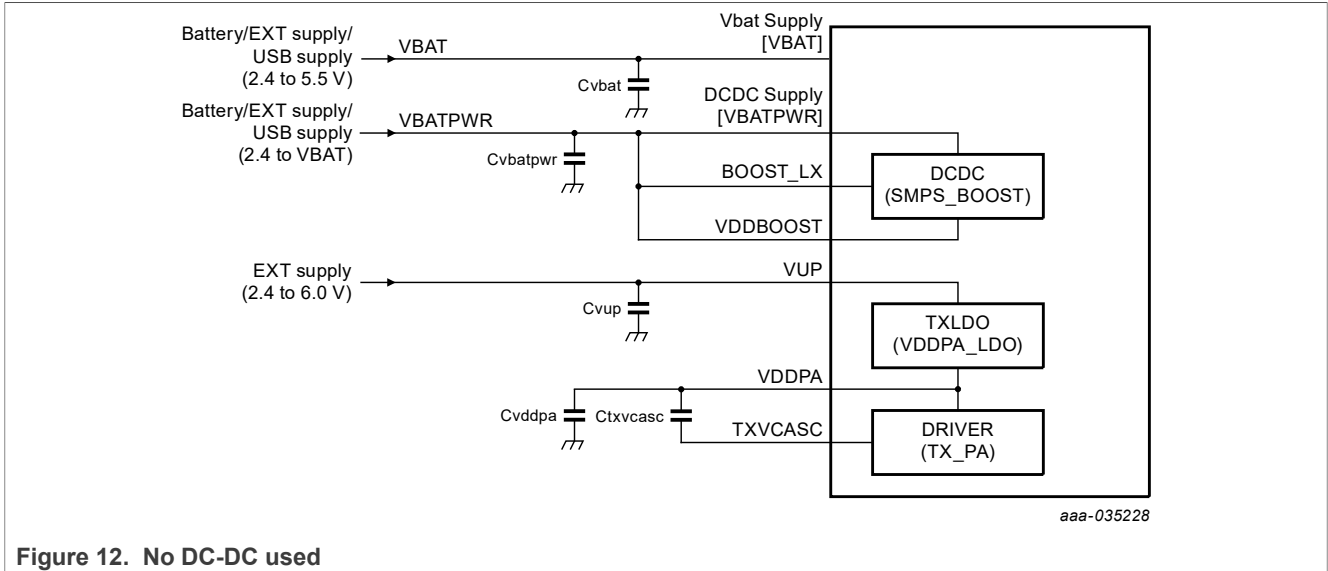


Figure 12. No DC-DC used

9.5.3.8 Configuration example 5: TX\_LDO not used - no DC-DC

VBAT is connected to VBATPWR.

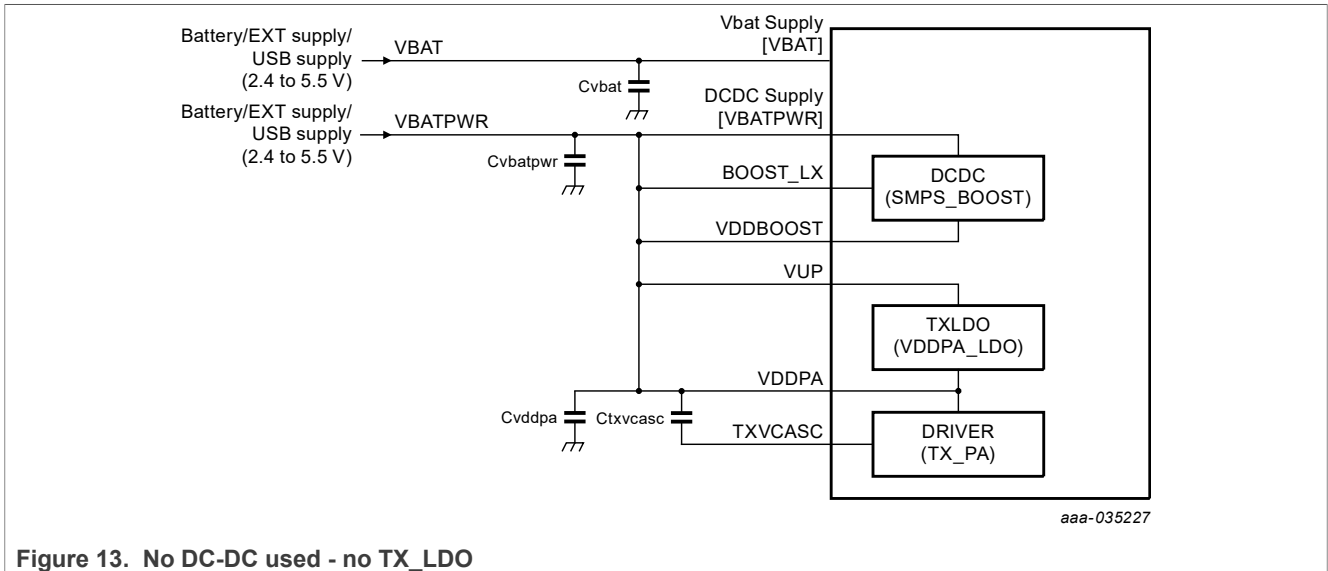


Figure 13. No DC-DC used - no TX\_LDO

## 9.5.3.9 Supply voltage range for transmitter supply configuration examples

Table 5. Supply voltage range configuration

| Supply  | Config1:<br>TX_LDO transmitter<br>supply<br>DC-DC active        | Config2:<br>TX_LDO<br>transmitter supply<br>DC-DC bypassed | Config3:<br>TX_LDO<br>transmitter<br>supply connected<br>to VBAT<br>no DC-DC | Config4:<br>TX_LDO supplied<br>independently<br>from VBAT<br>no DC-DC | Config5:<br>TX_LDO not used<br>no DC-DC |
|---|---|--|--|---|---|
| EEPROM configuration for DPC ENABLED - configured in DPC_CONFIG (address 0076h) |   |  |  |   |   |
| DCDC_PWR_CONFIG (address 0000h)   | - 0xE4(Variable BOOST with Auto Bypass).<br>- 0xE2(Fixed BOOST) | 0xE4 (Variable BOOST with Auto Bypass)                     | 0x21   | 0x21  | NA                                      |
| TXLDO_VDDPA_HIGH (0x06)   | 0x0 (1.5 V)   | 0x0 (1.5 V)  | 0x0 (1.5 V)  | 0x0 (1.5 V)   | NA                                      |
| TXLDO_VDDPA_MAX_RDR (0008h)   | 0x2A (5.7 V)  | 0x1C (4.3 V)   | 0x25 (5.2 V)   | 0x2A (5.7 V)  | NA                                      |
| BOOST_DEFAULT_VOLTAGE (000Ah)   | 0x1D (6 V).   | NA   | NA   | NA  | NA                                      |
| EEPROM configuration - DPC DISABLED - configured in DPC_CONFIG (address 0076h)  |   |  |  |   |   |
| DCDC_PWR_CONFIG (address 0000h)   | - 0xE4(Variable BOOST with Auto Bypass).<br>- 0xE2(Fixed BOOST) | 0xE4 (Variable BOOST with Auto Bypass)                     | 0x01   | 0x01  | 0x00                                    |
| TXLDO_VDDPA_HIGH (0x06)   | 0x0 (1.5 V)   | 0x0 (1.5 V)  | 0x0 (1.5 V)  | 0x0 (1.5 V)   | 0x0 (1.5 V)                             |
| TXLDO_VDDPA_MAX_RDR (0008h)   | NA  | NA   | NA   | NA  | NA                                      |
| BOOST_DEFAULT_VOLTAGE (000Ah)   | 0x1D (6 V).   | NA   | NA   | NA  | NA                                      |

Table 6. Supply voltage range

| Supply  | Config1:<br>TX_LDO transmitter supply<br>DC-DC active | Config2:<br>TX_LDO transmitter supply<br>DC-DC bypassed | Config3:<br>TX_LDO transmitter supply connected to VBAT<br>no DC-DC | Config4:<br>TX_LDO supplied independently from VBAT<br>no DC-DC | Config5:<br>TX_LDO not used<br>no DC-DC |
|---------|---|---|---|---|---|
| VBAT    | 2.8 V ... 5.5 V                                       | 2.8 V ... 4.8 V   | 2.4 V ... 5.5 V   | 2.4 V ... 5.5 V   | 2.4 V ... 5.5 V                         |
| VBATPWR | 2.8 V ... 4.8 V                                       | 2.8 V ... 4.8 V   | 2.4 V ... 5.5 V   | 2.4 V ... 5.5 V   | 2.4 V ... 5.5 V                         |
| VUP     | 3.1 V ... 6.0 V                                       | 2.8 V ... < VBATPWR                                     | 2.4 V ... 5.5 V   | 2.4 V ... 6.0 V   | 2.4 V ... 5.5 V                         |
| VDDPA   | VUP-0.3V drop of TX_LDO. max 5.7 V                    | VBATPWR - 0.5 V voltage drop                            | VUP-0.3V drop of TX_LDO   | VUP-0.3V drop of TX_LDO   | 2.4 V ... 5.5 V                         |

### 9.6 Clock generation

The device supports the operation with two clock options, which is configured in EEPROM address CLK\_INPUT\_FREQ (0012h).

One option is clocking by a crystal (default), the other a clocking by an external clock input frequency.

It is important to consider additional phase noise introduced e.g. by clock drivers in the design. Phase noise of the external clock has an impact on the RF performance which can be achieved.

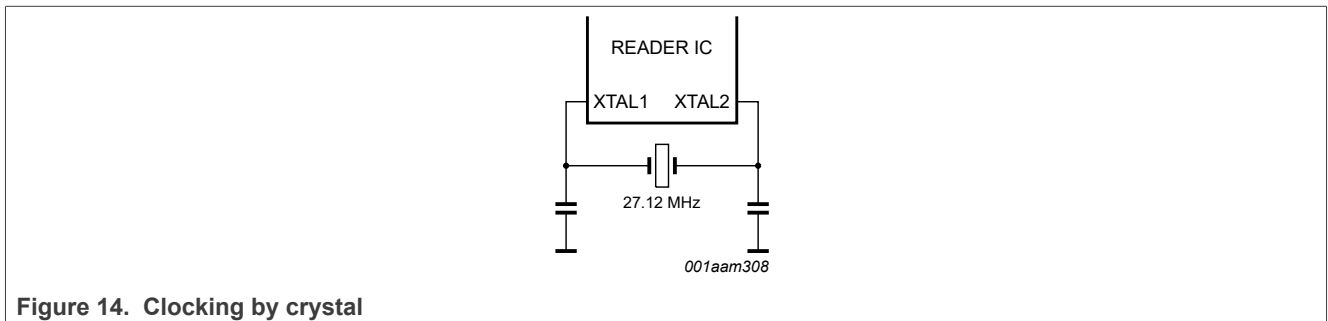


Figure 14. Clocking by crystal

### 9.7 External interfaces

The PN5190B1 requires the connection of a power supply, and a clock source like crystal or external clock and a host microcontroller connected by the SPI interface for operation.

Additional connections of the package require the connection of stabilizing capacitors and ground.

The RF interface connects transmitter and receiver to the EMC filter of a connected antenna matching network. Additional connections are available for the GPIO's (on PN5190B1 only outputs are implemented) and 2x DAC functionality (analog outputs).

The GPIO's implement internal Pull-up/Pull-down resistors. The output of the GPIO's can be configured in the pad configuration PAD\_CONFIG (0052h).

For more information, see [2].

### 9.8 Transmitter overcurrent and temperature protection <sup>2</sup>

The PN5190B1 implements different mechanisms to protect the chip against damage.

On the one hand, an overcurrent protection exists which shuts down the Transmitter Driver in case of a out of spec current. This can be enabled in EEPROM TXLDO\_CONFIG (0002h), bit 11: overcurrent enable (0: disable, 1: enable)

On the other hand, an internal temperature sensor allows to monitor the temperature of the chip. This is configured in the EEPROM TEMP\_WARNING (0014h). Three temperatures can be configured: 114 °C, 2:125 °C, 3:130 °C. GPIO0 is used to indicate this temperature warning to a connected host.

The actual measured temperature is available in the register TEMP\_SENSOR (005Bh).

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

### 9.9 Loading a dedicated RF configuration

The PN5190B1 allows an efficient selection of a dedicated RF protocol.

The selection of one RF protocol is done by sending a command to the PN5190B1. This instruction is used to load the RF configuration from EEPROM into registers.

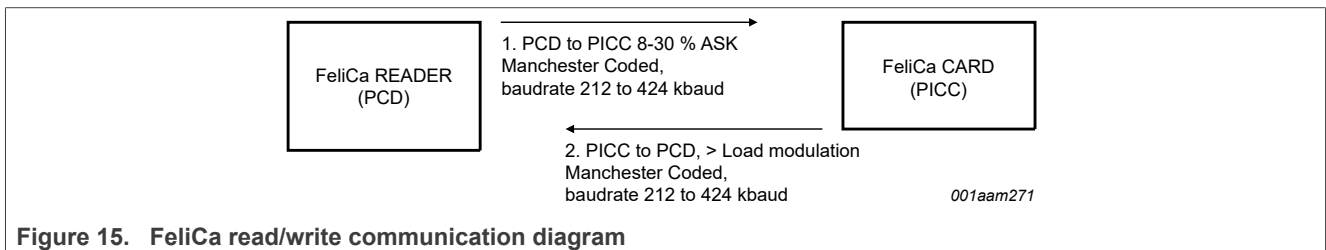
It is possible to configure RF technology, mode (target/initiator) and baud rate.

Configurations can be loaded separately for the receiver (RX configuration) and transmitter (TX configuration).

The Command used for loading a dedicated RF protocol is LOAD\_RF\_CONFIGURATION (0Dh).

### 9.10 FeliCa RF functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification.



The physical parameters are described in the table below:

Table 7. Communication for FeliCa reader/writer

| Communication direction  | Signal type            | Transfer speed FeliCa | FeliCa higher transfer speeds |
|--|------------------------|-----------------------|-------------------------------|
|  |                        | 212 kbit/s            | 424 kbit/s                    |
| Reader to card (send data from the PN5190B1 to a card) $f_c = 13.56$ MHz | reader side modulation | 8 % to 30 % ASK       | 8 % to 30 % ASK               |
|  | bit encoding           | Manchester encoding   | Manchester encoding           |

<sup>2</sup> Refer to the errata sheet

Table 7. Communication for FeliCa reader/writer...continued

| Communication direction                              | Signal type          | Transfer speed FeliCa | FeliCa higher transfer speeds |
|--|----------------------|-----------------------|-------------------------------|
|  |                      | 212 kbit/s            | 424 kbit/s                    |
|  | bit rate             | $f_c/64$              | $f_c/32$                      |
| Card to reader ( PN5190B1 receives data from a card) | card side modulation | Load modulation,      | Load modulation,              |
|  | bit encoding         | Manchester encoding   | Manchester encoding           |

The PN5190B1 needs to be connected to a host which implements the FeliCa protocol.

**Multiple reception cycles (RxMultiple)**

For FeliCa timeslot handling in PCD mode, PN5190B1 implements multiple reception cycles. The feature is enabled by setting the control bit RX\_MULTIPLE\_ENABLE in the register TRANSCEIVE\_CONTROL in combination with the transceive state machine.

Unlike for normal operation, the receiver is enabled again after a reception is finished. As there is only one receive buffer available, but several responses are expected, the buffer is split into sub buffers of 32 byte length. Hence, the maximum number of responses which can be handled is limited to 8. As the maximum length defined for a FeliCa response is 20 bytes, the buffer size defined does fulfill the requirements for that use case. The first data frame received is copied onto buffer address 0. The subsequent frames are copied to the buffer address 32 \* NumberOfReceivedFrames. The maximum number of data bytes allowed per frame is limited to 28.

All bytes in the buffer between the payload and the status byte are uninitialized and therefore invalid. The firmware on the host shall not use these bytes. The last word of the sub buffer (position 28 to 31) contains a status word. The status word contains the number of received bytes (may vary from the FeliCa length in case of an error), the CLError flag indicating any error in the reception (which is a combination of 3 individual error flags DATA\_INTEGRITY\_ERROR || PROTOCOL\_ERROR || COLLISION\_DETECTED) the individual error flags and the LenError flag indicating an incorrect length byte (either length byte is greater than 28 or the number of received bytes is shorter than indicated by the length byte). All unused bits (RFU) are masked to 0.

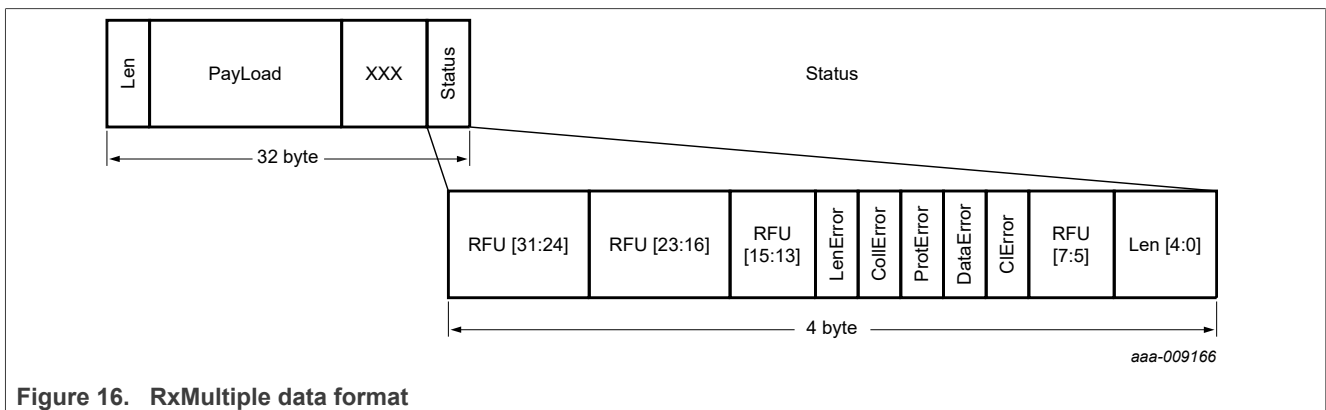


Figure 16. RxMultiple data format

There are 4 different cases possible for a reception:

1. *Correct reception* - Data integrity is correct (no CRC error), and additionally the number of bytes received is equal to the length byte. Data is written to the buffer. No error set in status byte.
2. *Erroneous reception* - Data is incorrect (data integrity error - CRC wrong) but frame length is correct. Data is written to buffer and the bits CLError and DataError in the status byte are set.

3. *Erroneous reception* - the length byte received indicates a frame length greater than 28. Data is written to buffer and the bit LenError in status byte is set.
4. *Erroneous reception* - the length byte is larger than the number of data bytes, which have been received. Data received is written to buffer and the ProtocolError bit in the status byte is set.

At the end of the reception, additionally the bit field RX\_NUM\_FRAMES\_RECEIVED in the register RX\_STATUS\_REG is updated to indicate the number of received frames. Upon start of a new EXCHANGE\_RF\_DATA command, the flag RX\_NUM\_FRAMES\_RECEIVED is cleared.

## 9.11 Dynamic power control (DPC)

The DPC is used for a special antenna tuning, called "symmetric antenna tuning". For an "asymmetric antenna tuning", the DPC is not required.

However, even for "asymmetric antenna tuning" with high output power needs, it might turn out that the RF field is too strong in close proximity of the antenna to be compliant with ISO/IEC14443 requirements. In this case, the DPC can be used as well to reduce the RF output power dependent on the distance of the card from the reader antenna.

The DPC works very well with a tuning called "symmetric tuning". With symmetric tuning, a detuning of the antenna is causing a reduction of the antenna impedance. This low antenna impedance might lead to a current which is too high for the targeted application. The DPC allows to limit the transmitter current even under antenna detuning conditions.

DPC is useful:

- To achieve NFC Forum and ISO/IEC 14443 compliancy (e.g. NFC Forum Power Transfer Maximum, ISO/IEC 14443 Field Emission Maximum)
- To improve interoperability

The Dynamic Power Control (DPC 2.0) allows controlling the transmitter driver voltage in 100 mV steps dependent on the actual transmitter current.

A lookup table is used to configure the transmitter output voltage and by this control the RF output power.

Features of the Dynamic power control (DPC 2.0):

- True current measurement provides maximum information for the regulation loop
- The transmitter current can be limited and additionally reduced according to detected transmitter current condition / antenna detuning condition
- DPC works autonomously without host interaction causing no additional processing load on the host
- Fastest response time of 1 ms for regulation
- Used for adaptive waveshape control (AWC)
- Used for adaptive RX sensitivity control (ARC)

The DPC is able to operate in two modes:

1. Current limiting mode
2. Current limiting + Current reduction mode

The DPC is configured in the EEPROM, this configuration is used after startup. This avoids that the host needs to configure the chip after each reset or power-off.

The following EEPROM registers are most relevant for the DPC configuration:

**0xF8: DPC\_Config:** Enables/Disables the DPC (enable: 0x39, disable: 0x00)

**0xF9: DPC\_TargetCurrent:** Unloaded VDDPA target current in mA, the target current +/- Hysteresis is limiting the current for the DPC.

- The DPC\_TargetCurrent is the current which can be measured for the selected antenna impedance and transmitter supply voltage in unloaded condition. This is the current the system is designed to operate at.

**0xFB: DPC\_Hysteresis:** Absolute difference to current target current in mA that triggers a DPC update event.

- The configuration of the hysteresis ensures, that the DPC is not regulating if small changes of the transmitter current occur due to external disturbances. A typical value for the DPC\_Hysteresis is e.g. 20 mA.

**0x8B: DPC\_Lookup\_Table:** configures the current reduction

The DPC\_LOOKUP\_TABLE allows in addition to the limitation of the current, to configure

- an additional current reduction on top of the current limitation, achieved by further lowering the transmitter supply voltage
- a relative change of modulated amplitude level
- and a relative change of falling and raising edge time constant for ASK10% and ASK100% modulations

This lookup table is initialized with 0x00 for devices delivered from the factory. (The customer development board is already initialized with useful data in EEPROM which work well with the antenna of the board).

The 0x00 entry in the DPC\_LOOKUP\_TABLE means that no additional function then the current limitation takes place for the DPC.

In order to achieve a limitation of the current even in the case of an antenna impedance that is lowered, the Transmitter supply voltage is reduced accordingly.

This transmitter supply voltage reduction is now used as index for the DPC\_LOOKUP\_TABLE.

For a specific transmitter supply voltage, it is possible to further reduce the current below the value of DPC\_TargetCurrent or to configure parameters for waveshaping and modulation. All these entries are relative values, granularity of the entries dependent on the transmitter supply voltage is 0.1 V, resulting in 42 table entries.

The DPC updates the content of the following register dependent on the antenna load / lookup table configuration:

0x30 - DGRM\_RSSI

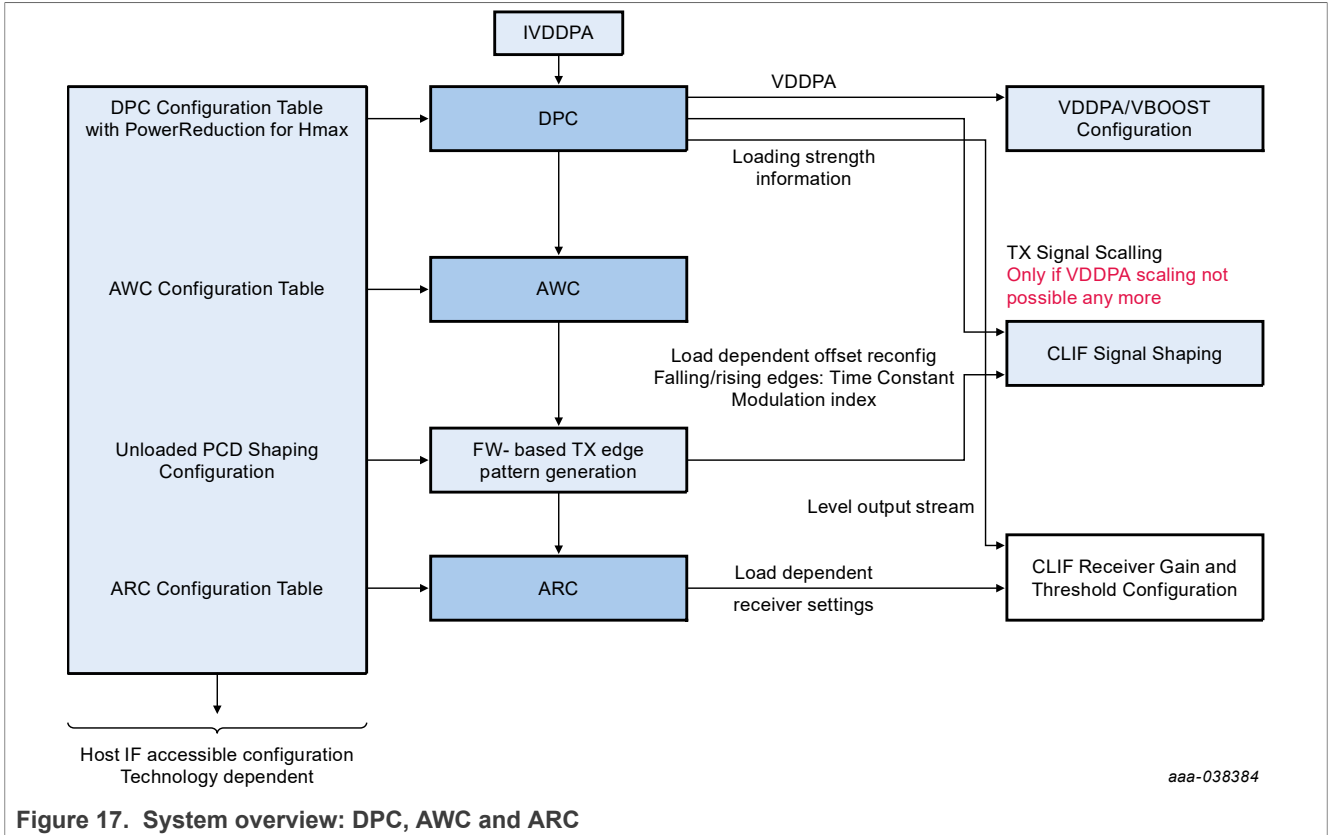


Figure 17. System overview: DPC, AWC and ARC



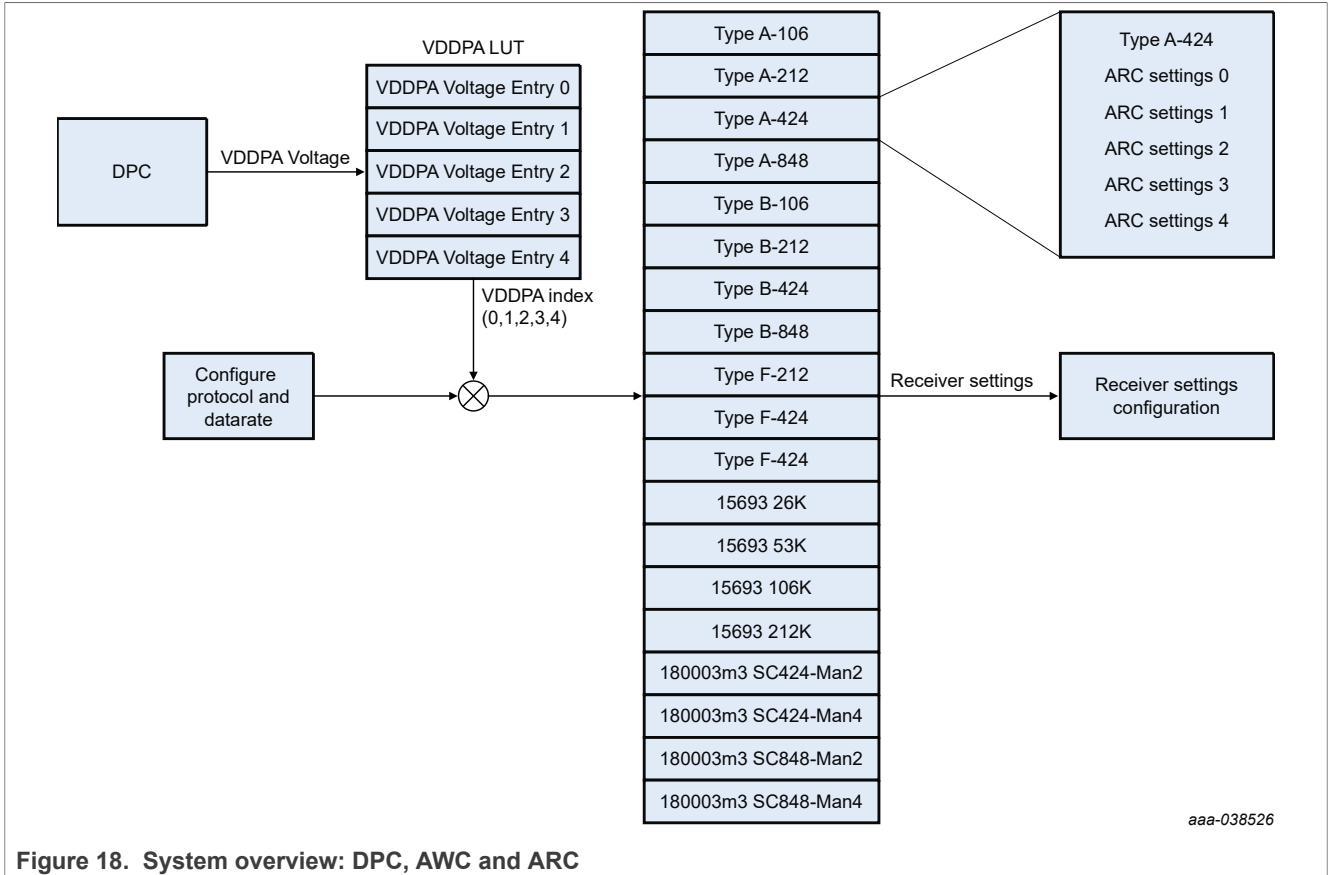


Figure 18. System overview: DPC, AWC and ARC

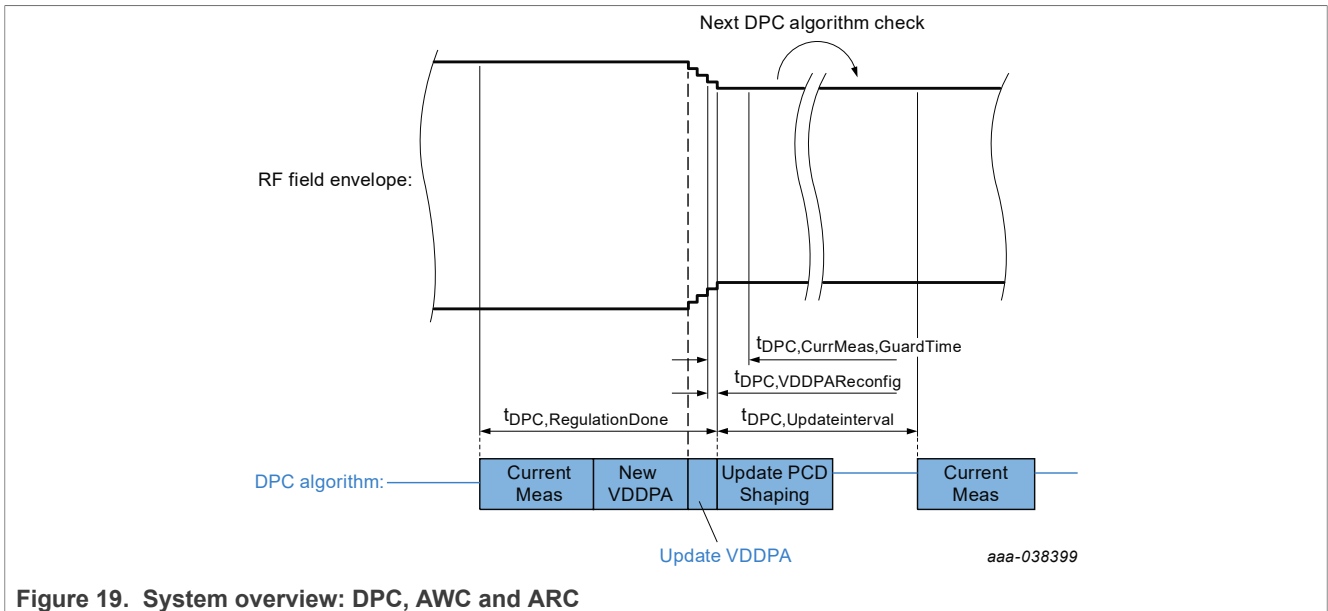


Figure 19. System overview: DPC, AWC and ARC

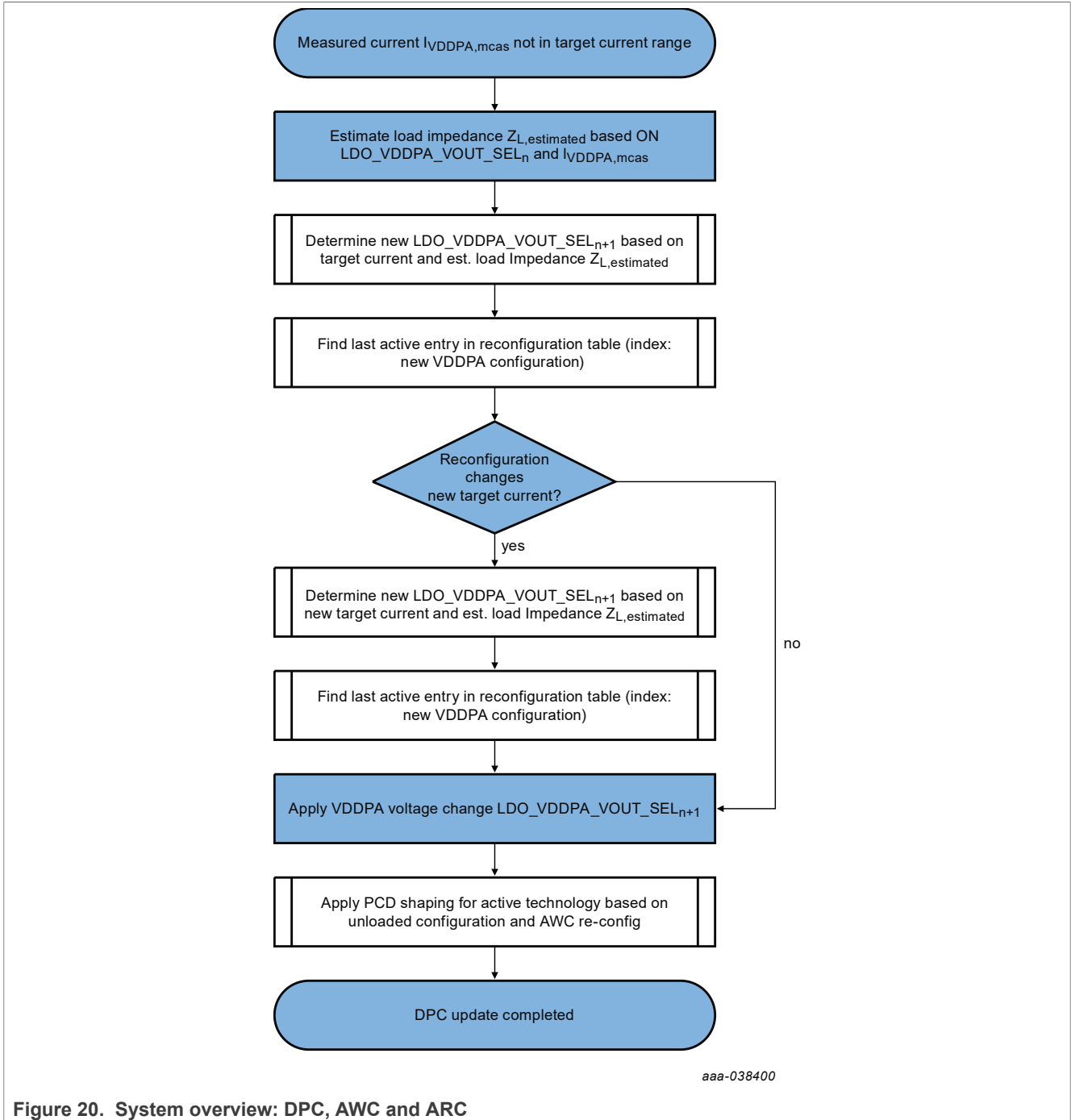


Figure 20. System overview: DPC, AWC and ARC

9.11.1 DPC algorithm

The DPC algorithm is controlling the transmitter current. It is using the following states:

1. Current measurement: Performs VDDPA current measurement
2. New VDDPA: Determine new VDDPA configuration based on measured current  
 $VDDPA_{New} \text{ (for target current of } I_{target}) = VDDPA_{Voltage} / VDDPA_{current} * I_{target}$
3. Update VDDPA: Perform output power update
4. Update PCD Shaping: Apply AWC configuration updates for active technology
5. Update RX sensitivity parameter only for short duration

Reconfiguration table includes Relative changes of target current and of waveform parameters adaption for all VDDPA voltage configurations. The VDDPA configuration is implicitly defined by the row index. The first row refers to LDO\_VDDPA\_VOUT\_SEL=0 (represents 1V5).

EXAMPLE:

Unloaded configuration After Field ON:

VDDPA max set to 42 (5.7 V) · Target current set to 280 mA

Technology B106: amp\_mod=200

Falling edge time constant=rising edge time constant=3

Table 8. DPC\_LOOKUP\_TABLE element, defining the configuration for one dedicated VDDPA voltage

| Function                                 | Bit   | Description  |
|--|-------|--|
| ENTRY 0                                  | 31:0  | This is the entry for 1.5 V.   |
| Target current reduction                 | 31:23 | ENTRY 0 -LSB - byte 0<br>Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V<br>bEntry_00 = 1V5 ... bEntry_42 = 5V7<br>Bits[7:0] = Target current reduction in mA (unsigned) |
| AWC amp mod change                       | 23:16 | ENTRY 0 - byte 1<br>Bits[7:0] = Relative change of modulated amplitude level (signed)  |
| AWC edge time constant for ASK100        | 15:8  | ENTRY 0 - byte 2<br>Bits[3:0] = ASK100, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)                      |
| AWC falling edge time constant for ASK10 | 7:0   | ENTRY 0 -MSB - byte 4<br>Bits[3:0] = ASK10, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)                   |

Loaded configuration After Field ON:

DPC regulates from unloaded VDDPA configuration 42 to 31. Consequently, new configuration to be applied based on index entry 31.

Target current stays at 280 mA.

Technology B106: amp\_mod=205, falling edge time constant=2, rising edge time constant=0

9.12 Adaptive waveshape control (AWC)

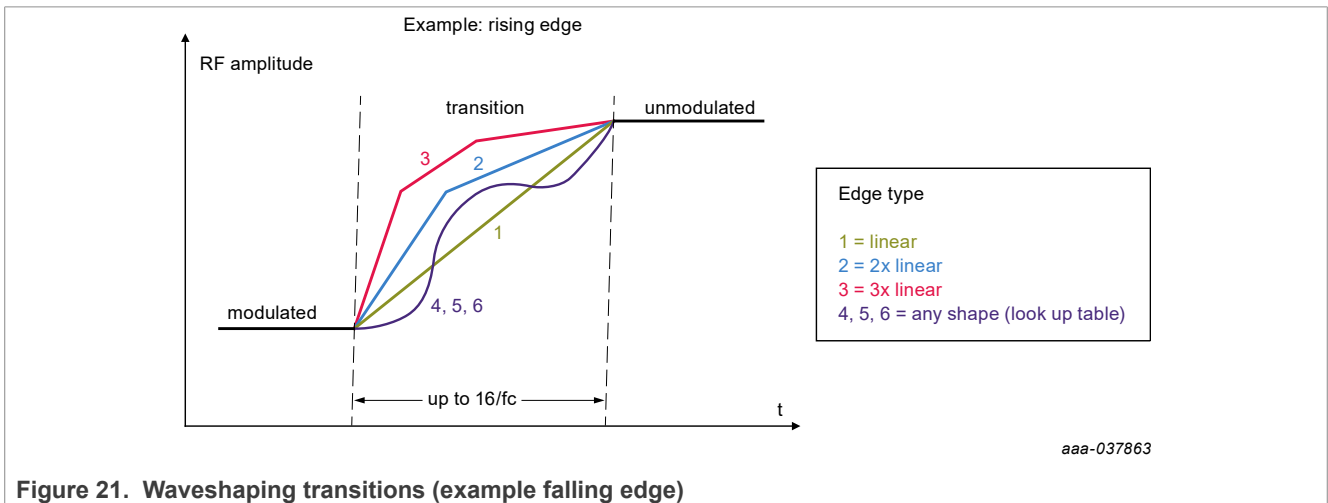
Depending on the level of detected detuning of the antenna, wave shaping related register settings can be automatically updated.

Two different waveshaping mechanisms can be used:

1. Firmware based shaping (1,2,3)
2. Lookup table based shaping (4,5,6)

The Firmware based shaping allows to correct rise times and overshoot with linear transition shapes.

The lookup table based shaping allows maximum flexibility and enables to configure almost any possible correction.



The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual detected detuning condition.

Each lookup table entry allows the configuration not only of a dedicated wave shaping configuration for the corresponding detuning condition. But allows in addition to configure the wave shaping individually dependent on the actual protocol which is active.

Features of the Adaptive Waveshape Control:

- No external components required
- No need to compromise antenna matching to meet waveshape requirements
- Waveshapes automatically adapted according to detected detuning condition
- RF standards define envelope timing and residual carrier parameters required for compliance and interoperability.

The device supports the design of compliant antennas by allowing to actively shaping the style of edge transition for falling and rising edges. The shaping of modulation edges is achieved by selecting one from three edge transition styles:

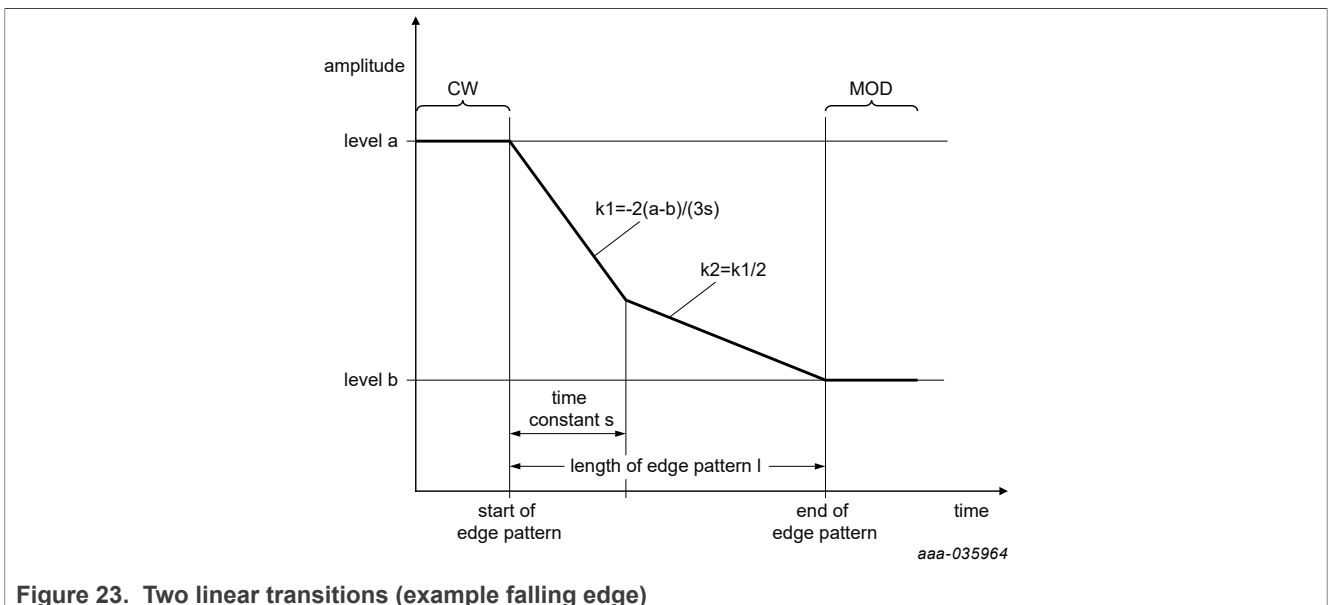
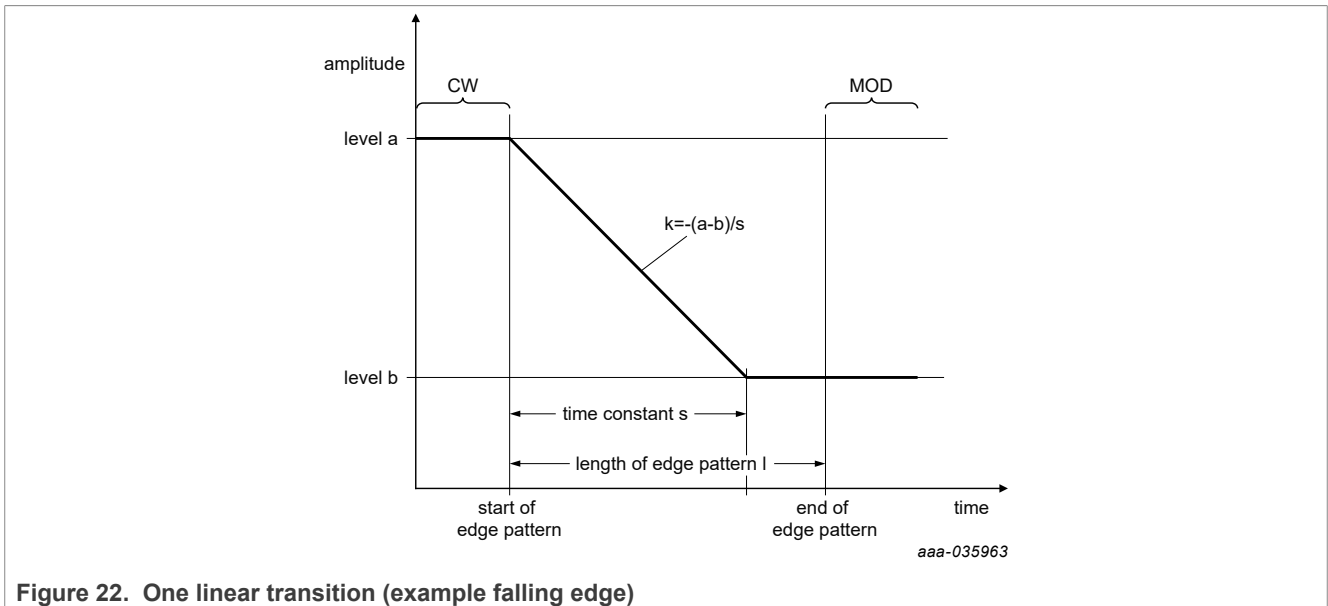
1. Linear transition between two amplitude levels
2. Two linear transition's between amplitude levels and
3. Three linear transitions between amplitude levels.

The type of the transition is selected in the EEPROM registers EDGE\_TYPE\_(protocol), and can be defined independent for each RF protocol and data rate - for both falling and rising edge.

The EEPROM registers EDGE\_STYLE\_(protocol) define the time constant "s" of falling/rising edge (depends on edge style).

The EEPROM registers EDGE\_LENGTH\_(protocol) define the total length of the edge pattern.

The figures below illustrate the edge type for the falling edge.



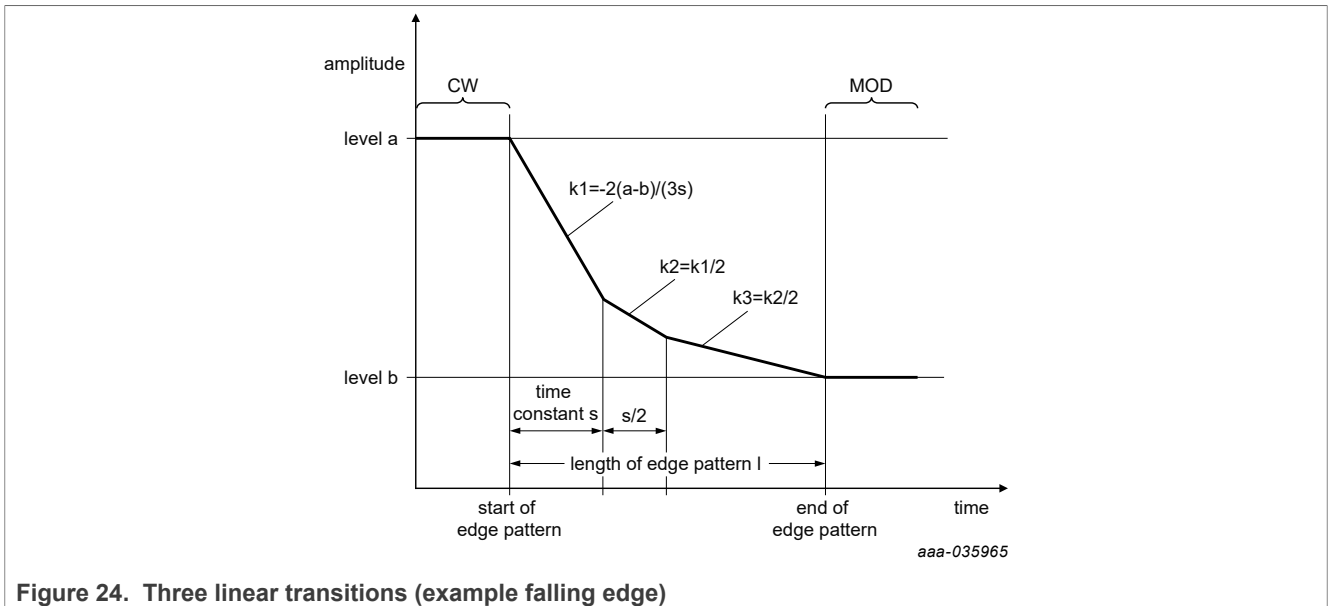


Figure 24. Three linear transitions (example falling edge)

The transition patterns are used as implicit pre-distortion to compensate effects of TX loading circuitry (e.g. resonant circuitry parameters) to the emitted RF envelope.

### 9.13 Adaptive receiver control (ARC)

Depending on the level of detected antenna detuning, receiver-related register settings can be automatically updated. The receiver-related registers which are allowed to be dynamically controlled are:

DGRM\_RSSI\_REG (30h) ->DGRM\_SIGNAL\_DETECT\_TH\_OVR\_VAL

SIGPRO\_RM\_Tech\_REG (22h) ->RM\_MF\_GAIN,

The adaptive receiver control settings override the default RM\_MF\_GAIN and DGRM\_SIGNAL\_DETECT\_TH\_OVR\_VAL settings configured by the command LOAD\_RF\_CONFIGURATION (0Dh).

The ARC algorithm is called when VDDPA voltage changes after DPC. There are two lookup tables used in ARC algorithm i.e VDDPA lookup and ARC lookup. In case of a VDDPA change, an EEPROM lookup (at current protocol and baud rate) is performed. The receiver-related settings i.e RM\_MF\_GAIN, DGRM\_SIGNAL\_DETECT\_TH\_OVR\_VAL and IIR\_ENABLE are read from EEPROM lookup table and configured in registers.

#### VDDPA lookup table:

VDDPA lookup table define maximum five voltage ranges. Number of VDDPA voltage ranges used in ARC algorithm is configured in bArcConfig[2:0]. VDDPA voltage output from DPC algorithm is input to VDDPA lookup. VDDPA lookup returns VDDPA\_range\_index (i.e 0,1,2,3,4).

Table 9. ARC\_VDDPA (0139Eh) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description  |
|---------------|-------------------|-----|--|
| 13D           | ARC VDDPA Setting | 7:0 | Byte[4] = ARC_VDDPA_0: ARC_VDDPA_3 > VDDPA < ARC_VDDPA_4 |

Table 9. ARC\_VDDPA (0139Eh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
| 13C           |          | 7:0 | Byte[3] = ARC_VDDPA_0: ARC_VDDPA_2 > VDDPA < ARC_VDDPA_3 |
| 13B           |          | 7:0 | Byte[2] = ARC_VDDPA_0: ARC_VDDPA_1 > VDDPA < ARC_VDDPA_2 |
| 13A           |          | 7:0 | Byte[1] = ARC_VDDPA_0: ARC_VDDPA_0 > VDDPA < ARC_VDDPA_1 |
| 139           |          | 7:0 | Byte[0] = ARC_VDDPA_0: 1.5 > VDDPA < ARC_VDDPA_0         |

**ARC lookup table:**

VDDPA index and RF protocol/datarates are input to ARC lookup. There are five Receiver settings entries for each protocol and data rates. ARC algorithm select one out of five entries (at current protocol and baud rate) based on VDDPA\_range\_index.

Following table show ARC settings for Type A-106.

Table 10. ARC\_RM\_A106 (address 013Eh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 146           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 144           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 142           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 140           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT,   |

Table 10. ARC\_RM\_A106 (address 013Eh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 13E           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** For ISO14443-A: In case ARC is disabled, it requires DPC\_SIGNAL\_DETECT\_TH\_OVR\_VAL larger than 0x50 (with MF\_GAIN = 2 (default))

**Note:** For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC\_SIGNAL\_DETECT\_TH\_OVR\_VAL larger than 0x50 (with MF\_GAIN = 2 (default)) if the ARC is enabled.

### 9.14 Timer

The PN5190B1 implements three different types of timers: 2 general-purpose timers (only general-purpose Timer0 is accessible by the user, Timer1 is used by the PN5190B1 as FDT Timer), 1 wake-up timer and 1 low frequency timer.

#### General-purpose timer

The PN5190B1 implements two 20-bit wide general-purpose timers - Timer0 and Timer1.

Timer0 can be configured by 2 registers each (TIMER0\_CONFIG, TIMER0\_RELOAD).

Timer 1 is typically used for as FDT and EMD timer configuration. Configuration can be done from the host but the associated IRQ is handled by the firmware of the PN5190B1. The Timer1 events are consumed by the PN5190B1 FW and respective Time-out status is included as part of the command response.

The general-purpose Timer0 and the FTD Timer1 have a max count of 1.048.575.

The register TIMER0\_CONFIG, TIMER0\_RELOAD configure if either the 13.56 MHz clock of the RF interface is used as Timer input, or if a divided clock frequency is used as input. These registers configure as well the start conditions for the timer.

The following clock frequencies can be selected for the prescaler:

- 000b - 6.78 MHz counter
- 001b - 3.39 MHz counter
- 010b - 1.70 MHz counter
- 011b - 848 kHz counter



- 100b - 424 kHz counter
- 101b - 212 kHz counter
- 110b - 106 kHz counter
- 111b - 53 kHz counter

**Wake-up timer**

The PN5190B1 implements one 10-bit wide wake-up timer.

Max count of the wake-up timer is 1023, input clock is the LFO CLK = 380 kHz. The max timeout is 269 ms.

The wake-up time is configured via the SWITCH\_MODE\_STANDBY / SWITCH\_MODE\_LPCD commands. There is no dedicated register available for this timer. The PN5190B1 enters the standby state by the switch mode command SWITCH\_MODE\_STANDBY/ SWITCH\_MODE\_LPCD. The counter value is part of the command and has to be sent as one configuration parameter. The 2-byte parameter value for the standby counter is indicating the counting time in milliseconds. The value needs to be provided in little-endian format.

**Low frequency timer**

The wakeup-counter for the ULPCD mode has a width of 12bits.

The input clock for this timer is 1 kHz. ULPCD uses the ULP\_STANDBY command, and for this the wake-up timer is feed by the 1 kHz clock. Count down value (12 bits counter; ULFO CLK / 4096 = 0.244 Hz i.e. 1 ms per bit).

The max timeout is 4.096 s.

**Timer for contactless interface**

In addition to the timers above, to guarantee correct protocol timing, a guard period timer is implemented for the RF\_EXCHANGE command in reception and transmission mode (TX\_WAIT, RX\_WAIT counting).

No configuration of this timer is available for the user, setup, and counting is managed completely by the hardware. Therefore this timer is not indicated in the timer overview.

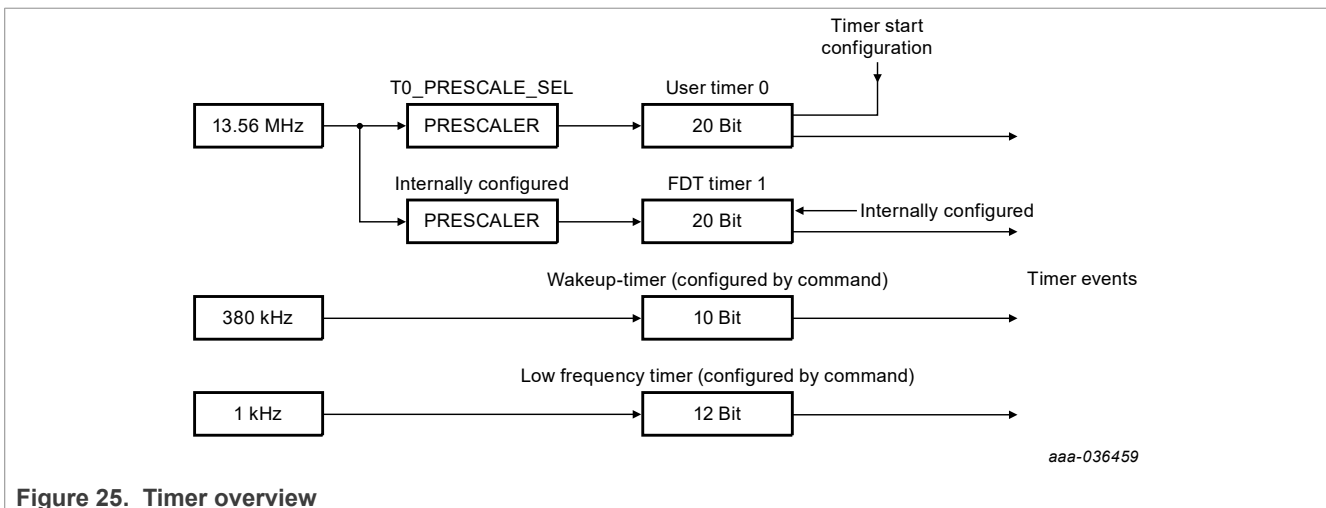


Figure 25. Timer overview

### 9.15 Energy-saving card detection

The low-power card detection (LPCD) and ultra-low power card detection (ULPCD) are an energy-saving card polling configuration for the PN5190B1. During LPCD and ULPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required.

A low frequency timer is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short pulse which allows to detect a detuning of the antenna. In case of a detected antenna detuning, the system is woken up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

There is no trimming for the Low Frequency Timer required.

The SWITCH\_MODE instruction allows entering the LPCD or ULPCD mode with a given standby duration value.

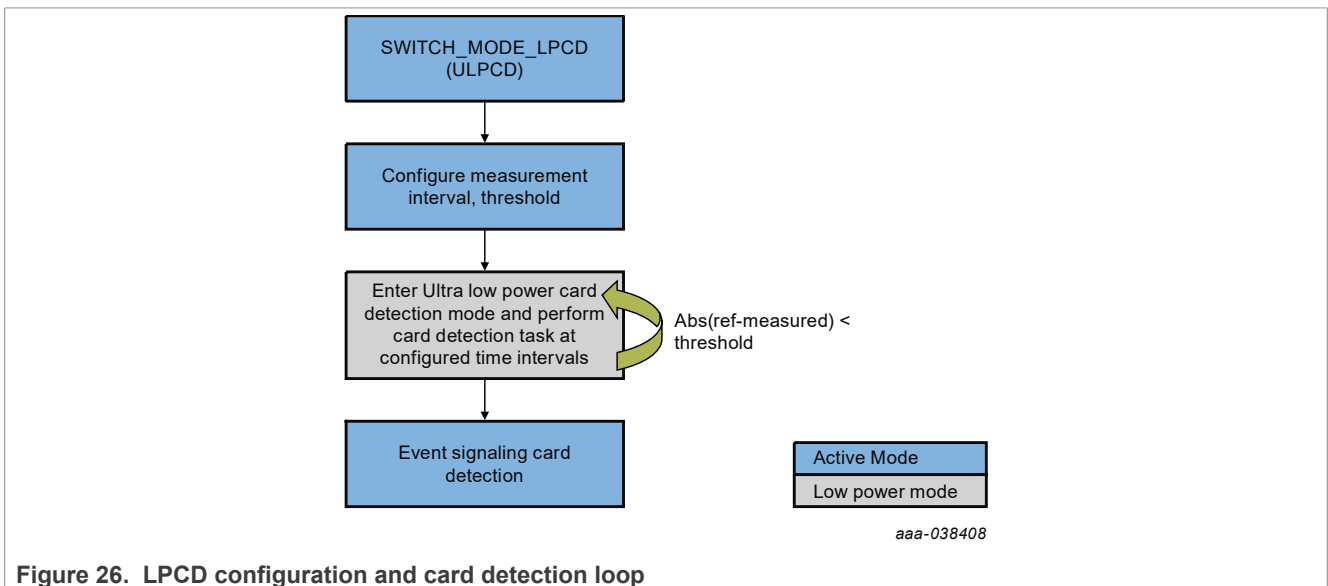


Figure 26. LPCD configuration and card detection loop

#### 9.15.1 Low-power card detection (LPCD)

The low-power card detection (LPCD) is an energy-saving card polling configuration for the PN5190B1. During LPCD, a host microcontroller can be set into power-saving mode, as no host controller interaction is required. The host microcontroller is woken up from power-saving mode by an IRQ send by the PN5190B1.

The LPCD mode offers highest sensitivity at the cost of slightly higher current consumption compared to the ULPCD mode.

A low frequency oscillator (there is no trimming for the low frequency oscillator required) is implemented to drive a wake-up counter, which triggers a periodic activation of the antenna drivers to emit a short RF pulse. This RF pulse allows to detect a detuning of the antenna by presence of conductive objects in proximity of the antenna (card, cell phone, metal).

In case of a detected antenna detuning, the system wakes up from power-saving mode. It sends an interrupt signal to the connected host microcontroller to wake up the host microcontroller from power-saving mode and to indicate a change of the antenna detuning condition.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN5190B1 from Standby mode. This allows implementation of low-power card detection polling loop at application level.

The host microcontroller can then perform a card polling sequence to verify if the technology of the object causing the antenna detuning is supported by the system.

The SWITCH\_MODE instruction allows entering the LPCD mode with a given standby duration value.

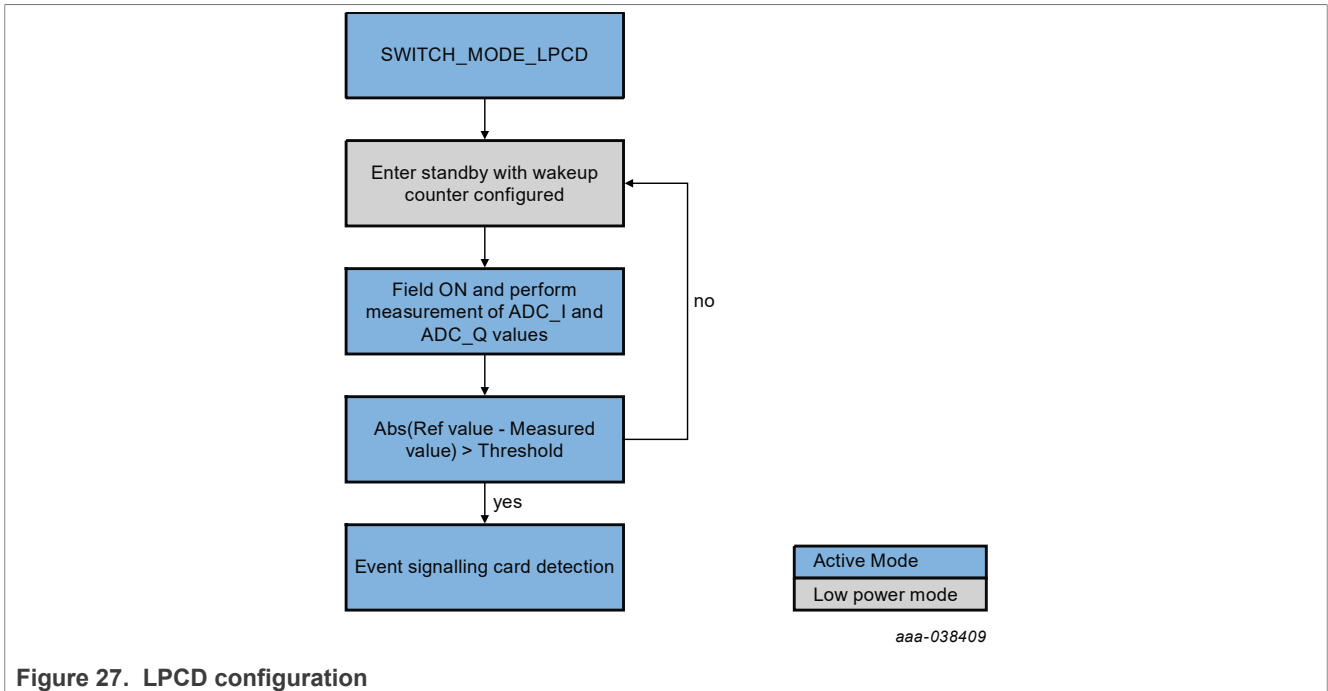


Figure 27. LPCD configuration

The LPCD mode is entered by the host interface command SWITCH\_MODE\_LPCD (23h), and terminated by the command SWITCH\_MODE\_NORMAL (20h). In addition, terminating the LPCD mode is possible by toggling a GPIO, by a reset (VEN) of the PN5190B1 or a signal of the RF Level detector.

Before entering the LPCD mode, ADC\_I and ADC\_Q reference value needs to be determined. This is done during the so-called calibration.

**LPCD calibration phase**

- a) An initial calibration measurement is performed to set up the RX chain parameters namely HFATT, DCO\_DAC\_I\_CTRL and DCO\_DAC\_Q\_CTRL values.
- b) The next measurement is done using the RX chain parameters that are set up, to arrive at the ADC\_I and ADC\_Q values which are used as reference values. All following LPCD measurements are done relative to the LPCD calibration measurement.

**The LPCD loop** itself works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN5190B1.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the ADC\_I and ADC\_Q values are compared to a reference value.

- If the ADC\_I and ADC\_Q values exceed the reference value, a LPCD\_IRQ is raised to the host. The register configurations done by the host to support a dedicated RF protocol are not restored after wake-up command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the ADC\_I and ADC\_Q values do not exceed the thresholds of the reference value, no LPC\_IRQ is raised and the IC is set to the first phase (Standby mode) again.

These two phases are executed in a loop until:

- Card / metal is detected (LPCD\_IRQ is raised).
- Reset occurs, which resets all the system configurations. The LPCD is also terminated in this case.
- NTS on host interface
- RF Level Detected
- GPIO toggle

As functionality from FW2.03 onwards, the GPIO1 (general-purpose input/output) pin can be enabled to wake up an external DC-DC from power down for the VDDPA supply. The GPO1 allows setting to high before the transmitter is switched on. This allows the wake-up of an external DC-DC from power down. The GPO1 can be set to low after the RF field is switched off to set an external DC-DC into Power-down mode. The time of toggling the GPO1 in relation to the RF-on and RF-off timings can be configured:

EEPROM field LpcdExtDcdcEnable (0xCE0) is used to enable the use of EXT DC-DC during LPCD.

EEPROM field: LpcdExtDcdcDelayToOn (0xCE1) is used to configure the delay to turn on the DC-DC in 8usecs steps.

EEPROM field: LpcdExtDcdcDelayToOff (0xCE2) is used to configure the delay to turn off the DC-DC in 8usecs steps.

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF\_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH\_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD\_FIELD\_ON\_TIME starts to count as soon as the RF\_ON command terminates.

**Table 11. Low-Power Card Detection: relevant EEPROM configuration**

| EEPROM address | Name             | Description   |
|----------------|------------------|---|
| 0492           | LPCD_AVG_SAMPLES | Defines how many samples of the I and Q values are used for the averaging. Used to optimize the system to achieve highest detection sensitivity versus false alarms.  |
| 0494           | LPCD_RSSI_TARGET | Value to be used as the RSSI target in the calibration phase to arrive at the RX chain parameters.<br>This parameter is used to arrive at an optimal target voltage level at RXP.                               |
| 0496           | LPCD_RSSI_HYST   | Value to be used as the RSSI hysteresis in the calibration phase to arrive at the RX chain parameters.<br>This is used to avoid oscillations while arriving at the target voltage level at RXP.                 |
| 049A           | LPCD_THRESHOLD   | If the difference between the measured value of I/Q and the reference value for I/Q is greater than the threshold on either channels, then a card is detected.  |
| 04B5           | LPCD_VDDPA       | VDDPA voltage when DC-DC (internal or external) or external power source is used to feed TXLDO  |
| 0013           | XTAL_CHECK_DELAY | Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). For fastest start-up this time, a check is performed at a time slightly higher than the expected startup time of the crystal. |

### 9.15.2 Semi-autonomous mode (LPCD)

**LPCD semi-autonomous mode**

The LPCD can be invoked by the host in the semi-autonomous mode wherein the ADC\_I and ADC\_Q values that are measured is returned back to the host.

In this mode, standby is not entered and the difference between the measured and reference values are not checked against the threshold. Nevertheless, the host may check the measured values against a reference and threshold to detect a card and also put the PN5190B1 in Standby mode between measurements, using the SWITCH\_MODE\_STANDBY command.

This mode is especially useful to find optimized settings for the LPCD, since it does not offer no significant current saving.

**Table 12. Low-Power Card Detection - semi-autonomous mode: relevant REGISTERS**

| REGISTER address | Name                  | Description  |
|------------------|-----------------------|--|
| 0050             | LPCD_CALIBRATE_CTRL   | Writing to this register triggers the LPCD calibration with the LPCD RSSI_HYSTERESIS and LPCD RSSI_TARGET values. After calibration is completed, calibration status is available in LPCD_CALIBRATE_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ_CHANNEL_VALS |
| 0051             | IQ_CHANNEL_VALS       | Actual I/Q channel value   |
| 0053             | LPCD_CALIBRATE_STATUS | 1: if successful - a new calibration clears this value   |

**9.15.3 Ultra low-power card detection (ULPCD)**

The ULPCD (ultra low-power card detection) offers highest current saving. In this mode, the only wake-up sources to escape from the card detection loop are either a detected antenna detuning, a signal on GPIO3 or a reset (RESET\_N) of the PN5190B1.

**The ULPCD cannot be used together with the DC-DC function. A connection as described in the chapter "TX\_LDO transmitter supply" or "Direct transmitter supply" is recommended.**

Only the wake-up timer is active during ULP standby state.

The ULPCD comprises 2 phases:

**1. Calibration phase**

In this phase, an RF field is established and the field strength(RSSI) for the unloaded state of the antenna is measured to be used during the measurement phase and stored in a low-power persistent register.

**2. Measurement phase**

In the measurement phase, the card detection activity is performed autonomously by the hardware at configurable time intervals. This configuration is passed as a parameter to the SWITCH\_MODE\_LPCD command. The RSSI value is measured and compared against the reference value measured in the calibration phase. A card is detected to be in the proximity of the reader when the measured RSSI differs from the reference RSSI by more than a configurable threshold.

The host can set the PN5190B1 into ultra-low power card detection state (ULP standby state) via the instruction SWITCH\_MODE\_LPCD.

XTAL\_CHECK\_DELAY (0013h) allows to optimize the startup of the crystal for the LPCD and ULPCD modes.

The following EEPROM configuration is available:

- ULPCD\_VOLTAGE\_CTRL (address 4C6h)
- ULPCD\_RSSI\_GUARD\_TIME (04C9h)

- ULPCD\_RSSI\_SAMPLE\_CFG (04CAh)
- ULPCD\_THRESH\_LVL(04CBh)
- ULPCD\_GPIO3 (04CCh) - Allows to abort the ULPCD based on GPIO input.

## 9.16 Automatic EMD error handling

The PN5190B1 supports a configurable EMD handling according to the ISO14443 or EMVCo standard. To support further extensions or changes of these standards, the EMD block is configurable.

After being configured, the PN5190B1 restarts both the receiver and a timeout timer automatically without host interaction in case of a detected EMD event.

Features of the Automatic EMD Error Handling:

- No real-time constraints
- Less processing load on the host processor
- Configurable, anticipating future specification changes

In addition to the EMD error handling according to ISO14443 and EMVCo, the PN5190B1 implements special features for FeliCa™ preamble processing.

Registers CLIF\_RX\_EMD\_1\_CONFIG(0x47) and CLIF\_RX\_EMD\_0\_CONFIG(0x48) hold the configurations for the EMD configurations for ISO/IEC14443, and NFC Forum.

EMVCo EMD configuration is supported in the register EMD\_CONTROL (0x03).

## 9.17 Autocoll (card emulation)

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC Forum Active and Passive Target activation (card emulation mode).

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip enters Standby mode automatically
- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFoff, the chip does not enter Standby mode.

At startup, the Autocoll state machine automatically performs a LOAD\_RF\_CONFIG with the General Target Mode Settings. When a technology is detected during activation, the Autocoll state machine performs an additional LOAD\_RF\_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled (EEPROM configuration), a random UID is generated after each RF-off.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own field.

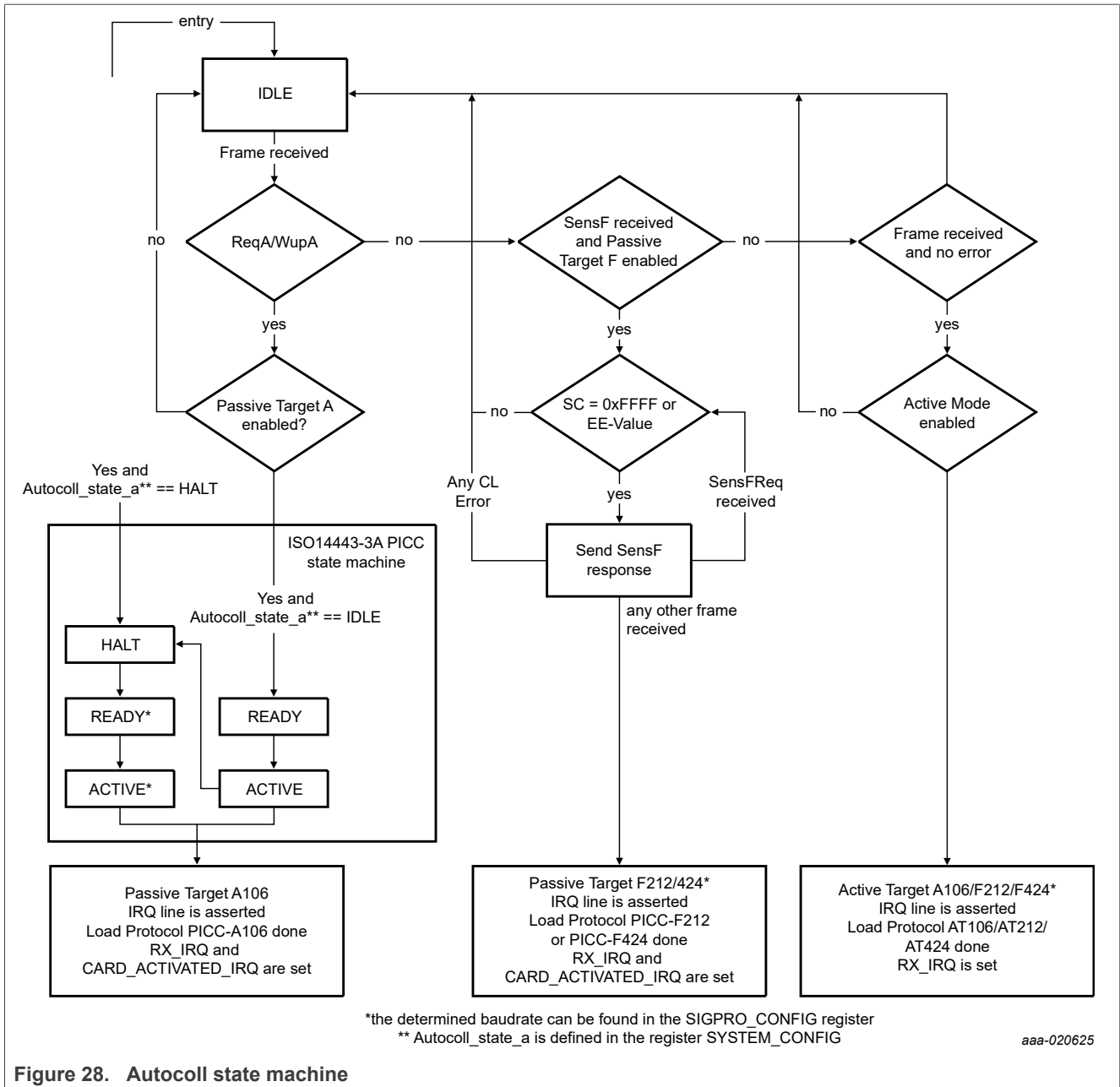


Figure 28. Autocoll state machine

### 9.18 RF-level detection

The PN5190B1 implements an RF level detector (RFLD) and an NFC level detector (NFCLD) which allows to detect the presence of an external RF field.

#### RF Level Detector:

During low-power card detection (LPCD), the RF level detector (RFLD) acts as wake-up source from power-saving mode.

During ultra low-power card detection (ULPCD), a specific ultra low-power RF level detector is used as RF level detector(RFLD). This can be enabled as wake-up source.

The purpose of the RFLD function is to detect any signal at 13.56 MHz in order to wake up the PN5190B1 from power-saving mode.

**NFC Level Detector:**

The NFC Level detector (NFCLD) is used during full power mode. The NFCLD function is required by NFC Forum to support the "RF collision avoidance".

The sensitivity of the NFCLD sensor can be configured by EEPROM register to meet the NFC Forum requirements.

It can be used as well in card mode to detect an external field.

**9.19 Antenna connection**

The PN5190B1 allows to connect antennas of different topology and matching to the transmitter.

Standard and recommended tuning of the antenna fitting to most applications is a symmetrical matched antenna connected to TX1, TX2 operating in push-pull operation.

VBAT is connected to VBATPWR.

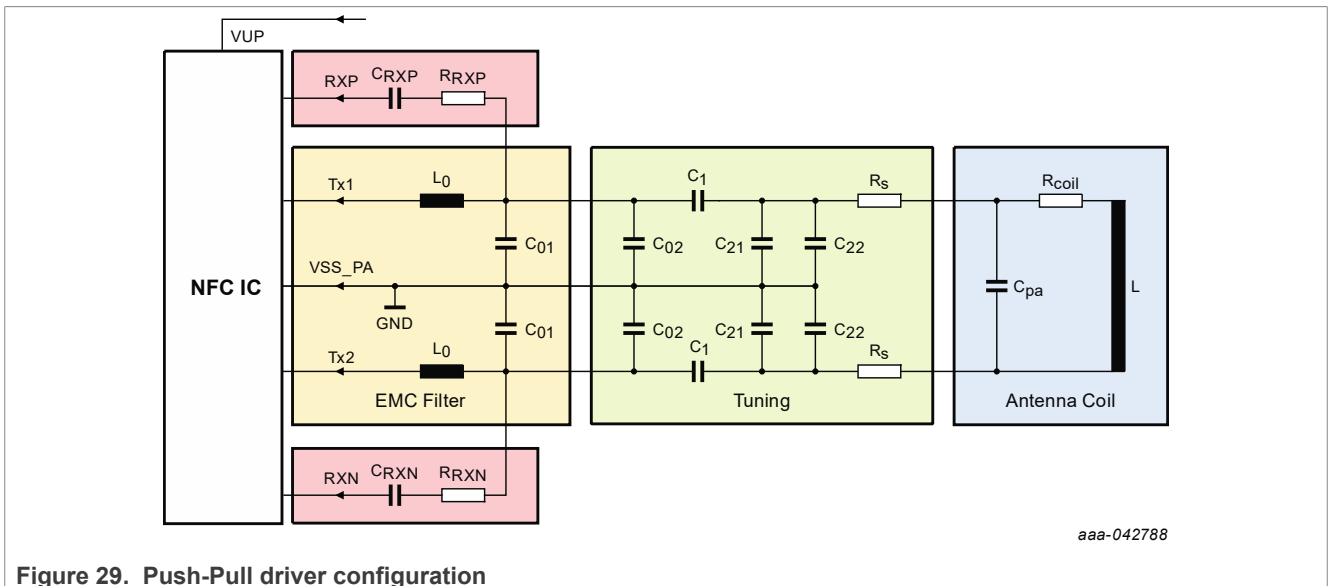


Figure 29. Push-Pull driver configuration

The PN5190B1 allows to operate the TX1, TX2 in common mode as well, which allows to use a single ended antenna. This configuration saves one EMC filter coil.

**Note:**

The RSSI Target for SE needs to be calculated as follows and differs from the differential antenna:  $RSSI\ Target = Target\ RX\ Peak\ Voltage * 1024 / (1.8 * 2)$

Example: For a 1.2 V target:  $DGRM\_RSSI\_TARGET = 1.2 * 1024 / (1.8 * 2) = 341d = 0x155$



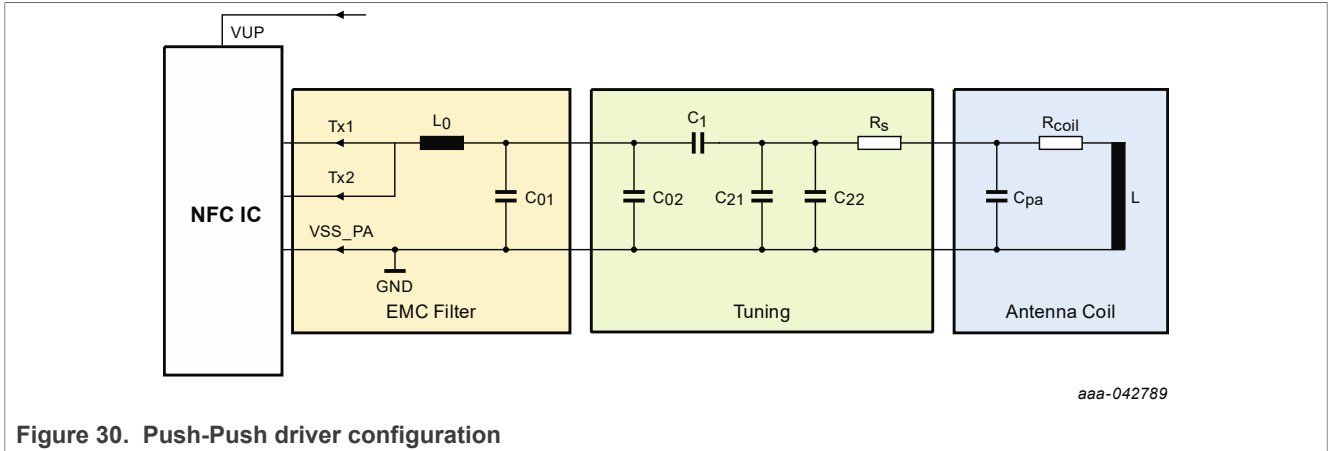


Figure 30. Push-Push driver configuration

The PN5190B1 allows to connect to antennas, one to each of the available driver outputs. The Figure below shows as well the receiver schematics for the RXN which is applicable for the Push-Push driver configuration as well.

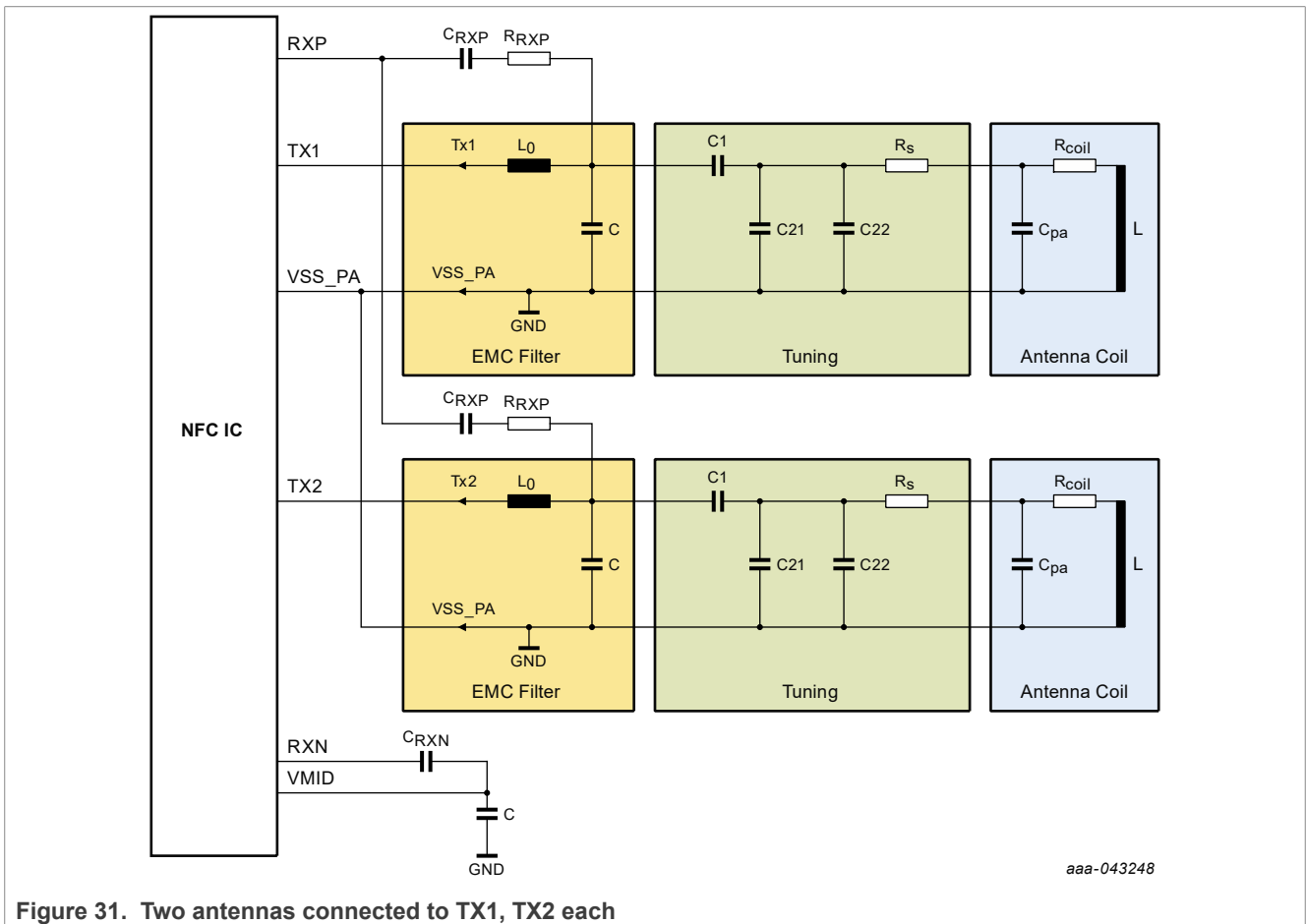


Figure 31. Two antennas connected to TX1, TX2 each

Table 13. Antenna register configuration

| Register (Address)  | Bit                   | Differential Antenna Push-Pull driver TX1, TX2 | Single-Ended Push-Push driver TX1, TX2  | Single-Ended TX1 driving  | Single-Ended TX2 driving  |
|---|-----------------------|--|---|---|---|
| SS_TX_CFG (0x15)<br>Stored as part of the RF protocol configuration                                 | TX2_USE_TX1_CONF      | 1b   | 1b  | 0b  | 0b  |
| SS_TX1_RMCFG (0x16)   | TX1_CLK_MODE_TRANS_RM | 111b   | 111b  | 111b  | 001b  |
| SS_TX1_RMCFG (0x16)   | TX1_CLK_MODE_MOD_RM   | 111b   | 111b  | 111b  | 001b  |
| SS_TX1_RMCFG (0x16)   | TX1_CLK_MODE_CW_RM    | 111b   | 111b  | 111b  | 001b  |
| SS_TX2_RMCFG (0x17)   | TX2_CLK_MODE_TRANS_RM | do not care                                    | do not care   | 001b  | 111b  |
| SS_TX2_RMCFG (0x17)   | TX2_CLK_MODE_MOD_RM   | do not care                                    | do not care   | 001b  | 111b  |
| SS_TX2_RMCFG (0x17)   | TX2_CLK_MODE_CW_RM    | do not care                                    | do not care   | 001b  | 111b  |
| DGRM_RSSI (0x30)<br>Stored as part of the RF protocol configuration                                 | DGRM_RSSI_TARGET      | direct entry                                   | as per calculation for SE<br>(RSSI Target = Target RX Peak Voltage*1024/ (1.8*2)) | as per calculation for SE<br>(RSSI Target = Target RX Peak Voltage*1024/ (1.8*2)) | as per calculation for SE<br>(RSSI Target = Target RX Peak Voltage*1024/ (1.8*2)) |
| ANA_RX_CTRL (0x43)<br>Stored as part of the RF protocol configuration                               | RX_MIXER_SE_MODE_EN   | 0  | 1   | 1   | 1   |
| ANACTRL_TX_CONFIG (0x44)<br>Stored as part of the EEPROM configuration, loaded during load protocol | TX_INV_P_RM           | 10b  | 00b   | no impact   | no impact   |

Table 13. Antenna register configuration...continued

| Register (Address)   | Bit            | Differential Antenna Push-Pull driver TX1, TX2 | Single-Ended Push-Push driver TX1, TX2 | Single-Ended TX1 driving | Single-Ended TX2 driving |
|--|----------------|--|--|--------------------------|--------------------------|
| ANACTRL_TX_CONFIG (0x44)<br>Stored as part of the EEPROM configuration, loaded during load protocol<br>- with 2 different antenna connected the TX shaping needs to be disabled. | TX_PWM_MODE_RM | 0b   | 0b                                     | 1b                       | 1b                       |

**Note:**

Recommendation is to use all the settings configured in EEPROM for each technology and baud rate so that the value is loaded after every load protocol.

Table 14. Antenna EEPROM configuration

| EEPROM (Address)                        | Bit | Differential Antenna Push-Pull driver TX1, TX2 | Single-Ended Push-Push driver TX1, TX2 | Single-Ended TX1 driving        | Single-Ended TX2 driving        |
|---|-----|--|--|---------------------------------|---------------------------------|
| TX_SHAPING_CONFIG (0x17)                | 0   | 0  | 0                                      | 1                               | 1                               |
| RM_GLOBAL_TX_SHAPING. bTX_INV_RM (0x18) | -   | 0x02   | 0x00                                   | do not care, leave default 0x02 | do not care, leave default 0x02 |

**9.20 Antenna tuning with variable capacitors**

The PN5190B1 allows the tuning of the connected antenna based on variable capacitors.

Variable capacitors are devices which allow to change their capacity dependent on a supplied control voltage. Typically, these capacitors are used as serial and parallel capacitors in an antenna matching network.

The PN5190B1 allows to measure a detuning of the connected antenna caused e.g. by surrounding metal and correct the actual detuning by applying an appropriate control voltage on 2 analog outputs.

To correct a potential detuning of the connected antenna, a phase measurement needs to be performed. The following sequence is required to read out the phase information:

Step 1: Disable DPC

Step 2: Perform Type A-106 load protocol

Step 3: Set the VDDPA Voltage as  $V_{(Vddpa\_AAT)}$

Step 4: Perform RF ON

Step 5: Read out RXM phase

Step 6: Perform RF OFF

Step 7: Enable DPC

For reading the RXM phase, refer to the related application note. Based on the phase information, a host is able to calculate the DAC output voltages to correct a detuning.

The antenna tuning requires the DPC to be disabled, and is typically not suitable for dynamic tuning e.g. during card communication.

**Note:**

Since disabling of the DPC requires a modification of the EEPROM is required, care must be taken not to exceed the maximum permitted number of Erase/Write cycles.

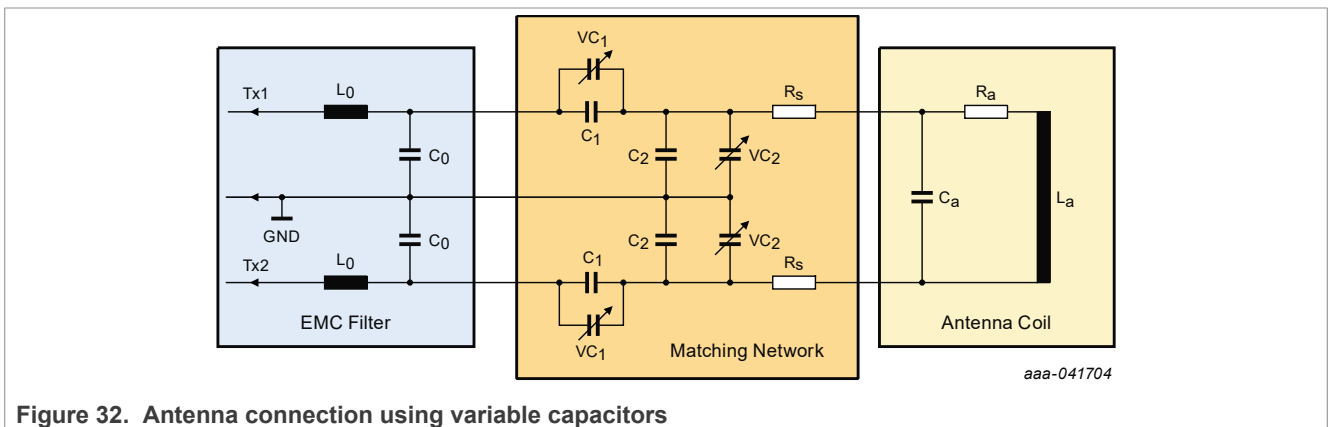


Figure 32. Antenna connection using variable capacitors

**9.21 RF debug signals**

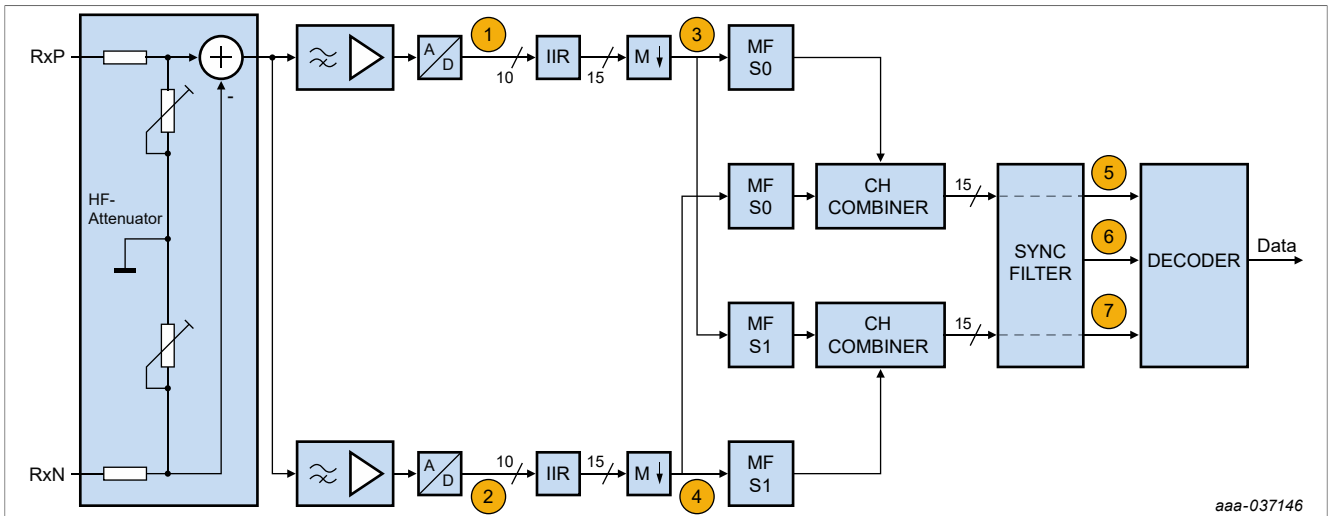
The following signals are available for debugging purposes:

The test signals are selected by sending a command string to the PN5190B1. The commands CONFIGURE\_TESTBUS\_DIGITAL (12h) and CONFIGURE\_TESTBUS\_ANALOG (13h) are used to configure the dedicated signal on an output pin.

If used, **ADC-Q needs to be routed always to AUX1, ADC-I needs to be routed always to AUX2.**

The analog test signals are analog representation of an internal digital value. The internal digital signal is converted by an 8-bit wide DAC to the analog signal.

This overview indicates the signals which are available for debugging purposes (indicated by numbers):



aaa-037146

Figure 33. Receiver block diagram

Table 15. DEBUG SIGNALS

| Signal                         | REGISTER                     | SIGNAL NAME    | BITS   | Description   |
|--------------------------------|------------------------------|----------------|--------|---|
| ADC Data I Channel (1)         | obs_clif_tbcontrol_patchbox0 | adc_data_i_i   | 9:2    | Unfiltered I channel signal upper 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)  |
|                                | obs_clif_tbcontrol_patchbox1 |                | 9; 6:0 | Unfiltered I channel signal lower 7 bit of the 10 bit signed unfiltered I channel signal including sign (bit9)  |
| ADC Data Q Channel (2)         | obs_clif_tbcontrol_patchbox2 | adc_data_q_i   | 9:2    | Unfiltered Q channel signal upper 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)  |
|                                | obs_clif_tbcontrol_patchbox3 |                | 9; 6:0 | Unfiltered Q channel signal lower 7 bit of the 10 bit signed unfiltered Q channel signal including sign (bit9)  |
| Preprocessor Out I Channel (3) | obs_clif_sigpro_rm0          | rm_cor_adc_i_o | 14:8   | Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU |
|                                | obs_clif_sigpro_rm1          |                | 7:0    | Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data I channel, after IIR filter and down-sampling                                    |
| Preprocessor Out Q Channel (4) | obs_clif_sigpro_rm2          | rm_cor_adc_q_o | 14:8   | Pre-processed ADC data I channel upper 7bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling including sign (bit14) bit 15: RFU |
|                                | obs_clif_sigpro_rm3          |                | 7:0    | Pre-processed ADC data I channel lower 8bit of 15bit signed pre-processed ADC data Q channel, after IIR filter and down-sampling                                    |
| Output MF S0 (5)               | obs_clif_sigpro_rm4          | mf_pt_s0_d     | 14:8   | Delayed matched filter S0 output, after CH combiner   |

Table 15. DEBUG SIGNALS ...continued

| Signal                            | REGISTER            | SIGNAL NAME   | BITS | Description   |
|-----------------------------------|---------------------|---------------|------|---|
|                                   |                     |               |      | upper 7 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore)   |
|                                   | obs_clif_sigpro_rm5 |               | 7:0  | Delayed matched filter S0 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S0 output, after Channel combiner   |
| Output MF S1 (6)                  | obs_clif_sigpro_rm6 | mf_pt_s1_d    | 14:8 | Delayed matched filter S1 output, after CH combiner upper 7 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner including sign (bit14) bit 15: RFU (ignore) Remark: S1 is not relevant for type A 106 |
|                                   | obs_clif_sigpro_rm7 |               | 7:0  | Delayed matched filter S1 output, after CH combiner lower 8 bit of the 15 bit signed delayed matched filter S1 output, after Channel combiner Remark: S1 is not relevant for type A 106   |
| Output Synchronization Filter (7) | obs_clif_sigpro_rm8 | sync_filt_out | 14:8 | Synchronization filter output upper 7 bit of the 15 bit signed synchronization filter output including sign (bit14) bit 15: RFU (ignore)  |
|                                   | obs_clif_sigpro_rm9 |               | 7:0  | Synchronization filter output lower 8 bit of the 15 bit signed synchronization filter output  |
| clif_status                       | transceive_state    |               | 7:5  |   |
|                                   | rx_cl_error         |               | 4    |   |
|                                   | tx_envelope         |               | 3    |   |
|                                   | rx_enevelope        |               | 2    |   |
|                                   | svalid              |               | 1    |   |
|                                   | sdata               |               | 0    |   |
| clif_transceive                   | rx_start_receive    |               | 7    |   |
|                                   | rx_over_ok          |               | 6    |   |
|                                   | rx_over_term        |               | 5    |   |
|                                   | rx_resume           |               | 4    |   |
|                                   | sgp_msg_busy        |               | 3    |   |
|                                   | fig_reset_sigpro    |               | 2    |   |
|                                   | fig_reset_rxdec     |               | 1    |   |
|                                   | cfg_sw_reset_sigpro |               | 0    |   |

Table 16. TRIGGER SIGNALS

| TRIGGER   | REGISTER        | SIGNAL NAME | BITS | Description   |
|-----------|-----------------|-------------|------|---|
| TX Active | obs_clif_txenc1 | tx_active_o | 1    | high level indicates transmission of data Remark: Falling edge can be used to trigger on end of transmission. |

Table 16. TRIGGER SIGNALS...continued

| TRIGGER               | REGISTER             | SIGNAL NAME | BITS | Description  |
|-----------------------|----------------------|-------------|------|--|
| RX Enable             | obs_clif_sigpro_rm15 | rx_enable_o | 1    | high level indicates that the reception is ongoing Remark: can be used to trigger on the start /end of reception |
| RX collision detected | obs_clif_sigpro_rm14 | rm_scoll_o  | 1    | high-level pulse indicates that the collision is detected during reception                                       |

## 9.22 Secure firmware update

The PN5190B1 supports a secure update of the implemented firmware.

The secure firmware download mode is using dedicated commands, but does not require a dedicated physical handling of the SPI interface lines.

The secure firmware download mode is entered by setting a register in non-volatile memory followed by a trigger of the VEN pin.

The firmware binary file which is used to update the PN5190B1 is protected with an RSA signature and AES encryption.

The key length of the RSA is 2048 bits, the public exponent supports any 32-bit integer value.

A pre-computed Montgomery format of signature is used, and the signature hash computation is based on SHA256 algorithm.

This prevents a download of any other software which is not released by NXP.

An anti-tearing function is implemented in order to detect supply voltage removal or memory fault.

During the secure firmware download, the NFC operation is not available, only the command set defined for the secure firmware download is valid.

**Updating the PN5190B1 with the default firmware binaries programs the memories for user configuration with default values. Any previous user configuration is overwritten. The user has to take care to restore the data of these memories after a secure firmware update.**

**If this is not intended, special firmware versions are available which do not overwrite the configuration. If the standard firmware file is named e.g. FW XX.YY, the name of the firmware which does not overwrite existing settings is then FW XX.FY. (The "F" is indicating the non-overwrite version)**

The PN5190B1 checks if the new major version number is equal or higher than the current one. In case the major version number of the new firmware to be installed is smaller than the already installed version number of the firmware, the secure firmware update is rejected. Downgrading major firmware versions is therefore not possible. Upgrading and therefore increasing major firmware versions is always possible.

In case of any failure or exception during the download (e.g. caused by a communication error or power off), the PN5190B1 remains in the secure firmware download mode until a complete and valid NXP firmware is available in the device.

Features of the automatic secure firmware update:

- Works without download request pin
- No special implementation of SPI interface handling
- Maximum integrity: Only encrypted and signed firmware images download possible via the secure firmware update functionality

- Updating the firmware overwrites existing all previous EEPROM configurations, unless a special version of the firmware was used.

## 9.23 SPI host interface

The interface of the PN5190B1 to a host microcontroller is based on a SPI interface.

The maximum SPI speed is 15 Mbit/s and fixed to CPOL = 0 and CPHA = 0. Only a half-duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer shall be written at once as well. No NSS assertion is allowed during data transfer.

The SPI host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of CPUs. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (pin VDDIO).

There is no external pull-up / pull-down resistor required, the SPI pads are automatically configured by the PN5190B1.

Only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.4 V.

**Note:** The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT.

### Controller in target out (MISO)

The MISO line is configured as an output in a target device. It is used to transfer data from the target to the controller, with the most significant bit sent first. The MISO signal is put into 3-state mode when NSS is high.

### Controller out target in (MOSI)

The MOSI line is configured as an input in a target device. It is used to transfer data from the controller to a target, with the most significant bit sent first.

### Serial clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

### Not target select (NSS)

The target select input (NSS) line is used to select a target device. It shall be set to low before any data transaction starts and must stay low during the transaction.

## 9.24 Host interface commands

### 9.24.1 Logical command layer

PN5190B1 has two main modes of operation to communicate with the host controller:

1. TLV-command response-based communication
2. HDLL-based communication, used when device is triggered to enter the “download mode”, to update its firmware.

The description of the transport layer in the next chapters is limited to TLV-based command-response communication.

For more information, see [\[3\]](#).



### 9.24.1.1 Logical frame definition

A SPI frame starts with the falling edge of NSS and ends with the rising edge of NSS.

SPI is per physical definition full duplex but PN5190B1 uses SPI in a half-duplex mode.

SPI mode is limited to CPOL 0 and CPHA 0 with a max clock speed of 15 MHz.

Every SPI frame is composed of a 1-byte header and n-bytes of body.

### 9.24.1.2 Logical flow definition

The HOST always sends as a first byte the flow indication byte whether it wants to write or read data from the PN5190B1.

In case of a read request and no data is available, the response contains 0xFF.

The data after the flow indication byte is one or several messages.

For every NSS assertion, the first byte is always a HEADER (flow indication byte), it can be either 0x7F/0xFF with respect to write/read operation.

### 9.24.1.3 Logical message type definition

A host controller communicates with PN5190B1 using messages which are transported within SPI frames.

There are three different message types:

- Command
- Response
- Event

Commands are only sent from host controller to PN5190B1 responses.

Events are only sent from PN5190B1 to host controller.

Allowed sequences and rules:

- Command is always acknowledged by a response
- Host Controller is not allowed to send another command before receiving a response to a previous command, except in concatenation
- Events may be sent asynchronously at any time (NOT interleaved within a command/response pair)
- EVENT messages are never combined with the RESPONSE messages within one frame.

### 9.24.1.4 Logical message format

**Type (T)** => 1 byte

Bit[7] Message Type

0: COMMAND or RESPONSE message

1: EVENT message

Bit[6:0]: Instruction Code

**Length (L)** => 2 bytes (large endian format)

Length of the message body

**Value (V)** => N bytes

Value/data of the TLV (Command Parameters / Response data) based on Length field (Large endian format)

**9.24.1.5 Split frame definition**

COMMAND message must be sent in one SPI frame RESPONSE and EVENT messages can be read in multiple SPI frames, e.g., to read out the length byte.

RESPONSE and EVENT messages can be read in single SPI frame but delayed by NO-CLOCK in between, e.g., to read out the length byte.

**9.24.2 Host interface command list**

PN5190B1 command/response list

Table 17. Host interface commands

| Command code | PN5180 legacy command | Command   |
|--------------|-----------------------|---|
| 0x00         | Yes                   | WRITE_REGISTER  |
| 0x01         | Yes                   | WRITE_REGISTER_OR_MASK  |
| 0x02         | Yes                   | WRITE_REGISTER_AND_MASK   |
| 0x03         | Yes                   | WRITE_REGISTER_MULTIPLE   |
| 0x04         | Yes                   | READ_REGISTER   |
| 0x05         | Yes                   | READ_REGISTER_MULTIPLE  |
| 0x06         | Yes                   | WRITE_EEPROM  |
| 0x07         | Yes                   | READ_EEPROM   |
| 0x08         | No                    | TRANSMIT_RF_DATA  |
| 0x09         | No                    | RETRIEVE_RF_DATA  |
| 0x0A         | No                    | EXCHANGE_RF_DATA  |
| 0x0B         | Yes                   | MFC_AUTHENTICATE  |
| 0x0C         | Yes                   | EPC_GEN2_INVENTORY  |
| 0x0D         | Yes                   | LOAD_RF_CONFIGURATION   |
| 0x0E         | Yes                   | UPDATE_RF_CONFIGURATION   |
| 0x0F         | Yes                   | GET_RF_CONFIGURATION  |
| 0x10         | Yes                   | RF_ON   |
| 0x11         | Yes                   | RF_OFF  |
| 0x12         | Yes                   | CONFIGURE_TESTBUS_DIGITAL (not available for engineering samples) |
| 0x13         | Yes                   | CONFIGURE_TESTBUS_ANALOG (not available for engineering samples)  |
| 0x14         | No                    | CTS_ENABLE  |
| 0x15         | No                    | CTS_CONFIGURE   |
| 0x16         | No                    | CTS_RETRIEVE_LOG  |

Table 17. Host interface commands...continued

| Command code | PN5180 legacy command | Command  |
|--------------|-----------------------|--|
| 0x17 - 0x18  | -                     | RFU  |
| 0x19         | No                    | up to FW 2.01: RFU   |
|              |                       | from FW2.03 onwards: RETRIEVE_RF_FELICA_EMD_DATA                   |
| 0x1A         | No                    | RECEIVE_RF_DATA  |
| 0x1B-0x1F    | -                     | RFU  |
| 0x20         | Yes                   | SWITCH_MODE_NORMAL   |
| 0x21         | Yes                   | SWITCH_MODE_AUTOCOLL   |
| 0x22         | Yes                   | SWITCH_MODE_STANDBY  |
| 0x23         | No                    | SWITCH_MODE_LPCD   |
| 0x24         | No                    | SWITCH_MODE_SUSPEND  |
| 0x25         | No                    | SWITCH_MODE_DOWNLOAD   |
| 0x26         | No                    | GET_DIE_ID   |
| 0x27         | No                    | GET_VERSION  |
| 0x28         | -                     | RFU  |
| 0x29         | No                    | GET_CRC_USER_AREA (available from FW 2.6 onwards)                  |
| 0x2A         | -                     | up to FW 2.03: RFU   |
|              | No                    | available from FW 2.05 onwards: CONFIGURE_MULTIPLE_TESTBUS_DIGITAL |
| 0x2B - 0x3F  | -                     | RFU  |
| 0x40         | -                     | RFU  |
| 0x41         | No                    | PRBS_TEST  |
| 0x41 - 0x50  | -                     | RFU  |

Below is a list of CLIF registers that are changed by the firmware between an RF Exchange followed by an RF Reset command:

Table 18. Register values changed by firmware between RF Exchange - RF Reset

| Register name                      | After first exchange | RF Reset after first exchange | Changes done in RF-ON      |
|------------------------------------|----------------------|-------------------------------|----------------------------|
| CLIF_STATUS_REG (Read-Only)        | 04000001             | 04000000                      | NA                         |
| CLIF_CONTROL_REG                   | 00000003             | 00000000                      | Command bit is set to IDLE |
| CLIF_CRC_RX_CONFIG_REG             | 00000008             | 00000009                      | RX CRC Is enabled          |
| CLIF_CRC_TX_CONFIG_REG             | 00000008             | 00000009                      | TX CRC is enabled          |
| CLIF_RXCTRL_STATUS_REG (Read-Only) | 07758704             | 077D8704                      | NA                         |

Table 18. Register values changed by firmware between RF Exchange - RF Reset ...continued

| Register name                    | After first exchange | RF Reset after first exchange | Changes done in RF-ON                               |
|----------------------------------|----------------------|-------------------------------|---|
| CLIF_DCOC_STATUS_REG (Read-Only) | 002607C8             | 001807B5                      | NA  |
| CLIF_TIMER0_CONFIG_REG           | 00000000             | 0000007D                      | Timer0 Configuration changes. But Timer not started |
| CLIF_TIMER0_RELOAD_REG           | 00000000             | 00000109                      | Timer0 Configuration changes.                       |
| CLIF_TIMER3_OUTPUT_REG           | 01000018             | 00000000                      | Timer3 Configuration changes.                       |
| CLIF_ANA_STATUS_REG (Read-Only)  | 001E404B             | 001D9831                      | NA  |
| CLIF_INT_STATUS_REG (Read-Only)  | 00000000             | 00000004                      | NA  |
| CLIF_INT_ENABLE_REG (Read-Only)  | 00060F21             | 00068F21                      | NA  |

9.24.3 EVENTS INDICATED BY INTERRUPT

Normal events are indicated over IRQ.

These normal events can be either

- always enabled - Host is always notified
- controlled by Host – Host is notified if the respective Event Enable bit is set in the register (EVENT\_ENABLE).

Low-level interrupts from the peripheral IPs including the CLIF are completely handled within the firmware and the host will be notified only of the events listed in the events section.

The firmware implements two event registers as RAM registers that can be written / read using WRITE\_REGISTER / READ\_REGISTER commands.

Two registers do exist to handle the events from a host microcontroller: EVENT\_ENABLE and EVENT\_STATUS:

- EVENT\_ENABLE => register, enables/disables specific event notifications
- EVENT\_STATUS => content of this register is part of the event message payload

Events are autocleared once the event message is read-out by the host.

Events are asynchronous in nature and are notified to the host if they are enabled within the event register.

Following is the list of events available to the host as part of the event message:

Table 19. IRQ EVENT LIST

| BIT    | EVENT     | Always enabled | Value/Description |
|--------|-----------|----------------|-------------------|
| 31..12 | RFU       | -              | -                 |
| 11     | CTS_EVENT | N              |                   |

Table 19. IRQ EVENT LIST ...continued

| BIT | EVENT                | Always enabled | Value/Description |
|-----|----------------------|----------------|-------------------|
| 10  | IDLE_EVENT           | Y              |                   |
| 9   | LP_CALIBRATION_EVENT | Y              |                   |
| 8   | LPCD_EVENT           | Y              |                   |
| 7   | AUTOCOLL_EVENT       | Y              |                   |
| 6   | TIMER0_EVENT         | N              |                   |
| 5   | TX_OVERCURRENT_EVENT | N              |                   |
| 4   | RFON_DET_EVENT       | N              |                   |
| 3   | RFOFF_DET_EVENT      | N              |                   |
| 2   | STANDBY_PREV_EVENT   | Y              |                   |
| 1   | GENERAL_ERROR_EVENT  | Y              |                   |
| 0   | BOOT_EVENT           | Y              |                   |

Note that no two events are clubbed except in case of errors. In case of errors during the operation, functional event (e.g. BOOT\_EVENT, AUTOCOLL\_EVENT etc.) and GENERAL\_ERROR\_EVENT will be set.

**9.24.4 EVENTS INDICATED ON GPIO**

Temperature events are possible to be indicated by a GPIO to speed up the notification to a host.

The EEPROM register ENABLE\_GPIO0\_ON\_OVERTEMP (0054h) allows enabling the indication of a temperature event on GPIO0.

No other event can be routed to a GPIO.

**9.25 Register description**

The default setting of a bit within a register is indicated by the "\*". Value indicates the allowed range for the bits of a symbol.

Note, that some registers change its content by the firmware between an RF Exchange followed by an RF Reset command.

**9.25.1 Register overview**

Table 20. Register overview

| Address (HEX) | Address (decimal) | Name               |
|---------------|-------------------|--------------------|
| 0h            | 0                 | SYSTEM_CONFIG      |
| 1h            | 1                 | EVENT_ENABLE       |
| 2h            | 2                 | EVENT_STATUS       |
| 3h            | 3                 | EMD_CONTROL        |
| 4h            | 4                 | FELICA_EMD_CONTROL |
| 5h            | 5                 | RX_STATUS          |
| 6h            | 6                 | RX_STATUS_ERROR    |

Table 20. Register overview...continued

| Address (HEX) | Address (decimal) | Name               |
|---------------|-------------------|--------------------|
| 7h            | 7                 | CLIF_STATUS        |
| 8h            | 8                 | TRANSCEIVE_CONTROL |
| 9h            | 9                 | TX_SYMBOL01_MOD    |
| Ah            | 10                | TX_SYMBOL1_DEF     |
| Bh            | 11                | TX_SYMBOL0_DEF     |
| Ch            | 12                | TX_SYMBOL23_MOD    |
| Dh            | 13                | TX_SYMBOL23_DEF    |
| Eh            | 14                | TX_SYMBOL_CONFIG   |
| Fh            | 15                | TX_FRAME_CONFIG    |
| 10h           | 16                | TX_DATA_MOD        |
| 11h           | 17                | TX_WAIT            |
| 12h           | 18                | TX_CRC_CONFIG      |
| 13h           | 19                | RFU                |
| 14h           | 20                | RFU                |
| 15h           | 21                | SS_TX_CONFIG       |
| 16h           | 22                | SS_TX1_RMCFG       |
| 17h           | 23                | SS_TX2_RMCFG       |
| 18h           | 24                | RFU                |
| 19h           | 25                | SS_TX_TRANS_CFG    |
| 1A-1C         | 26-28             | RFU                |
| 1D            | 29                | SIGPRO_CONFIG      |
| 1E            | 30                | RFU                |
| 1F            | 31                | PUBLIC_RESERVED    |
| 20            | 32                | SIGPRO_RM_PATTERN  |
| 21            | 33                | PUBLIC_RESERVED    |
| 22            | 34                | RFU                |
| 23-24         | 35-36             | PUBLIC_RESERVED    |
| 25            | 37                | RX_PROTOCOL_CONFIG |
| 26            | 38                | RX_FRAME_LENGTH    |
| 27            | 39                | RFU                |
| 28            | 40                | RX_CTRL_STATUS     |
| 29            | 41                | PUBLIC_RESERVED    |
| 2A            | 42                | SIGPRO_IIR_CONFIG0 |
| 2B-2C         | 43-44             | PUBLIC_RESERVED    |
| 2Dh           | 45                | DGRM_BBA           |
| 2E            | 46                | PUBLIC_RESERVED    |

Table 20. Register overview...continued

| Address (HEX) | Address (decimal) | Name                 |
|---------------|-------------------|----------------------|
| 2Fh           | 47                | RFU                  |
| 30h           | 48                | DGRM_RSSI            |
| 31h           | 49                | RX_CRC_CONFIG        |
| 32h           | 50                | RX_WAIT              |
| 33            | 51                | DCOC_CONFIG          |
| 34            | 52                | RFU                  |
| 35            | 53                | RXM_CTRL             |
| 36            | 54                | ANA_AGC_DCO_CTRL     |
| 37            | 55                | RFU                  |
| 38-3A         | 56-58             | PUBLIC RESERVED      |
| 3B            | 59                | SS_TX1_CMCFG         |
| 3C            | 60                | SS_TX2_CMCFG         |
| 3Dh           | 61                | TIMER0_CONFIG        |
| 3Eh           | 62                | TIMER0_RELOAD        |
| 3Fh           | 63                | RFU                  |
| 40h           | 64                | RFU                  |
| 41            | 65                | ANA_STATUS           |
| 42h           | 66                | RFU                  |
| 42            | 67                | ANA_RX_CTRL          |
| 44            | 68                | ANACTRL_TX_CONFIG    |
| 45-46         | 68-70             | RFU                  |
| 47h           | 71                | EMD_1_CONFIG         |
| 48h           | 72                | EMD_0_CONFIG         |
| 49-4F         | 73-79             | RFU                  |
| 50            | 80                | LPCD_CALIBRATE_CTRL  |
| 51            | 81                | IQ_CHANNEL_VALS      |
| 52            | 82                | PAD_CONFIG           |
| 53            | 83                | CALIBRATE_STATUS     |
| 54            | 84                | TXLDO_VDDPA_CONFIG   |
| 55            | 85                | GENERAL_ERROR_STATUS |
| 56            | 86                | TXLDO_VOUT_CURR      |
| 57            | 87                | DAC                  |
| 58            | 88                | RFU                  |
| 59            | 89                | RXM_FREQ             |
| 5A            | 90                | RXM_RSSI             |
| 5B            | 91                | TEMP_SENSOR          |

Table 20. Register overview...continued

| Address (HEX) | Address (decimal) | Name                                 |
|---------------|-------------------|--------------------------------------|
| 5D            | 93                | TX_NOV_CALIBRATE_AND_STORE           |
| 5E            | 94                | DPC_CONFIG                           |
| 5F            | 95                | TIMER0_OUTPUT (from FW 2.05 onwards) |
| 60            | 96                | TIMER1_OUTPUT (from FW 2.05 onwards) |
| 61            | 97                | TIMER2_CONFIG (from FW 2.05 onwards) |
| 62            | 98                | TIMER2_RELOAD (from FW 2.05 onwards) |
| 63            | 99                | TIMER2_OUTPUT (from FW 2.05 onwards) |
| 80            | 128               | SS_TX1_RTRANS0                       |
| 81            | 129               | SS_TX1_RTRANS1                       |
| 82            | 130               | SS_TX1_RTRANS2                       |
| 83            | 131               | SS_TX1_RTRANS3                       |
| 84            | 132               | SS_TX1_RTRANS4                       |
| 85            | 133               | SS_TX1_RTRANS5                       |
| 86            | 134               | SS_TX1_RTRANS6                       |
| 87            | 135               | SS_TX1_RTRANS7                       |
| 88            | 136               | SS_TX1_RTRANS8                       |
| 89            | 137               | SS_TX1_RTRANS9                       |
| 8A            | 138               | SS_TX1_RTRANS10                      |
| 8B            | 139               | SS_TX1_RTRANS11                      |
| 8C            | 140               | SS_TX1_RTRANS12                      |
| 8D            | 141               | SS_TX1_RTRANS13                      |
| 8E            | 142               | SS_TX1_RTRANS14                      |
| 8F            | 143               | SS_TX1_RTRANS15                      |

## 9.25.2 SYSTEM\_CONFIG (0000h)

Table 21. SYSTEM\_CONFIG register (address 0000h) bit description

| Bit  | Symbol                | Access | Value | Description   |
|------|-----------------------|--------|-------|---|
| 31:9 | RFU                   | r/w    | 0*,1  | -   |
| 8    | TX_NOV_CALIBRATION    | r/w    | 0*,1  | One time calibration when the host writes a 1 into this register, a one time calibration is performed.<br><b>Note:</b><br>The calibration is resulting a short RF-on. All the power configurations shall be configured before setting this bit. |
| 7    | RFU                   | r/w    | 0     | -   |
| 6:5  | 15693_CHANGE_DATARATE | r/w    | 0*,1  | 15693_changedatarate<br>0 - RFU<br>1 - Change data rate to 53kB/sec   |



Table 21. SYSTEM\_CONFIG register (address 0000h) bit description...continued

| Bit | Symbol                                 | Access | Value | Description   |
|-----|--|--------|-------|---|
|     |  |        |       | 2 - Change data rate to 106kB/sec<br>3 - Change data rate to 212kB/sec<br>By default, the basic data rate of 26kB/sec is loaded, switching to a different higher data rate requires this config register to be updated. All relevant related registers are updated automatically. |
| 4   | up to FW 2.03:<br>RFU                  | r/w    | 0*,1  | -   |
|     | from FW 2.05 onwards:<br>FAST_FIELD_ON | r/w    | 0*,1  | 0 - Field ON Duration includes time interval to start TXLDO and DC-DC as part of RF ON<br>1 - Field ON Duration is reduced as TXLDO and DC-DC remains ON and only TX Driver is Enabled/ Disabled as part of RF ON   |
| 3   | AUTOCOLL STATE A                       | r/w    | 0*,1  | 0: TypeA Card mode: Autocoll entry with IDLE state of the card<br>1: TypeA Card mode: Autocoll entry with HALT state of the card  |
| 2   | SOFT RESET                             | r/w    | 0*,1  | Performs a soft reset of the system, all registers are set to default values  |
| 1   | MF CRYPTO ON                           | r/w    | 0*,1  | If set to 1 the MIFARE - crypto bit is generated for MIFARE Classic en-/de-cryption   |
| 0   | RFU                                    | r/w    | 0*,1  | -   |

**Note:** For firmware versions up to V2.02, the SYSTEM\_CONFIG register requires to be initialized with value 0x00 upon every Power-On Reset. This initialization is not required for firmware versions V2.03 or higher.

### 9.25.3 EVENT\_ENABLE (0001h)

Table 22. EVENT\_ENABLE register (address 0001h) bit description

| Bit   | Symbol                            | Access | Value | Description                    |
|-------|-----------------------------------|--------|-------|--------------------------------|
| 31:12 | RFU                               | r      | 0*,1  | -                              |
| 11    | CTS_EVENT_ENABLE                  | r/w    | 0*,1  | Enable the corresponding event |
| 10    | IDLE_EVENT_ENABLE                 | r/w    | 0*,1  | Enable the corresponding event |
| 9     | LP_CALIBRATION_EVENT_ENABLE       | r/w    | 0*,1  | Enable the corresponding event |
| 8     | LPCD_EVENT_ENABLE                 | r/w    | 0*,1  | Enable the corresponding event |
| 7     | AUTOCOLL_EVENT_ENABLE             | r/w    | 0*,1  | Enable the corresponding event |
| 6     | TIMER0_EVENT_ENABLE               | r/w    | 0*,1  | Enable the corresponding event |
| 5     | TX_OVERCURRENT_ERROR_EVENT_ENABLE | r/w    | 0*,1  | Enable the corresponding event |
| 4     | RFON_DET_EVENT_ENABLE             | r/w    | 0*,1  | Enable the corresponding event |
| 3     | RFOFF_DET_EVENT_ENABLE            | r/w    | 0*,1  | Enable the corresponding event |
| 2     | STANDBY_PREV_EVENT_ENABLE         | r/w    | 0*,1  | Enable the corresponding event |

Table 22. EVENT\_ENABLE register (address 0001h) bit description...continued

| Bit | Symbol                     | Access | Value | Description                    |
|-----|----------------------------|--------|-------|--------------------------------|
| 1   | GENERAL_ERROR_EVENT_ENABLE | r/w    | 0*,1  | Enable the corresponding event |
| 0   | BOOT_EVENT_ENABLE          | r/w    | 0*,1  | Enable the corresponding event |

### 9.25.4 EVENT\_STATUS (0002h)

Table 23. EVENT\_STATUS register (address 0002h) bit description

| Bit   | Symbol                     | Access | Value | Description   |
|-------|----------------------------|--------|-------|---|
| 31:12 | RFU                        | r      | 0*,1  | -   |
| 11    | CTS_EVENT                  | r      | 0*,1  | Indicated the availability of CTS Event   |
| 10    | IDLE_EVENT                 | r      | 0*,1  | Indicated the availability of IDLE event.   |
| 9     | LP_CALIBRATION_EVENT       | r      | 0*,1  | Indicated the availability of LP Calibration event  |
| 8     | LPCD_EVENT                 | r      | 0*,1  | Indicated the availability of LPCD event.   |
| 7     | AUTOCOLL_EVENT             | r      | 0*,1  | Indicated the availability of Autocoll event  |
| 6     | TIMER0_EVENT               | r      | 0*,1  | Indicated the availability of Timer0 event  |
| 5     | TX_OVERCURRENT_ERROR_EVENT | r      | 0*,1  | Indicated the availability of transmitter over current error.<br>This bit is set, when the current on the TX driver is higher than the defined threshold in the EEPROM. Upon this condition, the field is automatically switched OFF before the notification to the host. |
| 4     | RFON_DET_EVENT             | r      | 0*,1  | Indicated the availability of RF ON detected.   |
| 3     | RFOFF_DET_EVENT            | r      | 0*,1  | Indication of external RF OFF detected  |
| 2     | STANDBY_PREV_EVENT         | r      | 0*,1  | Indicated the availability of Standby Prevention reason.  |
| 1     | GENERAL_ERROR_EVENT        | r      | 0*,1  | Indicated the availability of General Error event.  |
| 0     | BOOT_EVENT                 | r      | 0*,1  | Indicated the availability of Boot event.   |

### 9.25.5 EMD\_CONTROL (0003h)

To activate the EMVCo EMD handling of the PN5190B1, the following bits of the register need to be set as follows:

0001b: EMD\_ENABLE

1b: EMD\_TRANSMISSION\_ERROR\_ABOVE\_NOISE\_THRESHOLD\_IS\_NO\_EMD

0001b: EMD\_NOISE\_BYTES\_THRESHOLD

Table 24. EMD\_CONTROL register (address 0003h) bit description

| Bit   | Symbol                 | Access | Value | Description  |
|-------|------------------------|--------|-------|--|
| 31:12 | RFU                    | rw     | 0*,1  | -  |
| 11:10 | EMD_RM_EMD_SENSITIVITY | rw     | 0*,1  | RM EMD SENSITIVITY value that will be applied to SIGPRO_RM_CONFIG, |

Table 24. EMD\_CONTROL register (address 0003h) bit description...continued

| Bit | Symbol   | Access | Value | Description  |
|-----|--|--------|-------|--|
|     |  |        |       | At layer 4, when EMD is enabled, the value of EMD_RM_SENSITIVITY can be lowered to ensure robust EMD suppression, if during the layer 3 activation, the value of EMD_RM_SENSITIVITY in the protocol area is set to a high value to ensure collision detection and resolution when multiple typeA cards are presented at close distance to the antenna. |
| 9:8 | EMD_TRANSMISSION_TIMER_USED                            | rw     | 0*,1  | Timer used for RF communication.   |
| 7   | EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B               | rw     | 0*,1  | Missing CRC treated as protocol error in » case of Type B based communication P » case of Type B based communication   |
| 6   | EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A               | rw     | 0*,1  | Missing CRC treated as protocol error in » case of Type A based communication P » case of Type A based communication   |
| 5:2 | EMD_NOISE_BYTES_THRESHOLD                              | rw     | 0*,1  | Defines the threshold under which transmission errors are treated as noise.<br>Note: CRC bytes are NOT included/counted!   |
| 1   | EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD | rw     | 0*,1  | Transmission errors with received byte length >= EMD_NOISE_BYTES_THRESHOLD is never treated as EMD (can be used for versions below EMVCo3.0)   |
| 0   | EMD_ENABLE   | rw     | 0*,1  | EMD handling enabled<br>If this register is enabled by setting EMVCO_EMD_ENABLE=1, the registers EMD_0_CONFIG and EMD_1_CONFIG is ignored for the EMVCO_EMD function.  |

### 9.25.6 FELICA\_EMD\_CONTROL (0004h)

Table 25. FELICA\_EMD\_CONTROL register (address 0004h) bit description

| Bit   | Symbol                     | Access | setting for FeliCa EMD handling | Value | Description   |
|-------|----------------------------|--------|---------------------------------|-------|---|
| 31:24 | FELICA_EMD_RC_BYTE_VALUE   | rw     | 0                               | 0*,1  | FeliCa RC byte value that needs to be received does not treat the frame as EMD      |
| 23:16 | FELICA_EMD_LENGTH_BYTE_MAX | rw     | 0                               | 0*,1  | Maximum Length byte value that needs to be received does not treat the frame as EMD |
| 15:8  | FELICA_EMD_LENGTH_BYTE_MIN | rw     | 0                               | 0*,1  | Minimum Length byte value that needs to be received does not treat the frame as EMD |
| 7:5   | RESERVED                   | rw     | 0                               | 0*,1  | -   |
| 6     | FELICA_EMD_LOG_ENABLE      | rw     | 0 or 1                          | 0*1   | Log Enable bit to send RX Status during EMD   |

Table 25. FELICA\_EMD\_CONTROL register (address 0004h) bit description...continued

| Bit | Symbol                                    | Access | setting for FeliCa EMD handling | Value | Description  |
|-----|---|--------|---------------------------------|-------|--|
| 5   | FELICA_EMD_RC_CHECK_ON_CRC_CORRECT_ENABLE | rw     | 0 or 1                          | 0*1   | RC byte check enabled for FeliCa EMD handling on complete RF Frame when there is no Integrity Error observed |
| 4   | FELICA_EMD_INTEGRITY_ERR_CHECK_ENABLE     | rw     | 1                               | 0*,1  | FeliCa EMD handling enabled when integrity error is set  |
| 3   | FELICA_EMD_PROTOCOL_ERR_CHECK_ENABLE      | rw     | 1                               | 0*,1  | FeliCa EMD handling enabled when protocol error is set   |
| 2   | FELICA_EMD_RC_CHECK_ENABLE                | rw     | 0                               | 0*,1  | FeliCa RC byte check enabled for FeliCa EMD handling   |
| 1   | FELICA_EMD_LEN_CHECK_ENABLE               | rw     | 0                               | 0*,1  | FeliCa Length byte check enabled for FeliCa EMD handling   |
| 0   | FELICA_EMD_ENABLE                         | rw     | 1                               | 0*,1  | FeliCa EMD handling enabled  |

Recommended value for FeliCa EMD handling: 00FF0019h

9.25.7 RX\_STATUS (0005h)

Table 26. RX\_STATUS register (address 0005h) bit description

| Bit   | Symbol                 | Access | Value | Description  |
|-------|------------------------|--------|-------|--|
| 31:27 | RFU                    | r      | 0*,1  | -  |
| 26:20 | RX_COLL_POS            | r      | 0*,1  | Status indicating the bit position of the first collision detected in the data bit. The value is valid only when RX_COLLISION_DETECTED==1. The value of the RX_BIT_ALIGN is also taken into account (RX_COLL_POS = physical bit position in the flow + RX_BIT_ALIGN value).<br><br>Indicates the collision position in the first 8 bytes only. Can be used during the TypeA/ICODE/EPC anti-collision procedure. 0x00 - first bit 0x01 - second bit... 0x7F - 128th bit.<br><br>The status register is not updated by the collision detected on stop or parity bit. |
| 19:17 | RX_NUM_LAST_BITS       | r      | 0*,1  | Indicating the number of valid bits in the last byte received.<br><br>0: all bits are valid<br>1: 1 bit is valid<br>....<br>7: - 7 bits are valid<br><br>This is generally used during ISO/IEC14443 type A anti-collision  |
| 16:13 | RX_NUM_FRAMES_RECEIVED | r      | 0*,1  | Indicates the number of frames received. The value is updated after every normal frame reception in RX_MULTIPLE mode.  |

Table 26. RX\_STATUS register (address 0005h) bit description...continued

| Bit  | Symbol                | Access | Value | Description  |
|------|-----------------------|--------|-------|--|
|      |                       |        |       | The value is valid only if the bit RX_MULTIPLE_ENABLE=='1'.  |
| 12:0 | RX_NUM_BYTES_RECEIVED | r      | 0*,1  | Number of bytes received on the RF interface. This field is not relevant when RX_MULTIPLE_ENABLE=='1'. |

9.25.8 RX\_STATUS\_ERROR (0006h)

Table 27. RX\_STATUS\_ERROR register (address 0006h) bit description

| Bit   | Symbol                        | Access | Value | Description   |
|-------|-------------------------------|--------|-------|---|
| 31:30 | RFU                           | r      | 0*,1  |   |
| 29    | EMD_DETECTED_IN_RXDEC         | r      | 0*,1  | The high level indicates that the EMD was detected (in the SigPro or in the RxDecoder or in both) during the reception.       |
| 28    | EMD_DETECTED_IN_SIGPRO        | r      | 0*,1  | The high level indicates that the EMD was detected on the Physical layer (in the SigPro) during the reception.                |
| 27    | EXT_RFOFF_DETECTED            | r      | 0*,1  | The high level indicates that the external RF-field vanished during the reception   |
| 26    | RX_FRAME_MAXLEN_VIOL          | r      | 0*,1  | The high level indicates that the received frame length violated the configured maximum limit                                 |
| 25    | RX_FRAME_MINLEN_VIOL          | r      | 0*,1  | The high level indicates that the received frame length violated the configured minimum limit.                                |
| 24    | RX_FRAME_LE_CRC               | r      | 0*,1  | The high level indicates that the received frame length is less or equal to the expected CRC field length.                    |
| 23    | RX_NOT_FULL_BYTE              | r      | 0*,1  | The high level indicates that the last received character in the frame has less than 8 bits.                                  |
| 22    | RX_MISSING_PARBIT_DETECTED    | r      | 0*,1  | The high level indicates that the last received character in the frame has 8 data bits but the expected parity bit is absent. |
| 21    | RX_MISSING_STOPBIT_DETECTED   | r      | 0*,1  | The high level indicates that the last received character in the frame has 8 data bits but the expected stop bit is absent.   |
| 20    | RX_COLLISION_PARBIT_DETECTED  | r      | 0*,1  | The high level indicates that the collision was detected on the parity bit position.  |
| 19    | RX_COLLISION_STOPBIT_DETECTED | r      | 0*,1  | The high level indicates that the collision was detected on the stop bit position.  |
| 18    | RX_COLLISION_DETECTED         | r      | 0*,1  | The high level indicates that the collision was detected during the frame reception.  |
| 17    | RX_STOP_ON_RXOVER             | r      | 0*,1  | The high level indicates that the frame reception was stopped by SGP_MSG_RXOVER_* message reception.                          |
| 16    | RX_STOP_ON_RFOFF              | r      | 0*,1  | The high level indicates that the frame reception was interrupted by external RF-field vanishing event.                       |

Table 27. RX\_STATUS\_ERROR register (address 0006h) bit description...continued

| Bit | Symbol               | Access | Value | Description  |
|-----|----------------------|--------|-------|--|
| 15  | RX_STOP_ON_ERR       | r      | 0*,1  | The high level indicates that the frame reception was stopped by detected communication error event.   |
| 14  | RX_STOP_ON_LEN       | r      | 0*,1  | The high level indicates that the frame reception was normally stopped by byte counter expiration event. Relates to the protocols where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM).  |
| 13  | RX_STOP_ON_INVPAR    | r      | 0*,1  | The high level indicates that the frame reception was normally stopped by the inverted parity detection event. Relates to the TypeA RM 212-848 kbit/s modes.   |
| 12  | RX_STOP_ON_PATTERN   | r      | 0*,1  | The high level indicates that the frame reception was normally stopped by EOF pattern detection event. Relates to the TypeB RM/CM, B prime RM/CM modes.  |
| 11  | RX_STOP_ON_ANTICOLL  | r      | 0*,1  | The high level indicates that the frame reception was normally stopped by collision detected on data bit position. Relates to the bit-oriented frame reception in TypeA RM 106 kbit/s mode during the anti-collision procedure.  |
| 10  | RX_CRC_ERROR         | r      | 0*,1  | The high level indicates that the CRC error is detected in the received frame.   |
| 9   | RX_LEN_ERROR         | r      | 0*,1  | The high level is set if the received frame is shorter than the length stated in the received frame LEN field OR if the LEN parameter in the received frame violates the configured [RX_FRAME_MINLEN:RX_FRAME_MAX LEN] limits. Can assert only in the mode where the LEN field is used in the frame format (FeliCa RM/CM, FWEC RM/CM). |
| 8   | RX_SIGPRO_ERROR      | r      | 0*,1  | The high level indicates that the communication error/errors were detected during the frame reception on physical layer(in the SigPro).  |
| 7   | RX_PARITY_ERROR      | r      | 0*,1  | The high level indicates that the parity error was detected during the frame reception.  |
| 6   | RX_STOPBIT_ERROR     | r      | 0*,1  | The high level indicates that the stop bit error ('0' level instead of '1' on the stop bit position) was detected during the frame reception.  |
| 5   | RX_WRITE_ERROR       | r      | 0*,1  | The high level indicates that the error acknowledge status was received on the CLIF-system interface during the received frame transmission to the System RAM.   |
| 4   | RX_BUFFER_OVFL_ERROR | r      | 0*,1  | The high level indicates that the data payload length in the received frame exceeds the 28 bytes limit. Relates to the PollReq procedure in the FeliCa RM mode only.   |
| 3   | RX_LATENCY_ERROR     | r      | 0*,1  | The high level indicates that the write request flow was corrupted due to traffic congestion on  |

Table 27. RX\_STATUS\_ERROR register (address 0006h) bit description...continued

| Bit | Symbol                  | Access | Value | Description  |
|-----|-------------------------|--------|-------|--|
|     |                         |        |       | the system interface during the received frame transmission to the System RAM.   |
| 2   | RX_DATA_INTEGRITY_ERROR | r      | 0*,1  | The high level indicates that the data integrity corruption (parity/CRC/etc error) was detected in the received frame.   |
| 1   | RX_PROTOCOL_ERROR       | r      | 0*,1  | The high level indicates that the protocol requirements violation (stop bit error, missing parity bit, not full byte received, etc.) was detected in the received frame. |
| 0   | RX_CL_ERROR             | r      | 0*,1  | The high level indicates that some protocol/data integrity error/errors were detected during the frame reception   |

### 9.25.9 CLIF\_STATUS (0007h)

Table 28. CLIF\_STATUS register (address 0007h) bit description

| Bit   | Symbol                | Access | Value | Description   |
|-------|-----------------------|--------|-------|---|
| 31:30 | RFU                   | r      | 0*,1  | -   |
| 29    | CRC_OK                | r      | 0*,1  | This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct. meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only be evaluated at the end of a communication |
| 28    | RX_SC_DETECTED        | r      | 0*,1  | Status signal indicating that a subcarrier is detected.   |
| 27    | RX_SOF_DETECTED       | r      | 0*,1  | Status signal indicating that a SOF has been detected.  |
| 26    | TX_RF_STATUS          | r      | 0*,1  | If set to 1 this bit indicates that the drivers are turned on. meaning an RF-Field is created by the device itself.   |
| 25    | RF_DET_STATUS         | r      | 0*,1  | If set to 1 this bit indicates that an external RF-Field is detected by the RF level detectors (after digital filtering)  |
| 24    | ADC_Q_CLIPPING        | r      | 0*,1  | Indicates that the Q-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).   |
| 23    | ADC_I_CLIPPING        | r      | 0*,1  | Indicates that the I-Channel ADC has clipped (value 0 or 63), This bit is reset with Rx-reset (enabling of receiver).   |
| 22:12 | RFU                   | r      | 0*,1  | -   |
| 11    | TX_NO_DATA_ERROR      | r      | 0*,1  | This error flag is set to 1. in case a transmission is started but no data is available (register NumBytesToSend == 0).   |
| 10:8  | RF_ACTIVE_ERROR_CAUSE | r      | 0*,1  | This status flag indicates the cause of an NFC-Active error.<br>Note: These bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1. 0*  |

Table 28. CLIF\_STATUS register (address 0007h) bit description...continued

| Bit | Symbol            | Access | Value | Description   |
|-----|-------------------|--------|-------|---|
|     |                   |        |       | No Error. reset value 1 External field was detected on within TIDT timing 2 External field was detected on within TADT timing 3 No external field was detected within TADT timings 4 Peer did switch off RF Field without but no RX event was raised (no data received) 5 - 7 Reserved. |
| 7:6 | RFU               | r      | 0*,1  | -   |
| 5   | RX_ENABLE         | r      | 0*,1  | This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled and is now ready for data reception  |
| 4   | TX_ACTIVE         | r      | 0*,1  | This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing otherwise the TxEncoder is in idle state.  |
| 3   | RX_ACTIVE         | r      | 0*,1  | This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing. otherwise the RxDecoder is in idle state.   |
| 2:0 | RF_EXCHANGE_STATE | r      | 0*,1  | These registers hold the command bits<br>0* IDLE state<br>1 WaitTransmit state<br>2 Transmitting state<br>3 WaitReceive state<br>4 WaitForData state<br>5 Receiving state<br>6 LoopBack state<br>7 reserved   |

### 9.25.10 TRANSCEIVE\_CONTROL (0008h)

To meet the ISO14443A FDT with an accuracy of 1 carrier clock cycle, there is support implemented to synchronize the guard time prescaler to the modified Miller envelope pulses (end of pulse). For adjustment, there is a 7-bit wide configuration register - TX\_BITPHASE - which allows to adjust the FDT in the range of 0 to 128 carrier clock cycles. As defined in the ISO14443 the adjustment is different, depending on the data bit value of the data stream. For correct bit grid calculation, the prescaler must be set to a value corresponding exactly to one etu - for 106 kbit/s this corresponds to 0x7F. Otherwise the FdT will be incorrect.

Table 29. TRANSCEIVE\_CONTROL register (address 0008h) bit description

| Bit   | Symbol             | Access | Value | Description  |
|-------|--------------------|--------|-------|--|
| 31:16 | RFU                | r      | 0*,1  | -  |
| 15:8  | TX_BITPHASE        | r/w    | 0*,1  | Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is applicable for CardMode only. |
| 7:3   | RFU                | r/w    | 0*,1  | -  |
| 2     | RX_MULTIPLE_ENABLE | r/w    | 0*,1  | If this bit is set to 1. the receiver is reactivated after the end of a reception.   |
| 1:0   | RFU                | r/w    | 0*,1  | -  |



### 9.25.11 TX\_SYMBOL01\_MOD (0009h)

Table 30. TX\_SYMBOL01\_MOD register (address 0009h) bit description

| Bit   | Symbol               | Access | Value | Description  |
|-------|----------------------|--------|-------|--|
| 31:24 | RFU                  | rw     | 0*,1  | -  |
| 23:16 | TX_S01_MODWIDTH      | rw     | 0*,1  | Specifies the length of a pulse for sending data of symbol 0/1. The length is given by the number of carrier clocks + 1.   |
| 15:9  | RFU                  | rw     | 0*,1  | -  |
| 8     | TX_S01_MILLER_ENABLE | rw     | 0*,1  | If set to 1. pulse modulation is applied according to modified miller coding.  |
| 7     | TX_S01_INV_ENV       | rw     | 0*,1  | If set to 1. the output envelope is inverted.  |
| 6:4   | TX_S01_ENV_TYPE      | rw     | 0*,1  | Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tupple 111b RFU. |
| 3     | TX_S01_SC_FREQ       | rw     | 0*,1  | Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz   |
| 2:0   | TX_S01_BIT_FREQ      | rw     | 0*,1  | Specifies the frequency of the bit-stream.<br>000b -> 1.695 MHz.<br>001b -> Reserved.<br>010b -> 26 kHz.<br>011b -> 53 kHz.<br>100b -> 106 kHz.<br>101b -> 212 kHz.<br>110b -> 424 kHz.<br>111b -> 848 kHz.  |

### 9.25.12 TX\_SYMBOL1\_DEF (000Ah)

Table 31. TX\_SYMBOL1\_DEF register (address 000Ah) bit description

| Bit  | Symbol         | Access | Value | Description                    |
|------|----------------|--------|-------|--------------------------------|
| 31:0 | TX_SYMBOL1_DEF | rw     | 0*,1  | Pattern definition for Symbol1 |

### 9.25.13 TX\_SYMBOL0\_DEF (000Bh)

Table 32. TX\_SYMBOL0\_DEF register (address 000Bh) bit description

| Bit  | Symbol         | Access | Value | Description                    |
|------|----------------|--------|-------|--------------------------------|
| 31:0 | TX_SYMBOL0_DEF | rw     | 0*,1  | Pattern definition for Symbol0 |

9.25.14 TX\_SYMBOL23\_MOD (000Ch)

Table 33. TX\_SYMBOL23\_MOD register (address 000Ch) bit description

| Bit   | Symbol               | Access | Value | Description  |
|-------|----------------------|--------|-------|--|
| 31:24 | RFU                  | r      | 0*,1  | -  |
| 23:16 | TX_S23_MODWIDTH      | r/w    | 0*,1  | Specifies the length of a pulse for sending data of symbol 2/3. The length is given by the number of carrier clocks + 1.   |
| 15:9  | RFU                  | r/w    | 0*,1  | -  |
| 8     | TX_S23_MILLER_ENABLE | r/w    | 0*,1  | If set to 1 pulse modulation is applied according to modified miller coding  |
| 7     | TX_S23_INV_ENV       | r/w    | 0*,1  | If set to 1 the output envelope is inverted.   |
| 6:4   | TX_S23_ENV_TYPE      | r/w    | 0*,1  | Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ (pulse of half bit length at beginning of bit) 110b Manchester tuple 111b RFU |
| 3     | TX_S23_SC_FREQ       | r/w    | 0*,1  | Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz   |
| 2:0   | TX_S23_BIT_FREQ      | r/w    | 0*,1  | Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz.  |

9.25.15 TX\_SYMBOL23\_DEF (000Dh)

Table 34. TX\_SYMBOL23\_DEF register (address 000Dh) bit description

| Bit   | Symbol         | Access | Value          | Description                    |
|-------|----------------|--------|----------------|--------------------------------|
| 31:24 | RFU            | r      | 0*,1           | -                              |
| 23:16 | TX_SYMBOL3_DEF | r/w    | 0*,1           | Pattern definition for Symbol3 |
| 15:8  | RFU            | r/w    | 0*,1           | -                              |
| 7:0   | TX_SYMBOL2_DEF | r/w    | 0000h* - FFFFh | Pattern definition for Symbol2 |

9.25.16 TX\_SYMBOL\_CONFIG (000Eh)

Table 35. TX\_SYMBOL\_CONFIG register (address 000Eh) bit description

| Bit   | Symbol               | Access | Value          | Description  |
|-------|----------------------|--------|----------------|--|
| 31    | RFU                  |        | 0*,1           | -  |
| 30:27 | TX_SYMBOL1_BURST_LEN | r/w    | 0000h* - FFFFh | Specifies the number of bits issued for symbol 1 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit |

Table 35. TX\_SYMBOL\_CONFIG register (address 000Eh) bit description...continued

| Bit   | Symbol                  | Access | Value | Description  |
|-------|-------------------------|--------|-------|--|
| 26    | TX_SYMBOL1_BURST_TYPE   | r/w    | 0*,1  | Specifies the type of the burst of Symbol1 (logical zero / logical one)  |
| 25    | TX_SYMBOL1_BURST_ONLY   | r/w    | 0*,1  | If set to 1. Symbol1 consists only of a burst and no symbol pattern  |
| 24    | TX_SYMBOL1_BURST_ENABLE | r/w    | 0*,1  | If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL1_BURST_LEN is enabled  |
| 23    | RFU                     | r      | 0*,1  | -  |
| 22:19 | TX_SYMBOL0_BURST_LEN    | r/w    | 0*,1  | Specifies the number of bits issued for symbol 0 burst. The 3 bits encode a range from 8 to 256 bit length: 0000b 8 bit 0001b 12 bit 0010b 16 bit 0011b 24 bit 0100b 32 bit 0101b 40 bit 0110b 48 bit 0111b 64 bit 1000b 80 bit 1001b 96 bit 1010b 112 bit 1011b 128 bit 1100b 160 bit 1101b 192 bit 1110b 224 bit 1111b 256 bit |
| 18    | TX_SYMBOL0_BURST_TYPE   | r/w    | 0*,1  | Specifies the type of the burst of Symbol0 (logical zero / logical one)  |
| 17    | TX_SYMBOL0_BURST_ONLY   | r/w    | 0*,1  | If set to 1. Symbol0 consists only of a burst and no symbol pattern  |
| 16    | TX_SYMBOL0_BURST_ENABLE | r/w    | 0*,1  | If set to 1. the burst of Symbol0 of the length defined in bit field SYMBOL0_BURST_LEN is enabled  |
| 15:13 | TX_SYMBOL3_LEN          | r/w    | 0*,1  | Specifies the number of valid bits of the symbol definition of Symbol3. The range is from 1 bit (value 0000) to 8 bit (value 111)  |
| 12:10 | TX_SYMBOL2_LEN          | r/w    | 0*,1  | Specifies the number of valid bits of the symbol definition of Symbol2. The range is from 1 bit (value 0000) to 8 bit (value 111)  |
| 9:5   | TX_SYMBOL1_LEN          | r/w    | 0*,1  | Specifies the number of valid bits of the symbol definition of Symbol1. The range is from 1 bit (value 0000) to 31 bits (value 11110)  |
| 4:0   | TX_SYMBOL0_LEN          | r/w    | 0*,1  | Specifies the number of valid bits of the symbol definition of Symbol0. The range is from 1 bit (value 0000) to 31 bits (value 11110)  |

### 9.25.17 TX\_FRAME\_CONFIG (000Fh)

Table 36. TX\_FRAME\_CONFIG register (address 000Fh) bit description

| Bit   | Symbol            | Access | Value | Description   |
|-------|-------------------|--------|-------|---|
| 31:19 | RFU               | r      | 0*,1  | -   |
| 18:16 | TX_DATA_CODE_TYPE | r/w    | 0*,1  | Specifies the type of encoding of data to be used<br>000b No special code 001b 1 out of 4 code [ICODE SLI] 010b 1 out of 256 code [ICODE SLI] 011b Pulse interval encoding (PIE) [ICODE EPC-V2] 100b 2bit tuple code (intended only for test purpose) 101-111b Reserved |
| 15:13 | TX_STOPBIT_TYPE   | r/w    | 0*,1  | Enables the stop bit (logic 1) and extra guard time (logic 1). The value 0 disables transmission of stop-bits. 000b no stop-bit. no EGT 001b stop-bit. no EGT   |

Table 36. TX\_FRAME\_CONFIG register (address 000Fh) bit description...continued

| Bit | Symbol                    | Access | Value | Description   |
|-----|---------------------------|--------|-------|---|
|     |                           |        |       | 010b stop-bit + 1 EGT 011b stop-bit + 2 EGT 100b stop-bit + 3 EGT 101b stop-bit + 4 EGT 110b stop-bit + 5 EGT 111b stop-bit + 6 EGT   |
| 12  | TX_STARTBIT_ENABLE        | r/w    | 0*,1  | If set to 1. a start-bit (logic 0) will be sent   |
| 11  | TX_MSB_FIRST              | r/w    | 0*,1  | If set to 1. data bytes are interpreted MSB first for data transmission   |
| 10  | TX_PARITY_LAST_INV_ENABLE | r/w    | 0*,1  | If set to 1. the parity bit of last sent data byte is inverted  |
| 9   | TX_PARITY_TYPE            | r/w    | 0*,1  | Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated   |
| 8   | TX_PARITY_ENABLE          | r/w    | 0*,1  | If set to 1. a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero. then a NO_DATA_ERROR occurs. |
| 7:5 | RFU                       | r      | 0*,1  | -   |
| 4   | TX_DATA_ENABLE            | r/w    | 0*,1  | If set to 1. transmission of data is enabled otherwise only symbols are transmitted.  |
| 3:2 | TX_STOP_SYMBOL            | r/w    | 0*,1  | Defines which pattern symbol is sent as frame stop-symbol 00b No symbol is sent 01b Symbol1 is sent 10b Symbol2 is sent 11b Symbol3 is sent   |
| 1:0 | TX_START_SYMBOL           | r/w    | 0*,1  | Defines which symbol pattern is sent as frame start-symbol 00b No symbol pattern is sent 01b Symbol0 is sent 10b Symbol1 is sent 11b Symbol2 is sent                                |

9.25.18 TX\_DATA\_MOD (0010h)

Table 37. TX\_DATA\_MOD register (address 0010h) bit description

| Bit   | Symbol                        | Access | Value | Description  |
|-------|-------------------------------|--------|-------|--|
| 31:25 | RFU                           | r      | 0*,1  | -  |
| 24    | TX_ICODE_DATA_MODWIDTH_ENABLE | r/w    | 0*,1  | Enables modulation width of icode data. Width of modulation is defined by the TX_DATA_MODWIDTH field. When 1, we should have TX_DATA_ENV_TYPE=0 and TX_DATA_INV_ENV=0  |
| 23:16 | TX_DATA_MODWIDTH              | r/w    | 0*,1  | Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1.  |
| 15:9  | RFU                           | r      | 0*,1  | -  |
| 8     | TX_DATA_MILLER_ENABLE         | r/w    | 0*,1  | If set to 1 pulse modulation is applied according to modified miller coding  |
| 7     | TX_DATA_INV_ENV               | r/w    | 0*,1  | If set to 1 the output envelope is inverted  |
| 6:4   | TX_DATA_ENV_TYPE              | r/w    | 0*,1  | Specifies the type of envelope used for transmission of data packets. The selected envelope type is applied to the pseudo bit stream. 000b Direct output 001b Manchester code 010b Manchester code with subcarrier 011b BPSK 100b RZ (pulse of half bit length at beginning of second half of bit) 101b RZ |

Table 37. TX\_DATA\_MOD register (address 0010h) bit description...continued

| Bit | Symbol           | Access | Value | Description   |
|-----|------------------|--------|-------|---|
|     |                  |        |       | (pulse of half bit length at beginning of bit) 110b Manchester tupple coding 111b RFU   |
| 3   | TX_DATA_SC_FREQ  | r/w    | 0*,1  | Specifies the frequency of the subcarrier. 0 424 kHz 1 848 kHz  |
| 2:0 | TX_DATA_BIT_FREQ | r/w    | 0*,1  | Specifies the frequency of the bit-stream. 000b -> 1.695 MHz. 001b -> Reserved. 010b -> 26 kHz. 011b -> 53 kHz. 100b -> 106 kHz. 101b -> 212 kHz. 110b -> 424 kHz. 111b -> 848 kHz. |

9.25.19 TX\_WAIT (0011h)

To guarantee correct protocol timing a guard period timer is implemented for the RF\_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time TX\_WAIT is started after the end of a reception no matter if the frame is correct or erroneous.

It is not started in case the reception is restarted because of an EMD-event or in case the RX\_MULTIPLE\_ENABLE bit is set to 1 the TX\_WAIT.

In case the register flag TX\_WAIT\_RFON\_ENABLE is set to 1 the guard time timer is started when the devices own RF-Field was switched on.

It is possible to disable the guard time tx\_wait by setting the register TX\_WAIT\_VALUE to 00h.

TX\_WAIT can be used for 2 different purposes:

1. It can be used to prevent start of transmission before a certain period has expired - even if FW already finished data processing and set the START\_SEND bit. This behavior is mainly intended for reader mode to guaranteed PICC to PCD frame delay time (FDT).
2. TX\_WAIT time can be used to start the transmission at an exactly defined time.

Table 38. TX\_CLIF\_WAIT register (address 0011h) bit description

| Bit   | Symbol            | Access | Value | Description   |
|-------|-------------------|--------|-------|---|
| 31:28 | RFU               | r      | 0*,1  | -   |
| 27:8  | TX_WAIT_VALUE     | r/w    | 0*,1  | Defines the tx_wait timer reload value. Note: If set to 00000h the tx_wait timer guard time is disabled<br>Note: This bit is set by HW a protocol is detected in automatic mode detection |
| 0     | TX_WAIT_PRESCALER | r/w    | 0*,1  | Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detection  |

9.25.20 TX\_CRC\_CONFIG (0012h)

Table 39. TX\_CRC\_CONFIG (address 0012h) bit description

| Bit   | Symbol              | Access | Value    | Description  |
|-------|---------------------|--------|----------|--|
| 31:16 | TX_CRC_PRESET_VALUE | r/w    | 0*-FFFFh | Arbitrary preset value for the TX-Encoder CRC calculation. |

Table 39. TX\_CRC\_CONFIG (address 0012h) bit description...continued

| Bit  | Symbol              | Access | Value    | Description   |
|------|---------------------|--------|----------|---|
| 15:7 | RFU                 | r/w    | 0        | Reserved  |
| 6    | TX_CRC_BYTE2_ENABLE | r/w    | 0*,1     | If set; the CRC is calculated from the second byte onwards (intended for HID). This option is used in the TX-Encoder. |
| 5:3  | TX_CRC_PRESET_SEL   | r/w    | 000-101b | Preset values of the CRC register for the TX-Encoder. For a CRC calculation using 5 bits, only the LSByte is used.    |
|      |                     |        | 000b*    | 0000h, reset value  |
|      |                     |        | 001b     | 6363h   |
|      |                     |        | 010b     | A671h   |
|      |                     |        | 011b     | FFFFh   |
|      |                     |        | 100b     | 0012h   |
|      |                     |        | 101b     | E012h   |
|      |                     |        | 110b     | RFU   |
| 2    | TX_CRC_TYPE         | r/w    | 0*,1     | Controls the type of CRC calculation for the TX-Encoder   |
|      |                     |        | 0*       | 16-bit CRC calculation, reset value   |
|      |                     |        | 1        | 5-bit CRC calculation   |
| 1    | TX_CRC_INV          | r/w    | 0*,1     | Controls the sending of an inverted CRC value by the TX-Encoder   |
|      |                     |        | 0*       | Not inverted CRC checksum, reset value  |
|      |                     |        | 1        | Inverted CRC checksum   |
| 0    | TX_CRC_ENABLE       | r/w    | 0*, 1    | If set to one, the TX-Encoder computes and transmits a CRC.   |

### 9.25.21 SS\_TX\_CONFIG (00015h)

Table 40. SS\_TX\_CONFIG register (address 00015h) bit description

| Bit   | Symbol               | Access | Value | Description   |
|-------|----------------------|--------|-------|---|
| 31:14 | RFU                  | r      | 0*,1  | -   |
| 13    | TX2_USE_TX1_CONF     | r/w    | 0*,1  | When 1, the tx1 configuration is used also for tx2: all SS_TX2_* registers are discarded and configurations from corresponding SS_TX1_* register is used. |
| 12:6  | RFU                  | r/w    | 0*,1  | -   |
| 5:3   | TX2_CLK_MODE_DEFAULT | r/w    | 0*,1  | TX2 clk mode without field (RM and CM)  |
| 2:0   | TX1_CLK_MODE_DEFAULT | r/w    | 0*,1  | TX1 clk mode without field (RM and CM)  |

There are 5 choices for the RF output stage behavior during 100 % modulation, and one setting for 10 % modulation. The antenna driver TX1 clk mode and TX2 clk mode are possible to be configured as such:

Table 41. Settings for Antenna drivers TX1 and TX2

| TX_CLK_MODE_RM (binary) | Tx1 and TX2 output | Remarks   |
|-------------------------|--------------------|---|
| 000                     | High-impedance     | High-impedance of the transmitters (field-off)            |
| 001                     | 0                  | Output pulled to 0 in any case                            |
| 010                     | 1                  | Output pulled to 1 in any case                            |
| 110                     | RF high side push  | Open-drain, only high side (push) MOS supplied with clock |
| 101                     | RF low side pull   | Open-drain, only low side (pull) MOS supplied with clock  |
| 111                     | 13.56 MHz clock    | Push/pull operation                                       |

### 9.25.22 SS\_TX1\_RMCFG (00016h)

Table 42. SS\_TX1\_RMCFG register (address 00016h) bit description

| Bit   | Symbol                | Access | Value | Description   |
|-------|-----------------------|--------|-------|---|
| 31:25 | RFU                   | r      | 0*,1  | -   |
| 24:22 | TX1_CLK_MODE_TRANS_RM | r/w    | 0*,1  | TX1 clock mode in RM during transition  |
| 21:19 | TX1_CLK_MODE_MOD_RM   | r/w    | 0*,1  | TX1 clock mode of modulated wave in RM<br>000: TX1=High-Z<br>001: TX1=VSS_PA<br>010 - 110: RFU<br>111: TX1 clocked normal operation |
| 18:16 | TX1_CLK_MODE_CW_RM    | r/w    | 0*,1  | TX1 clock mode of modulated wave in RM<br>000: TX1=High-Z<br>001: TX1=VSS_PA<br>010 - 110: RFU<br>111: TX1 clocked normal operation |
| 15:8  | TX1_AMP_MOD_RM        | r/w    | 0*,1  | TX1 amplitude of modulated wave in RM ( 0x00 = 0% modulation, 0xFF: 100% modulation)  |
| 7:0   | TX1_AMP_CW_RM         | r/w    | 0*,1  | TX1 amplitude of unmodulated wave in RM ( 0x00 = 0% signal, 0xFF: 100% signal)  |

### 9.25.23 SS\_TX2\_RMCFG (00017h)

These settings for TX\_2 are only applied, if the bit 13 in TX\_CONFIG (TX2\_USE\_TX1\_CONF is set to 0.

Table 43. SS\_TX2\_RMCFG register (address 00017h) bit description

| Bit   | Symbol                | Access | Value | Description   |
|-------|-----------------------|--------|-------|---|
| 31:25 | RFU                   | r      | 0*,1  | -   |
| 24:22 | TX2_CLK_MODE_TRANS_RM | r/w    | 0*,1  | TX2 clock mode in RM during transition  |
| 21:19 | TX2_CLK_MODE_MOD_RM   | r/w    | 0*,1  | TX2 clock mode of modulated wave in RM<br>000: TX2=High-Z<br>001: TX2=VSS_PA<br>010 - 110: RFU<br>111: TX2 clocked normal operation |
| 18:16 | TX2_CLK_MODE_CW_RM    | r/w    | 0*,1  | TX2 clock mode of modulated wave in RM  |

Table 43. SS\_TX2\_RMCFG register (address 0017h) bit description...continued

| Bit  | Symbol         | Access | Value | Description   |
|------|----------------|--------|-------|---|
|      |                |        |       | 000: TX2=High-Z<br>001: TX2=VSS_PA<br>010 - 110: RFU<br>111: TX2 clocked normal operation |
| 15:8 | TX2_AMP_MOD_RM | r/w    | 0*,1  | TX2 amplitude of modulated wave in RM ( 0x00 = 0% modulation, 0xFF: 100% modulation)      |
| 7:0  | TX2_AMP_CW_RM  | r/w    | 0*,1  | TX2 amplitude of unmodulated wave in RM ( 0x00 = 0% signal, 0xFF: 100% signal)            |

### 9.25.24 SS\_TX\_TRANS\_CFG (00019h)

Table 44. SS\_TX\_TRANS\_CFG register (address 0019h) bit description

| Bit   | Symbol              | Access | Value | Description   |
|-------|---------------------|--------|-------|---|
| 31:12 | RFU                 | rw     | 0*,1  | -   |
| 11    | TX2_SS_TRANS_RATE   | rw     | 0*,1  | TX2 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM.              |
| 10    | TX1_SS_TRANS_RATE   | rw     | 0*,1  | TX1 shaping edge rate: 0: 1/fc, 1: 2/fc. 1/fc should be selected for CM               |
| 9:5   | TX2_SS_TRANS_LENGTH | rw     | 0*,1  | TX2 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid |
| 4:0   | TX1_SS_TRANS_LENGTH | rw     | 0*,1  | TX1 shaping edge length: from 0 (disable) to 16. for CM, only 0 or 4 values are valid |

### 9.25.25 SIGPRO\_CONFIG (001Dh)

Table 45. SIGPRO\_RM\_CONFIG register (address 001Fh) bit description

| Bit    | Symbol          | Access | Value | Description                          |
|--------|-----------------|--------|-------|--------------------------------------|
| 31     | DGRM_SOFT_RESET | r/w    | 0*,1  | When high (1) resets the DGRM block. |
| 30...0 | RFU             | r/w    | 0*,1  | -                                    |

### 9.25.26 SIGPRO\_RM\_PATTERN (0020h)

Table 46. SIGPRO\_RM\_PATTERN register (address 0020h) bit description

| Bit   | Symbol               | Access | Value | Description   |
|-------|----------------------|--------|-------|---|
| 31:16 | RM_SYNC_PATTERN      | r/w    | 0*,1  | Sync pattern for FeliCa. LSB transmitted last                                       |
| 15    | RM_SYNC_PATTERN_EXT4 | r/w    | 0*,1  | Extend FeliCa sync pattern with 16 leading 0s                                       |
| 14    | RM_SYNC_PATTERN_EXT2 | r/w    | 0*,1  | Extend FeliCa sync pattern with 8 leading 0s  |
| 13    | RM_RECEIVE_TILL_END  | r/w    | 0*,1  | Do not stop the reception before RxDecoder sends a stop command.                    |
| 12    | RFU                  | r      | 0*,1  | -   |
| 11:0  | RM_SOF_PATTERN       | r/w    | 0*,1  | SOF pattern for Type B. LSB transmitted last or Start Byte pattern for NFC passive. |



## 9.25.27 SIGPRO\_RM\_TECH (0022h)

Table 47. SIGPRO\_RM\_TECH register (address 0022h) bit description

| Bit   | Symbol     | Access | Value | Description  |
|-------|------------|--------|-------|--|
| 31:17 | RFU        | rw     | 0     | -  |
| 16:15 | RM_MF_GAIN | rw     | 0     | Defines the gain of the Matched-Filters<br>00: Minimum Gain,<br>11: Maximum Gain |
| 14:0  | RFU        | rw     | 0     | -  |

## 9.25.28 RX\_PROTOCOL\_CONFIG (0025h)

Table 48. RX\_PROTOCOL\_CONFIG register (address 0025h) bit description

| Bit  | Symbol           | Access | Value | Description  |
|------|------------------|--------|-------|--|
| 31:6 | RFU              | r      | 0*,1  | -  |
| 5:3  | RX_BIT_ALIGN     | r/w    | 0*,1  | Defines the position of the 1st received data bit in the formed data byte.000b - 0 position...111b - 7th position  |
| 2    | RX_PARITY_TYPE   | r/w    | 0*,1  | 0 - data + parity bits contain even number of "1". 1 - data + parity bits contain odd number of "1". Valid if <code>cfg_rx_parity_enable_i == 1</code> . |
| 1    | RX_PARITY_ENABLE | r/w    | 0*,1  | If set to '1', the bit following last data bit in the frame character is considered as parity bit.   |
| 0    | RFU              | r/w    | 0*,1  | -  |

## 9.25.29 RX\_FRAME\_LENGTH (0026h)

Table 49. RX\_FRAME\_LENGTH register (address 0026h) bit description

| Bit   | Symbol          | Access | Value | Description  |
|-------|-----------------|--------|-------|--|
| 31    | RFU             | r      | 0*,1  | -  |
| 30:16 | RX_FRAME_MAXLEN | r/w    | 0*,1  | Maximal number of received [DATA + CRC] bits in the frame. The violation of the maximum length limit can be also configured as an Error/EMD condition. If the max length violation is configured as error - the frame reception is stopped in case of maximum length limit exceeding. Otherwise the reception is continued.<br>0x0000 - 1 bit...0x7FFF - 32 kbit |
| 15    | RFU             | r      | 0*,1  | -  |
| 14:0  | RX_FRAME_MINLEN | r/w    | 0*,1  | Minimal number of received [DATA + CRC] bits in the frame. The violation of the minimum length limit can be also configured as an Error/EMD condition. The parameter also defines the number of received[DATA + CRC] bits before which any of the EOF patterns or INVPAR stop condition events are ignored.0x0000 - 1 bit...0x7FFF - 32 kbit                     |

### 9.25.30 RX\_CTRL\_STATUS (0028h)

Table 50. RX\_CTRL\_STATUS register (address 0028h) bit description

| Bit  | Symbol            | Access | Value | Description         |
|------|-------------------|--------|-------|---------------------|
| 31:9 | RFU               | r      | dyn   | -                   |
| 8:3  | RXCTRL_HF_ATT_VAL | r      | dyn   | HF attenuator value |
| 2:0  | RFU               | r      | dyn   | -                   |

### 9.25.31 SIGPRO\_IIR\_CONFIG0 (002Ah)

Table 51. SIGPRO\_IIR\_CONFIG0 register (address 002Ah) bit description

| Bit  | Symbol     | Access | Value | Description           |
|------|------------|--------|-------|-----------------------|
| 31:1 | RFU        | rw     | 0*,1  | -                     |
| 0    | IIR_ENABLE | rw     | 0*,1  | Enable the IIR filter |

### 9.25.32 DGRM\_BBA (002Dh)

Table 52. DGRM\_BBA register (address 002Dh) bit description

| Bit   | Symbol            | Access | Value | Description  |
|-------|-------------------|--------|-------|--|
| 31:17 | RFU               | r      | 0*,1  | -  |
| 16:14 | DGRM_BBA_MIN_VAL  | r/w    | 0*,1  | Defines the minimum value of BBA gain:<br>5: +24dB<br>4: +18dB<br>3: +12dB<br>2: +6dB<br>1: 0dB<br>0: -6dB |
| 13:11 | DGRM_BBA_MAX_VAL  | r/w    | 0*,1  | Defines the maximum value of BBA gain.<br>5: +24dB<br>4: +18dB<br>3: +12dB<br>2: +6dB<br>1: 0dB<br>0: -6dB |
| 10:8  | DGRM_BBA_INIT_VAL | r/w    | 0*,1  | Defines initial value of BBA gain.<br>5: +24dB<br>4: +18dB<br>3: +12dB<br>2: +6dB<br>1: 0dB<br>0: -6dB     |
| 7:0   | RFU               | r      | 0*,1  | -  |

### 9.25.33 DGRM\_RSSI (0030h)

This register is updated dynamically by the firmware if the DPC is enabled.

Table 53. DGRM\_RSSI register (address 0030h) bit description

| Bit   | Symbol                        | Access | Value | Description  |
|-------|-------------------------------|--------|-------|--|
| 31:30 | RFU                           |        |       | -  |
| 29    | DGRM_SIGNAL_DETECT_TH_OVR     | r/w    | 0*,1  | Enables the override of signal detect threshold. Override value is set based on DGRM_SIGNAL_DETECT_TH_OVR_VAL.   |
| 28:23 | RFU                           | r/w    | 0*,1  | -  |
| 22:17 | DGRM_RSSI_HYST                | r/w    | 0*,1  | Hysteresis value for RSSI target   |
| 16:7  | DGRM_RSSI_TARGET              | r/w    | 0*,1  | RSSI target value  |
| 6:0   | DGRM_SIGNAL_DETECT_TH_OVR_VAL | r/w    | 0*,1  | Defines the override value for signal detect threshold when DGRM_SIGNAL_DETECT_TH_OVR is set. These bits are modified dynamically by the ARC algorithm based on the DPC voltage.<br>Only if the ARC is disabled, the value written during LOAD_RF_CONFIGURATION(0x0D) is retained throughout the RF Field session. |

### 9.25.34 RX\_CRC\_CONFIG (0031h)

Table 54. RX\_CRC\_CONFIG register (address 0031h) bit description

| Bit   | Symbol              | Access | Value | Description   |
|-------|---------------------|--------|-------|---|
| 31:16 | RX_CRC_PRESET_VALUE | r      | 0*,1  | Arbitrary preset value for the Rx-Decoder CRC calculation.  |
| 15:8  | RFU                 | r/w    | 0*,1  | -   |
| 7     | RX_FORCE_CRC_WRITE  | r/w    | 0*,1  | If set, the Rx-Decoder will send to the RAM the CRC bits as well.   |
| 6     | RX_CRC_ALLOW_BITS   | r/w    | 0*,1  | If activated the frame with length $\leq$ CRC_length will be always sent to the System RAM as is, without CRC bits removal.   |
| 5:3   | RX_CRC_PRESET_SEL   | r/w    | 0*,1  | Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits only the LSByte is used.<br>000b* 0000h reset value. Note that this configuration is set by the Mode detector for FeliCa.<br>001b 6363h Note that this configuration is set by the Mode detector for ISO14443 type A.<br>010b A671h<br>011b FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B.<br>100b<br>0012h<br>101b E012h<br>110b RFU 111b Use arbitrary preset value RX_CRC_PRESET_VALUE |
| 2     | RX_CRC_TYPE         | r/w    | 0*,1  | Controls the type of CRC calculation for the Rx-Decoder 0* 16bit CRC calc   |
| 1     | RX_CRC_INV          | r/w    | 0*,1  | Controls the comparison of the CRC checksum for the Rx-Decoder  |

Table 54. RX\_CRC\_CONFIG register (address 0031h) bit description...continued

| Bit | Symbol        | Access | Value | Description   |
|-----|---------------|--------|-------|---|
|     |               |        |       | 0*: Not inverted CRC value: 0000h reset value.<br>Note that this bit is cleared by the Mode detector for ISO14443 type A and FeliCa.<br>1: Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B |
| 0   | RX_CRC_ENABLE |        |       | If set, the Rx-Decoder will check the CRC for correctness.<br>Note that this bit is set by the Mode Detector when ISO14443 type B, or FeliCa (212 kbd or 424 kbd) is detected.  |

9.25.35 RX\_WAIT (0032h)

To guarantee correct protocol timing a guard period timer is implemented for the RF\_EXCHANGE command in reception and transmission mode.

These guard times are not available for Transmit or Receive command.

The guard time RX\_WAIT is started after the end of a transmission. The guard time RX\_WAIT can be disabled by setting the register RX\_WAIT\_VALUE to 00h meaning the receiver is immediately enabled.

Table 55. RX\_WAIT register (address 0032h) bit description

| Bit   | Symbol            | Access | Value | Description   |
|-------|-------------------|--------|-------|---|
| 31:28 | RFU               | r      | 0*,1  | -   |
| 27:8  | RX_WAIT_VALUE     | r/w    | 0*,1  | Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled |
| 7:0   | RX_WAIT_PRESCALER | r/w    | 0*,1  | Defines the prescaler reload value for the rx_wait timer.   |

9.25.36 DCOC\_CONFIG (0033h)

Table 56. DCOC\_CONFIG register (address 0033h) bit description

| Bit   | Symbol              | Access | Value | Description                          |
|-------|---------------------|--------|-------|--------------------------------------|
| 31:22 | RFU                 | rw     | 0*,1  | -                                    |
| 21    | DCOC_CAL_DONE_FORCE | rw     | 0*,1  | forces the signal dcoc_cal_done to 1 |
| 20:0  | RFU                 | rw     | 0*,1  | -                                    |

9.25.37 RXM\_CTRL (0035h)

Table 57. RXM\_CTRL register (address 0035h) bit description

| Bit  | Symbol                      | Access | Value | Description  |
|------|-----------------------------|--------|-------|--|
| 31:3 | RFU                         |        |       | -  |
| 2    | RXM_FRQ_CHECK_PCRM_ENABLE   | r/w    |       | enable frequency check from PCRM   |
| 1    | RXM_FRQ_CHECK_CORDIC_ENABLE | r/w    |       | enable precise frequency check from cordic phase (+/- 1.7 MHz multiples) |
| 0    | RXM_ENABLE                  | r/w    |       | enable the all RxMeasure module  |

### 9.25.38 ANA\_AGC\_DCO\_CTRL (0036h)

Table 58. ANA\_AGC\_DCO\_CTRL register (address 0036h) bit description

| Bit   | Symbol      | Access | Value | Description                          |
|-------|-------------|--------|-------|--------------------------------------|
| 31:25 | RFU         | rw     | 0*,1  | -                                    |
| 24    | RX_DCO_C_EN | rw     | 0*,1  | Enable signal for the DCO coarse DAC |
| 23:4  | RFU         | rw     | 0*,1  | -                                    |
| 3     | RX_DCO_F_EN | rw     | 0*,1  | enable signal for the DCO fine DAC   |
| 2:0   | RFU         | rw     | 0*,1  | -                                    |

### 9.25.39 SS\_TX1\_CMCFG (0003Bh)

Table 59. SS\_TX1\_CMCFG register (address 003Bh) bit description

| Bit   | Symbol              | Access | Reset Value | Description                              |
|-------|---------------------|--------|-------------|--|
| 31:22 | RFU                 | rw     | 0           | -  |
| 21:19 | TX1_CLK_MODE_MOD_CM | rw     | 0           | TX1 clock mode of modulated wave in CM   |
| 18:16 | TX1_CLK_MODE_CW_CM  | rw     | 0           | TX1 clock mode of unmodulated wave in CM |
| 15:8  | TX1_AMP_MOD_CM      | rw     | 0           | TX1 clock mode of modulated wave in CM   |
| 7:0   | TX1_AMP_CW_CM       | rw     | 0xFF        | TX1 clock mode of unmodulated wave in CM |

### 9.25.40 SS\_TX2\_CMCFG (0003Ch)

Table 60. SS\_TX2\_CMCFG register (address 003Ch) bit description

| Bit   | Symbol              | Access | Reset Value | Description                              |
|-------|---------------------|--------|-------------|--|
| 31:22 | RFU                 | rw     | 0           | -  |
| 21:19 | TX2_CLK_MODE_MOD_CM | rw     | 0           | TX2 clock mode of modulated wave in CM   |
| 18:16 | TX2_CLK_MODE_CW_CM  | rw     | 0           | TX2 clock mode of unmodulated wave in CM |
| 15:8  | TX2_AMP_MOD_CM      | rw     | 0           | TX2 clock mode of modulated wave in CM   |
| 7:0   | TX2_AMP_CW_CM       | rw     | 0xFF        | TX2 clock mode of unmodulated wave in CM |

### 9.25.41 TIMER0\_CONFIG (003Dh)

Table 61. TIMER0\_CONFIG register (address 003Dh) bit description

| Bit  | Symbol           | Access | Value | Description   |
|------|------------------|--------|-------|---|
| 31:9 | RFU              | r      | 0*,1  | -   |
| 8    | T0_START_NOW     | r/w    | 0*,1  | T0_START_EVENT: If set. the timer T0 is started immediately                                     |
| 7    | RFU              | r      | 0*,1  | -   |
| 6    | T0_ONE_SHOT_MODE | r/w    | 0*,1  | When set to 1, the counter value does not reload again until the counter value has reached zero |
| 5:3  | T0_PRESCALE_SEL  | r/w    | 0*,1  | Controls input frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL. |

Table 61. TIMER0\_CONFIG register (address 003Dh) bit description ...continued

| Bit | Symbol           | Access | Value | Description   |
|-----|------------------|--------|-------|---|
|     |                  |        |       | 000b - 6.78 MHz counter<br>001b - 3.39 MHz counter<br>010b - 1.70 MHz counter<br>011b - 848 kHz counter<br>100b - 424 kHz counter<br>101b - 212 kHz counter<br>110b - 106 kHz counter<br>111b - 53 kHz counter                                    |
| 2   | T0_MODE_SEL      | r/w    | 0*,1  | Configuration of the timer T0 clock.<br>0b - Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz).<br>1b - Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_PRESCALE_SEL). |
| 1   | T0_RELOAD_ENABLE | r/w    | 0*,1  | If set to<br>0b - the timer T0 will stop on expiration. 0* After expiration the timer T0 will stop counting. i.e. remain zero. reset value.<br>1b - After expiration the timer T0 will reload its preset value and continue counting down.        |
| 0   | T0_ENABLE        | r/w    | 0*,1  | Enables the timer T0  |

9.25.42 TIMER0\_RELOAD (003Eh)

Table 62. TIMER0\_RELOAD register (address 003Eh) bit description

| Bit   | Symbol          | Access | Value | Description                   |
|-------|-----------------|--------|-------|-------------------------------|
| 31:20 | RFU             | r      | 0*,1  | -                             |
| 19:0  | T0_RELOAD_VALUE | r/w    | 0*,1  | Reload value of the timer T0. |

9.25.43 TIMER1\_CONFIG (003Fh)

Timer 1 is typically used for the FDT configuration. Configuration can be done from the host but the associated IRQ is handled by the firmware of the PN5190B1.

Table 63. TIMER1\_CONFIG register (address 003Fh) bit description

| Bit | Symbol                | Access | Value | Description  |
|-----|-----------------------|--------|-------|--|
| 31  | RFU                   | r      | 0*,1  | -  |
| 30  | T1_STOP_ON_RX_STARTED | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when a data reception begins (1st bit is received). |
| 29  | T1_STOP_ON_TX_STARTED | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when a data transmission begins.                    |
| 28  | T1_STOP_ON_RF_ON_EXT  | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field is detected.             |
| 27  | T1_STOP_ON_RF_OFF_EXT | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when the external RF field vanishes.                |

Table 63. TIMER1\_CONFIG register (address 003Fh) bit description ...continued

| Bit   | Symbol                   | Access | Value | Description   |
|-------|--------------------------|--------|-------|---|
| 26    | T1_STOP_ON_RF_ON_INT     | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned on.   |
| 25    | T1_STOP_ON_RF_OFF_INT    | r/w    | 0*,1  | T1_STOP_EVENT: If set. the timer T1 is stopped when the internal RF field is turned off.  |
| 24    | T1_STOP_ON_RX_ENDED      | r/w    | 0*,1  | T1_STOP_EVENT: If set the timer T1 is stopped when an activity on RX is detected.   |
| 23:18 | RFU                      | r      | 0*,1  | -   |
| 17    | T1_START_ON_RX_STARTED   | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when a data reception begins (1st bit is received).   |
| 16    | T1_START_ON_RX_ENDED     | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when a data reception ends.   |
| 15    | T1_START_ON_TX_STARTED   | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when a data transmission begins.  |
| 14    | T1_START_ON_TX_ENDED     | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when a data transmission ends.  |
| 13    | T1_START_ON_RF_ON_EXT    | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when the external RF field is detected.   |
| 12    | T1_START_ON_RF_OFF_EXT   | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when the external RF field is not detected anymore.   |
| 11    | T1_START_ON_RF_ON_INT    | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned on.   |
| 10    | T1_START_ON_RF_OFF_INT   | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when an internal RF field is turned off.  |
| 9     | T1_START_ON_TX_FRAMESTEP | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started when an activity on Frame step is detected.   |
| 8     | T1_START_NOW             | r/w    | 0*,1  | T1_START_EVENT: If set. the timer T1 is started immediately.  |
| 7     | RFU                      | r      | 0*,1  | -   |
| 6     | T1_ONE_SHOT_MODE         | r/w    | 0*,1  | When set to 1, the counter value does not reload again until the counter value has reached zero   |
| 5:3   | T1_PRESCALE_SEL          | r/w    | 0*,1  | Controls input frequency/period of the timer T0 when the prescaler is activated in T1_MODE_SEL.<br>000b - 6.78 MHz counter<br>001b - 3.39 MHz counter<br>010b - 1.70 MHz counter<br>011b - 848 kHz counter<br>100b - 424 kHz counter<br>101b - 212 kHz counter<br>110b - 106 kHz counter<br>111b - 53 kHz counter |
| 2     | T1_MODE_SEL              | r/w    | 0*,1  | If set. the timer T1 is started the prescaler for the timer T1 is enabled. 0* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1 Prescaler is enabled: the timer operates   |

Table 63. TIMER1\_CONFIG register (address 003Fh) bit description ...continued

| Bit | Symbol           | Access | Value | Description  |
|-----|------------------|--------|-------|--|
|     |                  |        |       | on the prescaler signal frequency (chosen by T1_PRESCALE_SEL).   |
| 1   | T1_RELOAD_ENABLE | r/w    | 0*,1  | If set to 0 the timer T1 will stop on expiration. 0* After expiration the timer T1 will stop counting. i.e. remain zero. reset value. 1 After expiration the timer T1 will reload its preset value and continue counting down. |
| 0   | T1_ENABLE        | r/w    | 0*,1  | Enables the timer T1   |

#### 9.25.44 TIMER1\_RELOAD (0040h)

Table 64. TIMER1\_RELOAD register (address 0040h) bit description

| Bit   | Symbol          | Access | Value | Description                   |
|-------|-----------------|--------|-------|-------------------------------|
| 31:20 | RFU             | r      | 0*,1  | -                             |
| 19:0  | T1_RELOAD_VALUE | r/w    | 0*,1  | Reload value of the timer T1. |

#### 9.25.45 ANA\_STATUS (0041h)

Table 65. ANA\_STATUS register (address 0041h) bit description

| Bit   | Symbol          | Access | Value | Description                             |
|-------|-----------------|--------|-------|---|
| 31:21 | RFU             | rw     | 0.1   | -                                       |
| 20:11 | ADC_DATA_I      | rw     | 0.1   | RX adc I output for validation purposes |
| 10:1  | ADC_DATA_Q      | rw     | 0.1   | RX adc Q output for validation purposes |
| 0     | PLL_LOCK_STATUS | rw     | 0.1   | PLL lock status indicator               |

#### 9.25.46 ANA\_RX\_CTRL (0043h)

Table 66. ANA\_RX\_CTRL register (address 0043h) bit description

| Bit  | Symbol              | Access | Value | Description                                   |
|------|---------------------|--------|-------|---|
| 31:7 | RFU                 | rw     | 0.1   | -   |
| 6    | RX_MIXER_SE_MODE_EN | rw     | 0.1   | enable signal for selecting single ended mode |
| 5:0  | RFU                 | rw     | 0.1   | -   |

#### 9.25.47 ANACTRL\_TX\_CONFIG (0044h)

Table 67. ANACTRL\_TX\_CONFIG register (address 0044h) bit description

| Bit  | Symbol    | Access | Value | Description  |
|------|-----------|--------|-------|--|
| 31:6 | RFU       | rw     | 0.1   | -  |
| 5:4  | TX_INV_RM | rw     | 0.1   | shift driver waves of 180 degrees in RM. Index 0: TX1; index 1: TX2<br>This value is initialized with data from TX_INV_RM (address 0018h) EEPROM bit 0.1 during Load protocol. |



Table 67. ANACTRL\_TX\_CONFIG register (address 0044h) bit description...continued

| Bit | Symbol         | Access | Value | Description   |
|-----|----------------|--------|-------|---|
| 3:2 | RFU            | rw     | 0.1   | -   |
| 1   | TX_PWM_MODE_RM | rw     | 0.1   | PWM scheme for RM: 0: TX1/2 3-levels (If at least either clk_mode_tx1 or clk_mode_tx2 is set on a clocked mode) 1: TX1/2 2-levels with differentiated pulses<br>This value is initialized with data from TX_SHAPING_CONFIG (address 0017h) EEPROM bit 0 during Load protocol. |
| 0   | RFU            | rw     | 0.1   | -   |

9.25.48 EMD\_1\_CFG (0047h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 68. EMD\_1\_CFG register (address 0047h) bit description

| Bit  | Symbol              | Access | Value | Description                                    |
|------|---------------------|--------|-------|--|
| 31:0 | EMD_1_Configuration | r/w    |       | 0000 FF03h EMD ISO<br>0000 FF04h EMD NFC Forum |

9.25.49 EMD\_0\_CONFIG (0048h)

This register allows to configure the ISO14443 and NFC-Forum EMD handling.

This register shall not be modified in case EMVCO or FeliCa EMD is activated.

Table 69. EMD\_0\_CONFIG register (address 0048h) bit description

| Bit  | Symbol              | Access | Value | Description                                       |
|------|---------------------|--------|-------|---|
| 31:0 | EMD_0_Configuration | r/w    |       | 176003FFh EMD ISO14443<br>1F6003FFh EMD NFC Forum |

9.25.50 LPCD\_CALIBRATE\_CTRL (00050h)

This register is used for LPCD semi autonomous mode. Writing to this register triggers the LPCD calibration with the RSSI\_HYSTERESIS and RSSI\_TARGET values as given in bits 23:16 and 15:0. After calibration is completed, calibration status is available in LPCD\_CALIBRATE\_STATUS. If the calibration is successful, the I/Q channel values can be read from register IQ\_CHANNEL\_VALS (51h).

Table 70. LPCD\_CALIBRATE\_CTRL register (address 0050h) bit description

| Bit | Symbol       | Access | Value | Description  |
|-----|--------------|--------|-------|--|
| 31  | RFU          | r      | 0*,1  | -  |
| 30  | FREEZE_VALUE | r/w    | 0*,1  | Write RSSI_TARGET and RSSI_HYSTERESIS into LPCD_CALIBRATE_CTRL:<br>1. <b>FREEZE_VALUE = 0:</b> This calibrates the Semi autonomous LPCD. The calibration status can be checked in bit 31 of CALIBRATE_STATUS register (0x53).<br>2. <b>FREEZE_VALUE = 1:</b> This writes the RSSI_TARGET and RSSI_HYSTERESIS into the EEPROM |

Table 70. LPCD\_CALIBRATE\_CTRL register (address 0050h) bit description...continued

| Bit   | Symbol          | Access | Value | Description  |
|-------|-----------------|--------|-------|--|
|       |                 |        |       | LPCD_RSSI_TARGET (0x494) and LPCD_RSSI_HYSTERESIS (0x496). |
| 29:24 | RFU             | r      | 0*,1  | -  |
| 23:16 | RSSI_HYSTERESIS | r/w    | 0*,1  | Value to be set in DGRM_RSSI_HYST used for calibration     |
| 15:0  | RSSI_TARGET     | r/w    | 0*,1  | Value to be set in DGRM_RSSI_TARGET used for calibration   |

### 9.25.51 IQ\_CHANNEL\_VALS (0051h)

Table 71. IQ\_CHANNEL\_VALS register (address 0051h) bit description

| Bit   | Symbol        | Access | Value | Description     |
|-------|---------------|--------|-------|-----------------|
| 31:16 | Q_CHANNEL_VAL | r      | -     | Q Channel value |
| 15:0  | I_CHANNEL_VAL | r      | -     | I Channel value |

### 9.25.52 PAD\_CONFIG (0052h)

Table 72. PAD\_CONFIG register (address 0052h) bit description

| Bit  | Symbol           | Access | Value | Description                                 |
|------|------------------|--------|-------|---|
| 31:7 | RFU              | rw     |       | -   |
| 6    | AUX3_OUTPUT_VAL  | rw     |       | Output value for AUX3<br>0: Low<br>1: High  |
| 5    | AUX2_OUTPUT_VAL  | rw     |       | Output value for AUX2<br>0: Low<br>1: High  |
| 4    | AUX1_OUTPUT_VAL  | rw     |       | Output value for AUX1<br>0: Low<br>1: High  |
| 3    | GPIO3_OUTPUT_VAL | rw     |       | Output value for GPIO3<br>0: Low<br>1: High |
| 2    | GPIO2_OUTPUT_VAL | rw     |       | Output value for GPIO2<br>0: Low<br>1: High |
| 1    | GPIO1_OUTPUT_VAL | rw     |       | Output value for GPIO1<br>0: Low<br>1: High |
| 0    | GPIO0_OUTPUT_VAL | rw     |       | Output value for GPIO0<br>0: Low<br>1: High |

On PN5190B1 only output functionality is available on GPIO's.

### 9.25.53 CALIBRATE\_STATUS (00053h)

Table 73. CALIBRATE\_STATUS register (address 0053h) bit description

| Bit  | Symbol                   | Access | Value | Description  |
|------|--------------------------|--------|-------|--|
| 31   | LPCD_CALIBRATION_STATUS  | r      | -     | Calibration Status<br>0 - Calibration Not Done,<br>1- Calibration Done |
| 30:1 | RFU                      | r      | -     | -  |
| 0    | TXNOV_CALIBRATION_STATUS |        |       | Calibration Status<br>0 - Calibration Not Done,<br>1- Calibration Done |

### 9.25.54 TXLDO\_VDDPA\_CONFIG (00054h)

If DPC is disabled, the VDDPA supply voltage can be set with this register. These register settings are overruled by the DPC.

This register does allow to read the actual VDDPA supply voltage independent from having the DPC enabled/disabled, this allows to read-out the actual transmitter supply voltage.

Table 74. TXLDO\_VDDPA\_CONFIG register (address 0054h) bit description

| Bit  | Symbol       | Access | Value | Description   |
|------|--------------|--------|-------|---|
| 31:8 | RFU          | rw     |       | -   |
| 7:0  | VDDPA CONFIG | rw     |       | TX_LDO output voltage<br>VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */<br>VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */<br>VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */<br>VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */<br>VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */<br>VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */<br>VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */<br>VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */<br>VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */<br>VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */<br>VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */<br>VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */<br>VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */<br>VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */<br>VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */<br>VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */<br>VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */<br>VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */<br>VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */<br>VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */<br>VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */<br>VDDPA_5V70, /* 0x2A */ |

### 9.25.55 GENERAL\_ERROR\_STATUS (0055h)

Table 75. GENERAL\_ERROR\_STATUS register (address 0055h) bit description

| Bit  | Symbol | Access | Value | Description |
|------|--------|--------|-------|-------------|
| 31:3 | RFU    | r      | 0*,1  | -           |

Table 75. GENERAL\_ERROR\_STATUS register (address 0055h) bit description...continued

| Bit | Symbol      | Access | Value | Description                |
|-----|-------------|--------|-------|----------------------------|
| 2   | TXLDO_ERROR | r      | 0*,1  | TXLDO does not start       |
| 1   | CLOCK_ERROR | r      | 0*,1  | XTAL or PLL does not start |
| 0   | GPADC_ERROR | r      | 0*,1  | GPADC initialization fail  |

### 9.25.56 TXLDO\_VOUT\_CURR (0056h)

Table 76. TXLDO\_VOUT\_CURR register (address 0056h) bit description

| Bit   | Symbol        | Access | Value | Description  |
|-------|---------------|--------|-------|--|
| 31:24 | RFU           | r      |       | -  |
| 23:8  | TXLDO_CURRENT | r      |       | Indicates the TXLDO Current, measured value is indicated in mA (1 bit = 1 mA)  |
| 7:0   | VDDPA_VOUT    | r      |       | VDDPA output voltage<br>VDDPA_1V50 /* 0x00 */ VDDPA_1V60, /* 0x01 */<br>VDDPA_1V70, /* 0x02 */ VDDPA_1V80, /* 0x03 */<br>VDDPA_1V90, /* 0x04 */ VDDPA_2V00, /* 0x05 */<br>VDDPA_2V10, /* 0x06 */ VDDPA_2V20, /* 0x07 */<br>VDDPA_2V30, /* 0x08 */ VDDPA_2V40, /* 0x09 */<br>VDDPA_2V50, /* 0x0A */ VDDPA_2V60, /* 0x0B */<br>VDDPA_2V70, /* 0x0C */ VDDPA_2V80, /* 0x0D */<br>VDDPA_2V90, /* 0x0E */ VDDPA_3V00, /* 0x0F */<br>VDDPA_3V10, /* 0x10 */ VDDPA_3V20, /* 0x11 */<br>VDDPA_3V30, /* 0x12 */ VDDPA_3V40, /* 0x13 */<br>VDDPA_3V50, /* 0x14 */ VDDPA_3V60, /* 0x15 */<br>VDDPA_3V70, /* 0x16 */ VDDPA_3V80, /* 0x17 */<br>VDDPA_3V90, /* 0x18 */ VDDPA_4V00, /* 0x19 */<br>VDDPA_4V10, /* 0x1A */ VDDPA_4V20, /* 0x1B */<br>VDDPA_4V30, /* 0x1C */ VDDPA_4V40, /* 0x1D */<br>VDDPA_4V50, /* 0x1E */ VDDPA_4V60, /* 0x1F */<br>VDDPA_4V70, /* 0x20 */ VDDPA_4V80, /* 0x21 */<br>VDDPA_4V90, /* 0x22 */ VDDPA_5V00, /* 0x23 */<br>VDDPA_5V10, /* 0x24 */ VDDPA_5V20, /* 0x25 */<br>VDDPA_5V30, /* 0x26 */ VDDPA_5V40, /* 0x27 */<br>VDDPA_5V50, /* 0x28 */ VDDPA_5V60, /* 0x29 */<br>VDDPA_5V70, /* 0x2A */ |

### 9.25.57 DAC (00057h)

This register allows configuring the output voltage of VTUNE1, VTUNE2.

Table 77. DAC register (address 00057h) bit description

| Bit   | Symbol             | Access | Value | Description   |
|-------|--------------------|--------|-------|---|
| 31:28 | RFU                |        |       | -   |
| 27:24 | TUNING_DAC_2_RANGE |        |       | Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111.<br><br>Available range:<br>0000=2 V<br>0001=3 V<br>0011=3.45 V |

Table 77. DAC register (address 0057h) bit description...continued

| Bit   | Symbol             | Access | Value | Description   |
|-------|--------------------|--------|-------|---|
|       |                    |        |       | 0111=3.8 V<br>If the VDDIO is 1.8 V, then configuration 000 shall be used. This applies only to DAC2.   |
| 23:17 | TUNING_DAC_2_VALUE |        |       | Output voltage of DAC2 according to $1/128 * <TUNING\_DAC\_2\_VALUE> * <Range\ in\ V>$  |
| 16    | TUNING_DAC_2_PD    |        |       | 0=DAC Turned off, 1=DAC enabled   |
| 15:12 | RFU                |        |       | -   |
| 11:8  | TUNING_DAC_1_RANGE |        |       | Reference voltage of the DAC, allows increasing the resolution in case a limited output voltage is required. For max output voltage, TUNING_DAC_2_RANGE needs to be configured to 111.<br>Available range:<br>0000=2 V<br>0001=3 V<br>0011=3.45 V<br>0111=3.8 V |
| 7:1   | TUNING_DAC_1_VALUE |        |       | Output voltage of DAC1 according to $1/128 * <TUNING\_DAC\_1\_VALUE> * <Range\ in\ V>$  |
| 0     | TUNING_DAC_1_PD    |        |       | 0=DAC Turned off, 1=DAC enabled   |

### 9.25.58 RXM\_FREQ (00059h)

Table 78. RXM\_FREQ register (address 0059h) bit description

| Bit   | Symbol             | Access | Value | Description  |
|-------|--------------------|--------|-------|--|
| 31    | RXM_FREQ_REG_VALID | r      | -     | CLIF_RXM_FREQ_REG fields are valid   |
| 30:25 | RFU                | r      | -     | -  |
| 24:16 | RXM_FREQ           | r      | -     | frequency difference between the last two consecutive measures at 1.7 MHz (multiple of 13.56 MHz/4096). Signed. 2-Complement coded |
| 15:9  | RFU                | r      | -     | -  |
| 0:8   | RXM_PHASE          | r      | -     | phase value  |

### 9.25.59 RXM\_RSSI (0005Ah)

Table 79. RXM\_RSSI register (address 005Ah) bit description

| Bit   | Symbol             | Access | Reset Value | Description                             |
|-------|--------------------|--------|-------------|---|
| 31:23 | RFU                | r      | -           | -                                       |
| 22    | RXM_RSSI_FROZEN    | r      | -           | The RSSI value is not currently updated |
| 21    | RXM_FRQ_OK         | r      | -           | The carrier frequency detected is OK.   |
| 20    | RXM_RSSI_REG_VALID | r      | -           | CLIF_RXM_RSSI_REG fields are valid      |
| 19:14 | RXM_HFATT          | r      | -           | HFAtt latched with RSSI                 |
| 13:0  | RXM_RSSI           | r      | -           | RSSI value                              |

### 9.25.60 TEMP\_SENSOR (005Bh)

Table 80. TEMP\_SENSOR register (address 005Bh) bit description

| Bit   | Symbol           | Access | Value | Description  |
|-------|------------------|--------|-------|--|
| 31:16 | -                | r      | 0*,1  | RFU  |
| 15:0  | TEMP_SENSOR_DATA | r      | 0*,1  | Indicates the current temperature of the chip in degree celsius.<br>This is the actual temperature data of the sensor which is used for the overheat protection.<br>Maximum temperature readable will be the maximum temperature threshold configured in EEPROM TEMP_WARNING address 0x14. |

### 9.25.61 TX\_NOV\_CALIBRATE\_AND\_STORE (005Dh)

Table 81. TX\_NOV\_CALIBRATE\_AND\_STORE register (address 005Dh) bit description

| Bit   | Symbol                         | Access | Value | Description  |
|-------|--------------------------------|--------|-------|--|
| 31:29 | RFU                            | rw     | 0*,1  | -  |
| 1:0   | TX_NOV_CALIBRATE_AND_STORE_VAL | rw     |       | Calibrates the TX NOV and stores the resulting value in EEPROM |

### 9.25.62 DPC\_CONFIG (005Eh)

Table 82. DPC\_CONFIG register (address 005Eh) bit description

| Bit  | Symbol             | Access | Value | Description  |
|------|--------------------|--------|-------|--|
| 31   | DPC_REG_ACCESS     | r/w    | 0*,1  | This bit is used to enable the DPC enable / disable control via register.<br>1: DPC enabled / disabled via register.<br>0: DPC enabled / disabled via EEPROM (default)<br>This bit needs to be SET to enable/disable the functionality of bit 0. |
| 30:1 | RFU                | r/w    | 0*,1  | -  |
| 0    | ENABLE_DISABLE_DPC | r/w    | 0*,1  | 1: DPC enabled, if bit 31 is enabled.<br>0: DPC disabled, if bit 31 is enabled.<br>The DPC can only be enabled or disabled during RF off.  |

### 9.25.63 TIMER0\_OUTPUT (005Fh)

Available from firmware version 2.05 onwards:

Table 83. TIMER0\_OUTPUT register (address 005Fh) bit description

| Bit   | Symbol     | Access | Value | Description                               |
|-------|------------|--------|-------|---|
| 31:25 | RFU        | r      | 0*,1  | -   |
| 24    | T0_RUNNING | r      | 0*,1  | Indicates that timer T0 is running (busy) |
| 23:20 | RFU        | r      | 0*,1  | -   |
| 19:0  | T0_VALUE   | r/w    | 0*,1  | Value of 20bit counter in timer T0        |

### 9.25.64 TIMER1\_OUTPUT (0060h)

Available from firmware version 2.05 onwards:

Table 84. TIMER1\_OUTPUT register (address 0060h) bit description

| Bit   | Symbol     | Access | Value | Description                               |
|-------|------------|--------|-------|---|
| 31:25 | RFU        | r      | 0*,1  | -   |
| 24    | T1_RUNNING | r      | 0*,1  | Indicates that timer T1 is running (busy) |
| 23:20 | RFU        | r      | 0*,1  | -   |
| 19:0  | T1_VALUE   | r/w    | 0*,1  | Value of 20bit counter in timer T1        |

### 9.25.65 TIMER2\_CONFIG (0061h)

Available from firmware version 2.05 onwards:

Timer 2 is typically used for the FDT measurement.

Table 85. TIMER2\_CONFIG register (address 0061h) bit description

| Bit   | Symbol                 | Access | Value | Description   |
|-------|------------------------|--------|-------|---|
| 31    | RFU                    | r      | 0*,1  | -   |
| 30    | T2_STOP_ON_RX_STARTED  | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when a data reception begins (1st bit is received).  |
| 29    | T2_STOP_ON_TX_STARTED  | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when a data transmission begins.                     |
| 28    | T2_STOP_ON_RF_ON_EXT   | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when the external RF field is detected.              |
| 27    | T2_STOP_ON_RF_OFF_EXT  | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when the external RF field vanishes.                 |
| 26    | T2_STOP_ON_RF_ON_INT   | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when the internal RF field is turned on.             |
| 25    | T2_STOP_ON_RF_OFF_INT  | r/w    | 0*,1  | T2_STOP_EVENT: If set, the timer T2 is stopped when the internal RF field is turned off.            |
| 24    | T2_STOP_ON_RX_ENDED    | r/w    | 0*,1  | T2_STOP_EVENT: If set the timer T2 is stopped when an activity on RX is detected.                   |
| 23:18 | RFU                    | r      | 0*,1  | -   |
| 17    | T2_START_ON_RX_STARTED | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when a data reception begins (1st bit is received). |
| 16    | T2_START_ON_RX_ENDED   | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when a data reception ends.                         |
| 15    | T2_START_ON_TX_STARTED | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when a data transmission begins.                    |
| 14    | T2_START_ON_TX_ENDED   | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when a data transmission ends.                      |
| 13    | T2_START_ON_RF_ON_EXT  | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when the external RF field is detected.             |
| 12    | T2_START_ON_RF_OFF_EXT | r/w    | 0*,1  | T2_START_EVENT: If set, the timer T2 is started when the external RF field is not detected anymore. |

Table 85. TIMER2\_CONFIG register (address 0061h) bit description ...continued

| Bit | Symbol                   | Access | Value | Description   |
|-----|--------------------------|--------|-------|---|
| 11  | T2_START_ON_RF_ON_INT    | r/w    | 0*,1  | T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned on.   |
| 10  | T2_START_ON_RF_OFF_INT   | r/w    | 0*,1  | T2_START_EVENT: If set. the timer T2 is started when an internal RF field is turned off.  |
| 9   | T2_START_ON_TX_FRAMESTEP | r/w    | 0*,1  | T2_START_EVENT: If set. the timer T2 is started when an activity on Frame step is detected.   |
| 8   | T2_START_NOW             | r/w    | 0*,1  | T2_START_EVENT: If set. the timer T2 is started immediately.  |
| 7   | RFU                      | r      | 0*,1  | -   |
| 6   | T2_ONE_SHOT_MODE         | r/w    | 0*,1  | When set to 1, the counter value does not reload again until the counter value has reached zero   |
| 5:3 | T2_PRESCALE_SEL          | r/w    | 0*,1  | Controls input frequency/period of the timer T0 when the prescaler is activated in T2_MODE_SEL.<br>000b - 6.78 MHz counter<br>001b - 3.39 MHz counter<br>010b - 1.70 MHz counter<br>011b - 848 kHz counter<br>100b - 424 kHz counter<br>101b - 212 kHz counter<br>110b - 106 kHz counter<br>111b - 53 kHz counter |
| 2   | T2_MODE_SEL              | r/w    | 0*,1  | If set. the timer T2 is started the prescaler for the timer T2 is enabled. 0* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1 Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T2_PRESCALE_SEL).                                      |
| 1   | T2_RELOAD_ENABLE         | r/w    | 0*,1  | If set to 0, the timer T2 stops on expiration. 0* After expiration the timer T2 stops counting. i.e. remain zero. reset value. 1 After expiration the timer T2 reloads its preset value and continue counting down.   |
| 0   | T2_ENABLE                | r/w    | 0*,1  | Enables the timer T2  |

### 9.25.66 TIMER2\_RELOAD (0062h)

Available from firmware version 2.05 onwards:

Table 86. TIMER2\_RELOAD register (address 0062h) bit description

| Bit   | Symbol          | Access | Value | Description                   |
|-------|-----------------|--------|-------|-------------------------------|
| 31:20 | RFU             | r      | 0*,1  | -                             |
| 19:0  | T2_RELOAD_VALUE | r/w    | 0*,1  | Reload value of the timer T2. |

### 9.25.67 TIMER2\_OUTPUT (0063h)

Available from firmware version 2.05 onwards:



Table 87. TIMER2\_OUTPUT register (address 0063h) bit description

| Bit   | Symbol     | Access | Value | Description                               |
|-------|------------|--------|-------|---|
| 31:25 | RFU        | r      | 0*,1  | -   |
| 24    | T2_RUNNING | r      | 0*,1  | Indicates that timer T2 is running (busy) |
| 23:20 | RFU        | r      | 0*,1  | -   |
| 19:0  | T2_VALUE   | r/w    | 0*,1  | Value of 20bit counter in timer T2        |

### 9.25.68 SS\_TX1\_RTRTRANS0 (00080h)

Table 88. SS\_TX1\_RTRTRANS0 register (address 0080h) bit description

| Bit   | Symbol         | Access | Value | Description                   |
|-------|----------------|--------|-------|-------------------------------|
| 31:24 | TX1_SS_RTRANS3 | rw     |       | TX1 rising transition value 3 |
| 23:16 | TX1_SS_RTRANS2 | rw     |       | TX1 rising transition value 2 |
| 15:8  | TX1_SS_RTRANS1 | rw     |       | TX1 rising transition value 1 |
| 7:0   | TX1_SS_RTRANS0 | rw     |       | TX1 rising transition value 0 |

### 9.25.69 SS\_TX1\_RTRTRANS1 (00081h)

Table 89. SS\_TX1\_RTRTRANS1 register (address 0081h) bit description

| Bit   | Symbol         | Access | Value | Description                   |
|-------|----------------|--------|-------|-------------------------------|
| 31:24 | TX1_SS_RTRANS7 | rw     |       | TX1 rising transition value 7 |
| 23:16 | TX1_SS_RTRANS6 | rw     |       | TX1 rising transition value 6 |
| 15:8  | TX1_SS_RTRANS5 | rw     |       | TX1 rising transition value 5 |
| 7:0   | TX1_SS_RTRANS4 | rw     |       | TX1 rising transition value 4 |

### 9.25.70 SS\_TX1\_RTRTRANS2 (00082h)

Table 90. SS\_TX1\_RTRTRANS2 register (address 0082h) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_RTRANS11 | rw     |       | TX1 rising transition value 11 |
| 23:16 | TX1_SS_RTRANS10 | rw     |       | TX1 rising transition value 10 |
| 15:8  | TX1_SS_RTRANS9  | rw     |       | TX1 rising transition value 9  |
| 7:0   | TX1_SS_RTRANS8  | rw     |       | TX1 rising transition value 8  |

### 9.25.71 SS\_TX1\_RTRTRANS3 (00083h)

Table 91. SS\_TX1\_RTRTRANS0 register (address 0080h) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_RTRANS15 | rw     |       | TX1 rising transition value 15 |
| 23:16 | TX1_SS_RTRANS14 | rw     |       | TX1 rising transition value 14 |
| 15:8  | TX1_SS_RTRANS13 | rw     |       | TX1 rising transition value 13 |
| 7:0   | TX1_SS_RTRANS12 | rw     |       | TX1 rising transition value 12 |

9.25.72 SS\_TX2\_RTRTRANS0 (00084h)

Table 92. SS\_TX2\_RTRTRANS0 register (address 0084h) bit description

| Bit   | Symbol         | Access | Value | Description                   |
|-------|----------------|--------|-------|-------------------------------|
| 31:24 | TX2_SS_RTRANS3 | rw     | 0*,1  | TX2 rising transition value 3 |
| 23:16 | TX2_SS_RTRANS2 | rw     | 0*,1  | TX2 rising transition value 2 |
| 15:8  | TX2_SS_RTRANS1 | rw     | 0*,1  | TX2 rising transition value 1 |
| 7:0   | TX2_SS_RTRANS0 | rw     | 0*,1  | TX2 rising transition value 0 |

9.25.73 SS\_TX2\_RTRTRANS1 (00085h)

Table 93. SS\_TX2\_RTRTRANS1 register (address 0085h) bit description

| Bit   | Symbol         | Access | Value | Description                   |
|-------|----------------|--------|-------|-------------------------------|
| 31:24 | TX2_SS_RTRANS7 | rw     |       | TX2 rising transition value 7 |
| 23:16 | TX2_SS_RTRANS6 | rw     |       | TX2 rising transition value 6 |
| 15:8  | TX2_SS_RTRANS5 | rw     |       | TX2 rising transition value 5 |
| 7:0   | TX2_SS_RTRANS4 | rw     |       | TX2 rising transition value 4 |

9.25.74 SS\_TX2\_RTRTRANS2 (00086h)

Table 94. SS\_TX2\_RTRTRANS2 register (address 0086h) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX2_SS_RTRANS11 | rw     |       | TX2 rising transition value 11 |
| 23:16 | TX2_SS_RTRANS10 | rw     |       | TX2 rising transition value 10 |
| 15:8  | TX2_SS_RTRANS9  | rw     |       | TX2 rising transition value 9  |
| 7:0   | TX2_SS_RTRANS8  | rw     |       | TX2 rising transition value 8  |

9.25.75 SS\_TX2\_RTRTRANS3 (00087h)

Table 95. SS\_TX2\_RTRTRANS3 register (address 0087h) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX2_SS_RTRANS15 | rw     |       | TX2 rising transition value 15 |
| 23:16 | TX2_SS_RTRANS14 | rw     |       | TX2 rising transition value 14 |
| 15:8  | TX2_SS_RTRANS13 | rw     |       | TX2 rising transition value 13 |
| 7:0   | TX2_SS_RTRANS12 | rw     |       | TX2 rising transition value 12 |

9.25.76 SS\_TX1\_FTRTRANS0 (00088h)

Table 96. SS\_TX1\_FTRTRANS0 register (address 0088h) bit description

| Bit   | Symbol         | Access | Value | Description                    |
|-------|----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_FTRANS3 | rw     | 0*,1  | TX1 falling transition value 3 |
| 23:16 | TX1_SS_FTRANS2 | rw     | 0*,1  | TX1 falling transition value 2 |
| 15:8  | TX1_SS_FTRANS1 | rw     | 0*,1  | TX1 falling transition value 1 |

Table 96. SS\_TX1\_FTRTRANS0 register (address 0088h) bit description...continued

| Bit | Symbol         | Access | Value | Description                    |
|-----|----------------|--------|-------|--------------------------------|
| 7:0 | TX1_SS_FTRANS0 | rw     | 0*,1  | TX1 falling transition value 0 |

9.25.77 SS\_TX1\_FTRTRANS1 (00089h)

Table 97. SS\_TX1\_FTRTRANS1 register (address 0089h) bit description

| Bit   | Symbol         | Access | Value | Description                    |
|-------|----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_FTRANS7 | rw     |       | TX1 falling transition value 7 |
| 23:16 | TX1_SS_FTRANS6 | rw     |       | TX1 falling transition value 6 |
| 15:8  | TX1_SS_FTRANS5 | rw     |       | TX1 falling transition value 5 |
| 7:0   | TX1_SS_FTRANS4 | rw     |       | TX1 falling transition value 4 |

9.25.78 SS\_TX1\_FTRTRANS2 (0008Ah)

Table 98. SS\_TX1\_FTRTRANS2 register (address 008Ah) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_FTRANS11 | rw     |       | TX1 rising transition value 11 |
| 23:16 | TX1_SS_FTRANS10 | rw     |       | TX1 rising transition value 10 |
| 15:8  | TX1_SS_FTRANS9  | rw     |       | TX1 rising transition value 9  |
| 7:0   | TX1_SS_FTRANS8  | rw     |       | TX1 rising transition value 8  |

9.25.79 SS\_TX1\_FTRTRANS3 (0008Bh)

Table 99. SS\_TX1\_FTRTRANS3 register (address 008Bh) bit description

| Bit   | Symbol          | Access | Value | Description                    |
|-------|-----------------|--------|-------|--------------------------------|
| 31:24 | TX1_SS_FTRANS15 | rw     |       | TX1 rising transition value 15 |
| 23:16 | TX1_SS_FTRANS14 | rw     |       | TX1 rising transition value 14 |
| 15:8  | TX1_SS_FTRANS13 | rw     |       | TX1 rising transition value 13 |
| 7:0   | TX1_SS_FTRANS12 | rw     |       | TX1 rising transition value 12 |

9.25.80 SS\_TX2\_FTRTRANS0 (0008Ch)

Table 100. SS\_TX2\_FTRTRANS0 register (address 008Ch) bit description

| Bit   | Symbol         | Access | Value | Description                    |
|-------|----------------|--------|-------|--------------------------------|
| 31:24 | TX2_SS_FTRANS3 | rw     |       | TX2 falling transition value 3 |
| 23:16 | TX2_SS_FTRANS2 | rw     |       | TX2 falling transition value 2 |
| 15:8  | TX2_SS_FTRANS1 | rw     |       | TX2 falling transition value 1 |
| 7:0   | TX2_SS_FTRANS0 | rw     |       | TX2 falling transition value 0 |

**9.25.81 SS\_TX2\_FTRTRANS1 (0008Dh)**

Table 101. SS\_TX2\_FTRTRANS1 register (address 008Dh) bit description

| Bit   | Symbol         | Access | Value | Description                    |
|-------|----------------|--------|-------|--------------------------------|
| 31:24 | TX2_SS_FTRANS7 | rw     |       | TX2 falling transition value 7 |
| 23:16 | TX2_SS_FTRANS6 | rw     |       | TX2 falling transition value 6 |
| 15:8  | TX2_SS_FTRANS5 | rw     |       | TX2 falling transition value 5 |
| 7:0   | TX2_SS_FTRANS4 | rw     |       | TX2 falling transition value 4 |

**9.25.82 SS\_TX2\_FTRTRANS2 (0008Eh)**

Table 102. SS\_TX2\_FTRTRANS2 register (address 008Eh) bit description

| Bit   | Symbol          | Access | Value | Description                     |
|-------|-----------------|--------|-------|---------------------------------|
| 31:24 | TX2_SS_FTRANS11 | rw     |       | TX2 falling transition value 11 |
| 23:16 | TX2_SS_FTRANS10 | rw     |       | TX2 falling transition value 10 |
| 15:8  | TX2_SS_FTRANS9  | rw     |       | TX2 falling transition value 9  |
| 7:0   | TX2_SS_FTRANS8  | rw     |       | TX2 falling transition value 8  |

**9.25.83 SS\_TX2\_FTRTRANS3 (0008Fh)**

Table 103. SS\_TX2\_FTRTRANS3 register (address 008Fh) bit description

| Bit   | Symbol          | Access | Value | Description                     |
|-------|-----------------|--------|-------|---------------------------------|
| 31:24 | TX2_SS_FTRANS15 | rw     |       | TX2 falling transition value 15 |
| 23:16 | TX2_SS_FTRANS14 | rw     |       | TX2 falling transition value 14 |
| 15:8  | TX2_SS_FTRANS13 | rw     |       | TX2 falling transition value 13 |
| 7:0   | TX2_SS_FTRANS12 | rw     |       | TX2 falling transition value 12 |

**9.26 EEPROM configuration description**

The settings done in EEPROM are used for basic configuration which does not change frequently. Typically it is performed once during trimming or configuration of a product. The EEPROM has a limited number of erase/write cycles that can be performed. This means, that configurations that change frequently must be performed in standard registers which do not keep their value during reset and power off.

This section describes the EEPROM configuration of the PN5190B1.

**Writing to the EEPROM has to be performed with Read-Modify-Write for all memory addresses which contain RFU bits.**

The detailed description of the EEPROM is available in the User API documentation.

## 9.26.1 EEPROM configuration overview

Table 104. EEPROM CONFIGURATION REGISTER

| Address (HEX) | Name                      |
|---------------|---------------------------|
| 0             | DCDC_PWR_CONFIG           |
| 1             | DCDC_CONFIG               |
| 2             | TXLDO_CONFIG              |
| 6             | TXLDO_VDDPA_HIGH          |
| 7             | RFU                       |
| 8             | TXLDO_VDDPA_MAX_RDR       |
| 9             | TXLDO_VDDPA_HIGH_MAX_CARD |
| A             | BOOST_DEFAULT_VOLTAGE     |
| 10            | XTAL_CONFIG               |
| 11            | XTAL_TIMEOUT              |
| 12            | CLK_INPUT_FREQ            |
| 13            | XTAL_CHECK_DELAY          |
| 14            | TEMP_WARNING              |
| 15            | RFU                       |
| 16            | ENABLE_GPIO0_ON_OVERTEMP  |
| 17            | TX_SHAPING_CONFIG         |
| 18            | TX_INV_RM                 |
| 19            | TX_CLK_MODE_1             |
| 1A            | TX_CLK_MODE_2             |
| 1B            | RFU                       |
| 1C            | RFU                       |
| 1D            | RFU                       |
| 1E            | RFU                       |
| 1F            | RFU                       |
| 20            | RFU                       |
| 21            | RFU                       |
| 22            | RESIDUAL_AMP_LEVEL_A106   |
| 23            | EDGE_TYPE_A106            |
| 24            | EDGE_STYLE_A106           |
| 25            | EDGE_LENGTH_A106          |
| 26            | RESIDUAL_AMP_LEVEL_A212   |
| 27            | EDGE_TYPE_A212            |
| 28            | EDGE_STYLE_A212           |
| 29            | EDGE_LENGTH_A212          |

Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name                       |
|---------------|----------------------------|
| 2A            | RESIDUAL_AMP_LEVEL_A424    |
| 2B            | EDGE_TYPE_A424             |
| 2C            | EDGE_STYLE_A424            |
| 2D            | EDGE_LENGTH_A424           |
| 2E            | RESIDUAL_AMP_LEVEL_A848    |
| 2F            | EDGE_TYPE_A848             |
| 30            | EDGE_STYLE_A848            |
| 31            | EDGE_LENGTH_A848           |
| 32            | RESIDUAL_AMP_LEVEL_B106    |
| 33            | EDGE_TYPE_B106             |
| 34            | EDGE_STYLE_B106            |
| 35            | EDGE_LENGTH_B106           |
| 36            | RESIDUAL_AMP_LEVEL_B212    |
| 37            | EDGE_TYPE_B212             |
| 38            | EDGE_STYLE_B212            |
| 39            | EDGE_LENGTH_B212           |
| 3A            | RESIDUAL_AMP_LEVEL_B424    |
| 3B            | EDGE_TYPE_B424             |
| 3C            | EDGE_STYLE_B424            |
| 3D            | EDGE_LENGTH_B424           |
| 3E            | RESIDUAL_AMP_LEVEL_B848    |
| 3F            | EDGE_TYPE_A848             |
| 40            | EDGE_STYLE_A848            |
| 41            | EDGE_LENGTH_A848           |
| 42            | RESIDUAL_AMP_LEVEL_F212    |
| 43            | EDGE_TYPE_F212             |
| 44            | EDGE_STYLE_F212            |
| 45            | EDGE_LENGTH_F212           |
| 46            | RESIDUAL_AMP_LEVEL_F424    |
| 47            | EDGE_TYPE_F424             |
| 48            | EDGE_STYLE_F424            |
| 49            | EDGE_LENGTH_F424           |
| 4A            | RESIDUAL_AMP_LEVEL_V100_26 |
| 4B            | EDGE_TYPE_V100_26          |
| 4C            | EDGE_STYLE_V100_26         |
| 4D            | EDGE_LENGTH_V100_26        |

Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name                                  |
|---------------|---------------------------------------|
| 4E            | RESIDUAL_AMP_LEVEL_V100_53            |
| 4F            | EDGE_TYPE_V100_53                     |
| 50            | EDGE_STYLE_V100_53                    |
| 51            | EDGE_LENGTH_V100_53                   |
| 52            | RESIDUAL_AMP_LEVEL_V100_106           |
| 53            | EDGE_TYPE_V100_106                    |
| 54            | EDGE_STYLE_V100_106                   |
| 55            | EDGE_LENGTH_V100_106                  |
| 56            | RESIDUAL_AMP_LEVEL_V100_212           |
| 57            | EDGE_TYPE_V100_212                    |
| 58            | EDGE_STYLE_V100_212                   |
| 59            | EDGE_LENGTH_V100_212                  |
| 5A            | RESIDUAL_AMP_LEVEL_V10_26             |
| 5B            | EDGE_TYPE_V10_26                      |
| 5C            | EDGE_STYLE_V10_26                     |
| 5D            | EDGE_LENGTH_V10_26                    |
| 5E            | RESIDUAL_AMP_LEVEL_V10_53             |
| 5F            | EDGE_TYPE_V10_53                      |
| 60            | EDGE_STYLE_V10_53                     |
| 61            | EDGE_LENGTH_V10_53                    |
| 62            | RESIDUAL_AMP_LEVEL_V10_106            |
| 63            | EDGE_TYPE_V10_106                     |
| 64            | EDGE_STYLE_V10_106                    |
| 65            | EDGE_LENGTH_V10_106                   |
| 66            | RESIDUAL_AMP_LEVEL_V10_212            |
| 67            | EDGE_TYPE_V10_212                     |
| 68            | EDGE_STYLE_V10_212                    |
| 69            | EDGE_LENGTH_V10_212                   |
| 66            | RESIDUAL_AMP_LEVEL_V10_212            |
| 67            | EDGE_TYPE_V10_212                     |
| 68            | EDGE_STYLE_V10_212                    |
| 69            | EDGE_LENGTH_V10_212                   |
| 6A            | RESIDUAL_AMP_LEVEL_180003m3_tari18p88 |
| 6B            | EDGE_TYPE_180003m3_tari18p88          |
| 6C            | EDGE_STYLE_180003m3_tari18p88         |
| 6D            | EDGE_LENGTH_180003m3_tari18p88        |

Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name  |
|---------------|---|
| 6E            | RESIDUAL_AMP_LEVEL_180003m3_tari9p44          |
| 6F            | EDGE_TYPE_180003m3_tari9p44                   |
| 70            | EDGE_STYLE_180003m3_tari9p44                  |
| 71            | EDGE_LENGTH_180003m3_tari9p44                 |
| 72            | RESIDUAL_AMP_LEVEL_B_PRIME_106                |
| 73            | EDGE_TYPE_B_PRIME_106                         |
| 74            | EDGE_STYLE_B_PRIME_106                        |
| 75            | EDGE_LENGTH_B_PRIME_106                       |
| 76            | DPC_CONFIG                                    |
| 77            | DPC_TARGET_CURRENT                            |
| 79            | DPC_HYSTERESIS_LOADING                        |
| 7A            | RFU   |
| 7B            | RFU   |
| 7C            | DPC_HYSTERESIS_UNLOADING                      |
| 7D            | DPC_TXLDOVDDPALow                             |
| 7E            | DPC_TXGSN                                     |
| 7F            | DPC_RDON_Control                              |
| 80            | DPC_InitialRDO <sub>n</sub> _RFO <sub>n</sub> |
| 81            | DPC_TXLDO_MAX_DROP                            |
| 83            | RFU   |
| 85            | RFU   |
| 87            | DPC_GUARD_TIME                                |
| 88            | DPC_ENABLE_DURING_FDT                         |
| 89            | DPC_GUARD_TIME_AFTER_RX                       |
| 8A            | RFU   |
| 8B            | DPC_LOOKUP_TABLE                              |
| 137           | ARC_CONFIG                                    |
| 139           | ARC_VDDPA                                     |
| 13E           | ARC_RM_A106                                   |
| 148           | ARC_RM_A212                                   |
| 152           | ARC_RM_A424                                   |
| 15C           | ARC_RM_A848                                   |
| 166           | ARC_RM_B106                                   |
| 170           | ARC_RM_B212                                   |
| 17A           | ARC_RM_B424                                   |
| 184           | ARC_RM_B848                                   |



Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name                       |
|---------------|----------------------------|
| 18E           | ARC_RM_F212                |
| 198           | ARC_RM_F424                |
| 1A2           | ARC_RM_V6p6                |
| 1AC           | ARC_RM_V26                 |
| 1B6           | ARC_RM_V53                 |
| 1C0           | ARC_RM_V106                |
| 1CA           | ARC_RM_V212                |
| 1D4           | ARC_RM_18003m3_SC424_4MAN  |
| 1DE           | ARC_RM_18003m3_SC848_2MAN  |
| 1E8           | ARC_RM_18003m3_SC848_4MAN  |
| 1F2           | ARC_RM_18003m3_SC848_2MAN  |
| 1FC           | ARC_RM_AI106               |
| 206           | ARC_RM_AI212               |
| 210           | ARC_RM_AI424               |
| 2B2           | RF_DEBOUNCE_TIMEOUT        |
| 2B3           | SENSE_RES                  |
| 2B5           | NFC_ID1                    |
| 2B8           | SEL_RES                    |
| 2B9           | FELICA_POLL_RES            |
| 2CB           | RANDOM_UID_ENABLE          |
| 2CC           | MFC_AUTH_TIMEOUT           |
| 2DA           | RSSI_TIMER                 |
| 2DC           | RSSI_TIMER_FIRST_PERIOD    |
| 2DE           | RSSI_CTRL_00_AB            |
| 2DF           | RSSI_NB_ENTRIES_AB         |
| 2E0           | RSSI_THRESHOLD_PHASE_TABLE |
| 3A2           | TX_PARAM_ENTRY_TABLE       |
| 492           | LPCD_AVG_SAMPLES           |
| 494           | LPCD_RSSI_TARGET           |
| 496           | LPCD_RSSI_HYST             |
| 497-499       | RFU                        |
| 49A           | LPCD_THRESHOLD             |
| 49B-4AA       | RFU                        |
| 4AB           | WAIT_RX_SETTLE             |
| 4AF           | LPCD_VDDPA                 |
| 4BF           | ULPCD_VDDPA_CTRL           |

Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name   |
|---------------|--|
| 4C2           | ULPCD_TIMING_CTRL  |
| 4C6           | ULPCD_VOLTAGE_CTRL   |
| 4C7           | RFU  |
| 4C9           | ULPCD_RSSI_GUARD_TIME  |
| 4CA           | ULPCD_RSSI_SAMPLE_CFG  |
| 4CB           | ULPCD_THRESH_LVL   |
| 4CC           | ULPCD_GPIO3  |
| 559           | TXIRQ_GUARDTIME  |
| 55D           | FDT_DEFAULTVAL   |
| 561           | RXIRQ_GUARDTIME  |
| 562-6D2       | RFU  |
| 6D3           | NFCLD_RFLD_Valid   |
| 6D4-ABB       | RFU  |
| ABC           | RFU  |
| ABD-BD9       | RFU  |
| BDA           | CORRECTION_ENTRY_TABLE   |
| C03           | RTRANS_FRTANS_TABLE  |
| C83           | CFG_NOV_CAL  |
| C84           | NOV_CAL_VAL1   |
| C85           | NOV_CAL_VAL2   |
| C86           | NOV_CAL_THRESHOLD  |
| C87           | NOV_CAL_OFFSET1  |
| C8B           | NOV_CAL_OFFSET2  |
| C8F           | VDDPA_DISCHARGE  |
| C9D           | ARC_RM_A106_FDT  |
| CA8-CC4       | RFU  |
| CC5           | Tx_Symbol23_Mod_Reg_BR_53                                      |
| CC9           | Tx_Data_Mod_Reg_BR_53  |
| CCD           | Tx_Symbol23_Mod_Reg_BR_106                                     |
| CD1           | Tx_Data_Mod_Reg_BR_106   |
| CD5           | Tx_Symbol23_Mod_Reg_BR_212                                     |
| CD9           | Tx_Data_Mod_Reg_BR_212   |
| CDA-CDE       | RFU  |
| CDF           | CardModeUltraLowPowerEnabled                                   |
| CE0           | Up to FW2.01: RFU<br>from FW2.02 onwards: LPCD_EXT_DCDC_ENABLE |

Table 104. EEPROM CONFIGURATION REGISTER...continued

| Address (HEX) | Name   |
|---------------|--|
| CE1           | Up to FW2.01: RFU<br>from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON      |
| CE2           | Up to FW2.01: RFU<br>from FW2.02 onwards: LPCD_EXT_DCDC_DELAY_TO_ON      |
| CE3-CE7       | DO NOT MODIFY - INTERNAL SETTINGS  |
| CE8           | RxGuardTO_Multiple   |
| CE9           | up to FW 2.03: RFU<br>from FW2.05 onwards: DigitalTBSignalIndex          |
| CEA           | up to FW 2.03: RFU<br>from FW2.05 onwards: DigitalTBSignalBit            |
| CEB           | up to FW 2.03: RFU<br>from FW2.05 onwards: AnalogTBSignal                |
| CEC           | up to FW 2.06: RFU<br>from FW 2.07 onwards: ENABLE_ULFO_TRIM_CALIBRATION |
| CED-D2C       | RFU  |
| D2D-D3C       | up to FW 2.03: RFU<br>from FW2.05 onwards: USER DATA                     |
| D3Dh-1400h    | DO NOT MODIFY - INTERNAL SETTINGS  |

### 9.26.2 DCDC\_PWR\_CONFIG (0000h)

Table 105. PWR\_CONFIG (address 0000h) EEPROM configuration bit description

| Address (hex) | Function                   | Bit  | Description  |
|---------------|----------------------------|------|--|
| 0             | DC-DC usage in card mode   | 7    | 0b: DC-DC is not powered and set to bypass<br>1b: DC-DC is powered and not bypassed  |
|               | DC-DC usage in reader mode | 6    | 0b: DC-DC is not powered and set to bypass<br>1b: DC-DC is powered and not bypassed  |
|               | RFU                        | 5    | Do not touch, default value 01b  |
|               | VUP input voltage          | 4..0 | 0x00: Not connected or 0 V<br>0x01: No DC-DC and internal VDDPA_LDO: VUP supplied by VBAT / VBATPWR (pin VUP_TX connected to VBAT/VBATPWR)<br>0x02: Internal DC-DC: with fixed VDDBOOST<br>0x04: Internal DC-DC: with auto by pass and variable boost w.r.t VDDPA (internal DPC controls VDDBOOST): DC-DC goes into pass through mode when the VDDPA goes below 3.3 V. When VDDPA is greater than 3.3 V, the DC-DC is configured to boost voltage in range of 3.3 V to 6 V.<br>0x05 - 0x09: RFU<br>0x10: No DC-DC and internal VDDPA_LDO: VUP supplied by external LDO (not connected to VBAT) |

### 9.26.3 DCDC\_CONFIG (0001h)

Table 106. DCDC\_CONFIG (address 0001h) EEPROM configuration bit description

| Address (hex) | Function            | Bit | Description  |
|---------------|---------------------|-----|--|
| 1             | DC-DC configuration | 7:5 | RFU  |
|               |                     | 4   | DC-DC passthrough feature is:<br>0: Not supported (Vout = 0v or +5v)<br>1: Supported (Vout = 0v, Vin or +5v) |
|               |                     | 3   | Use of DC-DC for LPCD (attention: not ULPCD)<br>1: enabled<br>0: disabled                                    |
|               |                     | 2:0 | RFU  |

### 9.26.4 TXLDO\_CONFIG (0002h)

Table 107. TXLDO\_CONFIG (address 0002h) EEPROM configuration bit description

| Address (hex) | Function             | Bit  | Description  |
|---------------|----------------------|------|--|
| 2             | TX_LDO Configuration | 31:2 | RFU  |
|               |                      | 1    | Overcurrent protection (0: Disable, 1: Enable)   |
|               |                      | 0    | Enable TXLDO<br>0b: disabled - no voltage output of the TXLDO<br>1b: enabled - regulated output of the TXLDO |

### 9.26.5 TXLDO\_VDDPA\_HIGH (0006h)

Table 108. TXLDO\_VDDPA\_HIGH (address 0006h) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description  |
|---------------|--|-----|--|
| 6             | TX_LDO output: initial voltage in case the DPC is used. Applies directly at the beginning of the RF-field-on before any DPC regulation takes place. (Initial VDDPA Voltage at RF ON).<br>These values define as well the TX_LDO output voltage in case the DPC is disabled and not used. | 7:0 | 0x00: 1V50<br>0x01: 1V60<br>0x02: 1V70<br>0x03: 1V80<br>0x04: 1V90<br>0x05: 2V00<br>0x06: 2V10<br>0x07: 2V20<br>0x08: 2V30<br>0x09: 2V40<br>0x0A: 2V50<br>0x0B: 2V60<br>0x0C: 2V70<br>0x0D: 2V80<br>0x0E: 2V90<br>0x0F: 3V00 |

Table 108. TXLDO\_VDDPA\_HIGH (address 0006h) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 0X10: 3V10<br>0x11: 3V20<br>0x12: 3V30<br>0x13: 3V40<br>0x14: 3V50<br>0x15: 3V60<br>0x16: 3V70<br>0x17: 3V80<br>0x18: 3V90<br>0x19: 4V00<br>0x1A: 4V10<br>0x1B: 4V20<br>0x1C: 4V30<br>0x1D: 4V40<br>0x1E: 4V50<br>0x1F: 4V60<br>0x20: 4V70<br>0x21: 4V80<br>0x22: 4V90<br>0x23: 5V00<br>0x24: 5V10<br>0x25: 5V20<br>0x26: 5V30<br>0x27: 5V40<br>0x28: 5V50<br>0x29: 5V60<br>0x2A: 5V70 |

9.26.6 TXLDO\_VDDPA\_MAX\_RDR (0008h)

Table 109. TXLDO\_VDDPA\_MAX\_RDR (address 0008h) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description  |
|---------------|--|-----|--|
| 8             | VDDPA maximum output voltage in case the DPC is enabled in reader mode. This is used only when DPC is enabled. This ensures the Maximum Voltage up to which VDDPA reached during DPC Regulation. | 7:0 | 0x00: 1V50<br>0x01: 1V60<br>0x02: 1V70<br>0x03: 1V80<br>0x04: 1V90<br>0x05: 2V00<br>0x06: 2V10<br>0x07: 2V20<br>0x08: 2V30<br>0x09: 2V40<br>0x0A: 2V50<br>0x0B: 2V60<br>0x0C: 2V70<br>0x0D: 2V80 |

Table 109. TXLDO\_VDDPA\_MAX\_RDR (address 0008h) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description |
|---------------|----------|-----|-------------|
|               |          |     | 0x0E: 2V90  |
|               |          |     | 0x0F: 3V00  |
|               |          |     | 0x10: 3V10  |
|               |          |     | 0x11: 3V20  |
|               |          |     | 0x12: 3V30  |
|               |          |     | 0x13: 3V40  |
|               |          |     | 0x14: 3V50  |
|               |          |     | 0x15: 3V60  |
|               |          |     | 0x16: 3V70  |
|               |          |     | 0x17: 3V80  |
|               |          |     | 0x18: 3V90  |
|               |          |     | 0x19: 4V00  |
|               |          |     | 0x1A: 4V10  |
|               |          |     | 0x1B: 4V20  |
|               |          |     | 0x1C: 4V30  |
|               |          |     | 0x1D: 4V40  |
|               |          |     | 0x1E: 4V50  |
|               |          |     | 0x1F: 4V60  |
|               |          |     | 0x20: 4V70  |
|               |          |     | 0x21: 4V80  |
|               |          |     | 0x22: 4V90  |
|               |          |     | 0x23: 5V00  |
|               |          |     | 0x24: 5V10  |
|               |          |     | 0x25: 5V20  |
|               |          |     | 0x26: 5V30  |
|               |          |     | 0x27: 5V40  |
|               |          |     | 0x28: 5V50  |
|               |          |     | 0x29: 5V60  |
|               |          |     | 0x2A: 5V70  |

9.26.7 TXLDO\_VDDPA\_MAX\_CARD (0009h)

Table 110. TXLDO\_VDDPA\_MAX\_CARD (address 0009h) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description |
|---------------|--|-----|-------------|
| 9             | VDDPA maximum output voltage in case the APC is enabled in card mode | 7:0 | 0x00: 1V50  |
|               |  |     | 0x01: 1V60  |
|               |  |     | 0x02: 1V70  |
|               |  |     | 0x03: 1V80  |
|               |  |     | 0x04: 1V90  |
|               |  |     | 0x05: 2V00  |
|               |  |     | 0x06: 2V10  |
|               |  |     | 0x07: 2V20  |
|               |  |     | 0x08: 2V30  |
|               |  |     | 0x09: 2V40  |
|               |  |     | 0x0A: 2V50  |
|               |  |     | 0x0B: 2V60  |

Table 110. TXLDO\_VDDPA\_MAX\_CARD (address 0009h) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description |
|---------------|----------|-----|-------------|
|               |          |     | 0x0C: 2V70  |
|               |          |     | 0x0D: 2V80  |
|               |          |     | 0x0E: 2V90  |
|               |          |     | 0x0F: 3V00  |
|               |          |     | 0x10: 3V10  |
|               |          |     | 0x11: 3V20  |
|               |          |     | 0x12: 3V30  |
|               |          |     | 0x13: 3V40  |
|               |          |     | 0x14: 3V50  |
|               |          |     | 0x15: 3V60  |
|               |          |     | 0x16: 3V70  |
|               |          |     | 0x17: 3V80  |
|               |          |     | 0x18: 3V90  |
|               |          |     | 0x19: 4V00  |
|               |          |     | 0x1A: 4V10  |
|               |          |     | 0x1B: 4V20  |
|               |          |     | 0x1C: 4V30  |
|               |          |     | 0x1D: 4V40  |
|               |          |     | 0x1E: 4V50  |
|               |          |     | 0x1F: 4V60  |
|               |          |     | 0x20: 4V70  |
|               |          |     | 0x21: 4V80  |
|               |          |     | 0x22: 4V90  |
|               |          |     | 0x23: 5V00  |
|               |          |     | 0x24: 5V10  |
|               |          |     | 0x25: 5V20  |
|               |          |     | 0x26: 5V30  |
|               |          |     | 0x27: 5V40  |
|               |          |     | 0x28: 5V50  |
|               |          |     | 0x29: 5V60  |
|               |          |     | 0x2A: 5V70  |

9.26.8 BOOST\_DEFAULT\_VOLTAGE (000Ah)

Table 111. BOOST\_DEFAULT\_VOLTAGE (address 000Ah) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description  |
|---------------|--|-----|--|
| 0A            | DC-DC configuration<br>This Field is Used only in case of Fixed BOOST. In case of Variable BOOST the value is calculated based on the VDDPA. | 7:0 | VDDBOOST output voltage in case of DC-DC with fixed VDDBOOST is enabled (PWR_CONFIG)<br>0x00: 3.1 V<br>0x01: 3.2 V<br>0x02: 3.3 V<br>0x03: 3.4 V<br>0x04: 3.5 V<br>0x05: 3.6 V<br>0x06: 3.7 V<br>0x07: 3.8 V |

Table 111. BOOST\_DEFAULT\_VOLTAGE (address 000Ah) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | 0x08: 3.9 V<br>0x09: 4.0 V<br>0x0A: 4.1 V<br>0x0B: 4.2 V<br>0x0C: 4.3 V<br>0x0D: 4.4 V<br>0x0E: 4.5 V<br>0x0F: 4.6 V<br>0x10: 4.7 V<br>0x11: 4.8 V<br>0x12: 4.9 V<br>0x13: 5.0 V<br>0x14: 5.1 V<br>0x15: 5.2 V<br>0x16: 5.3 V<br>0x17: 5.4 V<br>0x18: 5.5 V<br>0x19: 5.6 V<br>0x1A: 5.7 V<br>0x1B: 5.8 V<br>0x1C: 5.9 V<br>0x1D: 6.0 V<br>all other values: RFU |

### 9.26.9 XTAL\_CONFIG (0010h)

Table 112. XTAL\_CONFIG (address 0010h) EEPROM configuration bit description

| Address (hex) | Function                                     | Bit | Description   |
|---------------|--|-----|---|
| 10            | Configuration for the XTAL startup procedure | 7:1 | RFU   |
|               |  | 0   | Crystal recalibration start after wake-up from standby<br>1: enable<br>0: disable |

### 9.26.10 XTAL\_TIMEOUT (0011h)

Table 113. XTAL\_TIMEOUT (address 0011h) EEPROM configuration bit description

| Address (hex) | Function                                     | Bit | Description  |
|---------------|--|-----|--|
| 11            | Configuration for the XTAL startup procedure | 7:0 | Timeout for XTAL to be ready (in *128us), if the timeout happens, an XTAL error event will be raised.<br>This configuration does not speed up the boot time. |



9.26.11 CLK\_INPUT\_FREQ (0012h)

Table 114. CLK\_INPUT\_FREQ (address 0012h) EEPROM configuration bit description

| Address (hex) | Function  | Bit | Description   |
|---------------|---|-----|---|
| 12            | Configuration for the PLL input clock frequency | 7:4 | RFU   |
|               |   | 3:0 | 0011b: 24 MHz<br>0100b: 32 MHz<br>0101b: 48 MHz<br>1000b: XTAL 27.12 MHz<br>All others: RFU |

9.26.12 XTAL\_CHECK\_DELAY (0013h)

Correct Crystal clocking is detected by locking the crystal to the PLL. This allows the system to start quick independent from the crystal startup time. High-quality crystals will start up typically fast and allow by this optimized current consumption, e.g. during ULPCD.

A user needs to find an optimized balance between retry numbers of checking for a proper locking and the interval for checking for a locked PLL.

This allows to configure a timeout value for locking the crystal to the PLL. The timeout value is defined by **Retry\_number x Interval**. If the timeout is reached, a clock error is raised.

Table 115. XTAL\_CHECK\_DELAY (address 0013h) EEPROM configuration bit description

| Address (hex) | Function            | Bit | Description   |
|---------------|---------------------|-----|---|
| 13            | <b>Retry_number</b> | 7:5 | Max Number of retries before a clock error is raised  |
|               | <b>Interval</b>     | 4:0 | Interval which is used to check if XTAL is ready (unit is 256/fc, e.g. ~18.8 us). This is the time to try to lock the PLL, a stable crystal clock is required for locking. If the PLL is not locked, a next retry to lock the PLL will be done after this interval.<br><br>This value can be used to optimize the startup time dependent on the crystal characteristics. This is important, e.g., for optimization of the LPCD and ULPCD. |

9.26.13 TEMP\_WARNING (0014h)

Table 116. TEMP\_WARNING (address 0014h) EEPROM configuration bit description

| Address (hex) | Function                         | Bit | Description  |
|---------------|----------------------------------|-----|--|
| 14            | CLIF and PMU temperature warning | 7:6 | PMU high threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)  |
|               |                                  | 5:4 | PMU low threshold (0: disabled, 1:114degC, 2:125degC, 3:130degC)   |
|               |                                  | 3:2 | high threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) -<br>in case temp sensor is triggered, transmitter and TX_LDO are shut down, system goes in low-power mode - default is 130 °C. This event is not indicated by an IRQ to the host, instead GPIO0 is used to indicate this critical event (Register PAD_CONFIG 0x52). GPIO0 is set from LOW to HIGH before the IC enters standby.<br>To enable this event on GPIO0, the EEPROM configuration ENABLE_GPIO0_ON_OVERTEMP (0016h) must be set. |

Table 116. TEMP\_WARNING (address 0014h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | <b>Remark:</b> As soon as the chip enters standby, the GPIO0 will go to LOW   |
|               |          | 1:0 | low threshold (0: disabled, 1:114 °C, 2:125 °C, 3:130 °C) - in case temperature sensed is lower than threshold, system wakes up from low-power mode indicated by an IRQ - default is 114 °C.<br>As soon as the chip wakes up, the wake-up source shall be checked to ensure a wake-up due to the low threshold sensing. |

9.26.14 ENABLE\_GPIO0\_ON\_OVERTEMP (0016h)

Table 117. ENABLE\_GPIO0\_ON\_OVERTEMP (address 0016h) EEPROM configuration bit description

| Address (hex) | Function                                 | Bit  | Description   |
|---------------|--|------|---|
| 16            | RFU                                      | 7..1 | -   |
|               | Set/Clear GPIO0 during over temperature. | 0    | If set, the GPIO0 is used to indicate a temperature event.<br>The temperature warning levels are configured in the Register TEMP_WARNING (0014h). |

9.26.15 TX\_SHAPING\_CONFIG (0017h)

Table 118. TX\_SHAPING\_CONFIG (address 0017h) EEPROM configuration register bit description

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
| 17            |          | 7:1 | RFU   |
|               |          | 0   | PWM scheme for RM<br>0: defining 3-levels for drivers TX1/2 - required for balanced antenna (default)<br>1: defining 2-levels for drivers TX1/2 - required for single ended antenna<br>This value is written into CLIF_ANACTROL_TX_CONFIG_REG during Load protocol. |

9.26.16 TX\_INV\_RM (0018h)

Table 119. TX\_INV\_RM (address 0018h) EEPROM configuration register bit description

| Address (hex) | Function                  | Bit | Description   |
|---------------|---------------------------|-----|---|
| 18            | Transmitter configuration | 7:6 | RFU   |
|               |                           | 5   | 0: TX1 non-inverted output (output zero remains zero)<br>1: TX1 inverted output (common mode operation, output zero becomes one)<br>This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol. |
|               |                           | 4   | 0: TX2 non-inverted output (output zero remains zero)<br>1: TX2 inverted output (common mode operation, output zero becomes one)<br>This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol. |
|               |                           | 3:2 | RFU   |
|               |                           | 1   | 0: TX1 no phase shift, 0°   |

Table 119. TX\_INV\_RM (address 0018h) EEPROM configuration register bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 1: TX1 phase shifted by 180°<br>This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol.                              |
|               |          | 0   | 0: TX2 no phase shift, 0°<br>1: TX2 phase shifted by 180°<br>This value is written into CLIF_ANACTROL_TX_CONFIG_REG (0x44) during Load protocol. |

### 9.26.17 TX\_CLK\_MODE\_1 (0019h)

Table 120. TX\_CLK\_MODE\_1 (address 0019h) EEPROM configuration register bit description

| Address (hex) | Function                        | Bit | Description     |
|---------------|---------------------------------|-----|-----------------|
| 19            | Transmitter clock configuration | 7   | RFU             |
|               |                                 | 6:4 | CLK_MODE_CW_RM  |
|               |                                 | 3   | RFU             |
|               |                                 | 2:0 | CLK_MODE_MOD_RM |

### 9.26.18 TX\_CLK\_MODE\_2 (001Ah)

Table 121. TX\_CLK\_MODE\_2 (address 001Ah) EEPROM configuration register bit description

| Address (hex) | Function                        | Bit | Description       |
|---------------|---------------------------------|-----|-------------------|
| 1A            | Transmitter clock configuration | 7   | RFU               |
|               |                                 | 6:4 | CLK_MODE_DEFAULT  |
|               |                                 | 3   | RFU               |
|               |                                 | 2:0 | CLK_MODE_TRANS_RM |

### 9.26.19 RESIDUAL\_AMPL\_LEVEL\_A106 (0022h)

Table 122. RESIDUAL\_AMPL\_LEVEL\_A106 (address 0022h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0% carrier<br>FF: 100% carrier |

## 9.26.20 EDGE\_TYPE\_A106 (0023h)

Table 123. EDGE\_TYPE\_A106 (address 0023h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU            |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

## 9.26.21 EDGE\_STYLE\_A106 (0024h)

Table 124. EDGE\_STYLE\_A106 (address 0024h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

## 9.26.22 EDGE\_LENGTH\_A106 (0025h)

Table 125. EDGE\_LENGTH\_A106 (address 0025h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

## 9.26.23 RESIDUAL\_AMPL\_LEVEL\_A212 (0026h)

Table 126. RESIDUAL\_AMPL\_LEVEL\_A212 (address 0026h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.24 EDGE\_TYPE\_A212 (0027h)

Table 127. EDGE\_TYPE\_A212 (address 0027h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 127. EDGE\_TYPE\_A212 (address 0027h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.25 EDGE\_STYLE\_A212 (0028h)

Table 128. EDGE\_STYLE\_A212 (address 0028h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.26 EDGE\_LENGTH\_A212 (0029h)

Table 129. EDGE\_LENGTH\_A212 (address 0029h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.27 RESIDUAL\_AMPL\_LEVEL\_A424 (002Ah)

Table 130. RESIDUAL\_AMPL\_LEVEL\_A424 (address 002Ah) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 2A            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.28 EDGE\_TYPE\_A424 (002Bh)

Table 131. EDGE\_TYPE\_A424 (address 002Bh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.29 EDGE\_STYLE\_A424 (002Ch)

Table 132. EDGE\_STYLE\_A424 (address 002Ch) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.30 EDGE\_LENGTH\_A424 (002Dh)

Table 133. EDGE\_LENGTH\_A424 (address 002Dh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.31 RESIDUAL\_AMPL\_LEVEL\_A848 (002Eh)

Table 134. RESIDUAL\_AMPL\_LEVEL\_A848 (address 002Eh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

### 9.26.32 EDGE\_TYPE\_A848 (002Fh)

Table 135. EDGE\_TYPE\_A848 (address 002Fh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |



Table 135. EDGE\_TYPE\_A848 (address 002Fh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

9.26.33 EDGE\_STYLE\_A848 (0030h)

Table 136. EDGE\_STYLE\_A848 (address 0030h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.34 EDGE\_LENGTH\_A848 (0031h)

Table 137. EDGE\_LENGTH\_A848 (address 0031h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.35 RESIDUAL\_AMPL\_LEVEL\_B106 (0032h)

Table 138. RESIDUAL\_AMPL\_LEVEL\_B106 (address 0032h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.36 EDGE\_TYPE\_B106 (0033h)

Table 139. EDGE\_TYPE\_B106 (address 0033h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

## 9.26.37 EDGE\_STYLE\_B106 (0034h)

Table 140. EDGE\_STYLE\_B106 (address 0034h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.38 EDGE\_LENGTH\_B106 (0035h)

Table 141. EDGE\_LENGTH\_B106 (address 0035h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.39 RESIDUAL\_AMPL\_LEVEL\_B212 (0036h)

Table 142. RESIDUAL\_AMPL\_LEVEL\_B212 (address 0036h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.40 EDGE\_TYPE\_B212 (0037h)

Table 143. EDGE\_TYPE\_B212 (address 0037h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA  |

Table 143. EDGE\_TYPE\_B212 (address 0037h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.41 EDGE\_STYLE\_B212 (0038h)

Table 144. EDGE\_STYLE\_B212 (address 0038h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.42 EDGE\_LENGTH\_B212 (0039h)

Table 145. EDGE\_LENGTH\_B212 (address 0039h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.43 RESIDUAL\_AMPL\_LEVEL\_B424 (003Ah)

Table 146. RESIDUAL\_AMPL\_LEVEL\_B424 (address 003Ah) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.44 EDGE\_TYPE\_B424 (003Bh)

Table 147. EDGE\_TYPE\_B424 (address 003Bh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

## 9.26.45 EDGE\_STYLE\_B424 (003Ch)

Table 148. EDGE\_STYLE\_B424 (address 003Ch) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description   |
|---------------|--|-----|---|
| 24            | RFU  | 7   | -   |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1,2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -   |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1,2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

## 9.26.46 EDGE\_LENGTH\_B424 (003Dh)

Table 149. EDGE\_LENGTH\_B424 (address 003Dh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

## 9.26.47 RESIDUAL\_AMPL\_LEVEL\_B848 (003Eh)

Table 150. RESIDUAL\_AMPL\_LEVEL\_B848 (address 003Eh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.48 EDGE\_TYPE\_B848 (003Fh)

Table 151. EDGE\_TYPE\_B848 (address 003Fh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 151. EDGE\_TYPE\_B848 (address 003Fh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.49 EDGE\_STYLE\_B848 (0040h)

Table 152. EDGE\_STYLE\_B848 (address 0040h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.50 EDGE\_LENGTH\_B848 (0041h)

Table 153. EDGE\_LENGTH\_B848 (address 0041h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.51 RESIDUAL\_AMPL\_LEVEL\_F212 (0042h)

Table 154. RESIDUAL\_AMPL\_LEVEL\_F212 (address 0042h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.52 EDGE\_TYPE\_F212 (0043h)

Table 155. EDGE\_TYPE\_F212 (address 0043h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.53 EDGE\_STYLE\_F212 (0044h)

Table 156. EDGE\_STYLE\_F212 (address 0044h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |



### 9.26.54 EDGE\_LENGTH\_F212 (0045h)

Table 157. EDGE\_LENGTH\_F212 (address 0045h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.55 RESIDUAL\_AMPL\_LEVEL\_F424 (0046h)

Table 158. RESIDUAL\_AMPL\_LEVEL\_F424 (address 0046h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

### 9.26.56 EDGE\_TYPE\_F424 (0047h)

Table 159. EDGE\_TYPE\_F424 (address 0047h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 159. EDGE\_TYPE\_F424 (address 0047h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.57 EDGE\_STYLE\_F424 (0048h)

Table 160. EDGE\_STYLE\_F424 (address 0048h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.58 EDGE\_LENGTH\_F424 (0049h)

Table 161. EDGE\_LENGTH\_F424 (address 0049h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.59 RESIDUAL\_AMPL\_LEVEL\_V100\_26 (004Ah)

Table 162. RESIDUAL\_AMPL\_LEVEL\_V100\_26 (address 004Ah) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.60 EDGE\_TYPE\_V100\_26 (004Bh)

Table 163. EDGE\_TYPE\_V100\_26 (address 004Bh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

## 9.26.61 EDGE\_STYLE\_V100\_26 (004Ch)

Table 164. EDGE\_STYLE\_V100\_26 (address 004Ch) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.62 EDGE\_LENGTH\_V100\_26 (004Dh)

Table 165. EDGE\_LENGTH\_V100\_26 (address 004Dh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.63 RESIDUAL\_AMPL\_LEVEL\_V100\_53 (004Eh)

Table 166. RESIDUAL\_AMPL\_LEVEL\_V100\_53 (address 004Eh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.64 EDGE\_TYPE\_V100\_53 (004Fh)

Table 167. EDGE\_TYPE\_V100\_53 (address 004Fh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 167. EDGE\_TYPE\_V100\_53 (address 004Fh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

9.26.65 EDGE\_STYLE\_V100\_53 (0050h)

Table 168. EDGE\_STYLE\_A106 (address 0050h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.66 EDGE\_LENGTH\_V100\_53 (0051h)

Table 169. EDGE\_LENGTH\_V100\_53 (address 0051h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.67 RESIDUAL\_AMPL\_LEVEL\_V100\_106 (0052h)

Table 170. RESIDUAL\_AMPL\_LEVEL\_V100\_106 (address 0052h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.68 EDGE\_TYPE\_V100\_106 (0053h)

Table 171. EDGE\_TYPE\_V100\_106 (address 0053h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.69 EDGE\_STYLE\_V100\_106 (0054h)

Table 172. EDGE\_STYLE\_V100\_106 (address 0054h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.70 EDGE\_LENGTH\_V100\_106 (0055h)

Table 173. EDGE\_LENGTH\_V100\_106 (address 0055h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.71 RESIDUAL\_AMPL\_LEVEL\_100\_212 (0056h)

Table 174. RESIDUAL\_AMPL\_LEVEL\_100\_212 (address 0056h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.72 EDGE\_TYPE\_V100\_212 (0057h)

Table 175. EDGE\_TYPE\_V100\_212 (address 0057h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 175. EDGE\_TYPE\_V100\_212 (address 0057h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.73 EDGE\_STYLE\_V100\_212 (0058h)

Table 176. EDGE\_STYLE\_V100\_212 (address 0058h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.74 EDGE\_LENGTH\_V100\_212 (0059h)

Table 177. EDGE\_LENGTH\_V100\_212 (address 0059h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.75 RESIDUAL\_AMPL\_LEVEL\_V10\_26 (005Ah)

Table 178. RESIDUAL\_AMPL\_LEVEL\_V10\_26 (address 005Ah) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |



9.26.76 EDGE\_TYPE\_V10\_26 (005Bh)

Table 179. EDGE\_TYPE\_V10\_26 (address 005Bh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.77 EDGE\_STYLE\_V10\_26 (005Ch)

Table 180. EDGE\_STYLE\_V10\_26 (address 005Ch) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

## 9.26.78 EDGE\_LENGTH\_V10\_26 (005Dh)

Table 181. EDGE\_LENGTH\_V10\_26 (address 005Dh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

## 9.26.79 RESIDUAL\_AMPL\_LEVEL\_V10\_53 (005Eh)

Table 182. RESIDUAL\_AMPL\_LEVEL\_V10\_53 (address 005Eh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.80 EDGE\_TYPE\_V10\_53 (005Fh)

Table 183. EDGE\_TYPE\_V10\_53 (address 005Fh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 183. EDGE\_TYPE\_V10\_53 (address 005Fh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

9.26.81 EDGE\_STYLE\_V10\_53 (0060h)

Table 184. EDGE\_STYLE\_V10\_53 (address 0060h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.82 EDGE\_LENGTH\_V10\_53 (0061h)

Table 185. EDGE\_LENGTH\_V10\_53 (address 0061h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.83 RESIDUAL\_AMPL\_LEVEL\_V10\_106 (0062h)

Table 186. RESIDUAL\_AMPL\_LEVEL\_V10\_106 (address 0062h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.84 EDGE\_TYPE\_V10\_106 (0063h)

Table 187. EDGE\_TYPE\_V10\_106 (address 0063h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

## 9.26.85 EDGE\_STYLE\_V10\_106 (0064h)

Table 188. EDGE\_STYLE\_V100\_212 (address 0064h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

## 9.26.86 EDGE\_LENGTH\_V10\_106 (0065h)

Table 189. EDGE\_LENGTH\_V10\_106 (address 0065h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

## 9.26.87 RESIDUAL\_AMPL\_LEVEL\_V10\_212 (0066h)

Table 190. RESIDUAL\_AMPL\_LEVEL\_V10\_212 (address 0066h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.88 EDGE\_TYPE\_V10\_212 (0067h)

Table 191. EDGE\_TYPE\_V10\_212 (address 0067h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction  |

Table 191. EDGE\_TYPE\_V10\_212 (address 0067h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.89 EDGE\_STYLE\_V10\_212 (0068h)

Table 192. EDGE\_STYLE\_V10\_212 (address 0068h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.90 EDGE\_LENGTH\_V10\_212 (0069h)

Table 193. EDGE\_LENGTH\_V100\_212 (address 0069h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.91 RESIDUAL\_AMPL\_LEVEL\_180003m3\_tari18p88 (006Ah)

Table 194. RESIDUAL\_AMPL\_LEVEL\_180003m3\_tari18p88 (address 006Ah) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.92 EDGE\_TYPE\_180003m3\_tari18p88 (006Bh)

Table 195. EDGE\_TYPE\_180003m3\_tari18p88 (address 006Bh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.93 EDGE\_STYLE\_180003m3\_tari18p88 (006Ch)

Table 196. EDGE\_STYLE\_180003m3\_tari18p88 (address 006Ch) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

## 9.26.94 EDGE\_LENGTH\_180003m3\_tari18p88 (006Dh)

Table 197. EDGE\_LENGTH\_180003m3\_tari18p88 (address 006Dh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

## 9.26.95 RESIDUAL\_AMPL\_LEVEL\_180003m3\_tari9p44 (006Eh)

Table 198. RESIDUAL\_AMPL\_LEVEL\_180003m3\_tari9p44 (address 006Eh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

## 9.26.96 EDGE\_TYPE\_180003m3\_tari9p44 (006Fh)

Table 199. EDGE\_TYPE\_180003m3\_tari9p44 (address 006Fh) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA  |



Table 199. EDGE\_TYPE\_180003m3\_tari9p44 (address 006Fh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |

### 9.26.97 EDGE\_STYLE\_180003m3\_tari9p44 (0070h)

Table 200. EDGE\_STYLE\_180003m3\_tari9p44 (address 0070h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

### 9.26.98 EDGE\_LENGTH\_180003m3\_tari9p44 (0071h)

Table 201. EDGE\_LENGTH\_180003m3\_tari9p44 (address 0071h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

### 9.26.99 RESIDUAL\_AMPL\_LEVEL\_B\_PRIME\_106 (0072h)

Table 202. RESIDUAL\_AMPL\_LEVEL\_180003m3\_tari18p88 (address 0072h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description  |
|---------------|-----------------------------------|-----|--|
| 22            | Transmitter shaping configuration | 7:0 | Residual amplitude level<br>00: 0 % carrier<br>FF: 100 % carrier |

9.26.100 EDGE\_TYPE\_B\_PRIME\_106 (0073h)

Table 203. EDGE\_TYPE\_B\_PRIME\_106 (address 0073h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 23            | Transmitter shaping configuration | 7:4 | Definition of edge transition style of falling edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU |
|               |                                   | 3:0 | Definition of edge transition style of rising edge<br>Defines style of edge transition:<br>Firmware based shaping:<br>1: linear transition between two amplitude levels<br>2: two linear transitions between amplitude levels<br>3: three linear transitions between amplitude levels Others: RFU<br>Lookup table based shaping:<br>4: lookup table-based transition, no automatic adaptation based on VDDPA<br>5: lookup table-based transition, automatic adaptation based on VDDPA including s Correction<br>6: lookup table-based transition, automatic adaptation based on VDDPA but no s Correction<br>others: RFU  |

9.26.101 EDGE\_STYLE\_B\_PRIME\_106 (0074h)

Table 204. EDGE\_STYLE\_B\_PRIME\_106 (address 0074h) EEPROM configuration bit description

| Address (hex) | Function                                       | Bit | Description  |
|---------------|--|-----|--|
| 24            | RFU  | 7   | -  |
|               | Transmitter shaping configuration falling edge | 6:4 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of falling edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of falling edge (0,1,2,3) |
|               | RFU  | 3   | -  |
|               | Transmitter shaping configuration rising edge  | 2:0 | If EDGE_TYPE is 1, 2 or 3:<br>Time constant configuration of rising edge (depends on edge style)<br>If EDGE_TYPE is 4,5,6:<br>This number is the lookup table which shall be used of rising edge (0,1,2,3)   |

9.26.102 EDGE\_LENGTH\_B\_PRIME\_106 (0075h)

Table 205. EDGE\_LENGTH\_B\_PRIME\_106 (address 0075h) EEPROM configuration bit description

| Address (hex) | Function                          | Bit | Description   |
|---------------|-----------------------------------|-----|---|
| 25            | Transmitter shaping configuration | 7   | Scaling of edge transition by factor 2 of rising/falling edge (refers to both rising and falling edge at the same time)<br>0=disabled (1 transition state = one carrier cycle)<br>1=enabled (1 transition state = two carrier cycles) |
|               |                                   | 6:5 | RFU   |
|               |                                   | 4:0 | Number of active transition states in rising and falling edge pattern (refers to both rising and falling edge at the same time)   |

9.26.103 DPC\_CONFIG (0076h)

Table 206. DPC\_CONFIG (address 0076h) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description  |
|---------------|-------------------|-----|--|
| 76            | DPC Configuration | 7:3 | RFU  |
|               |                   | 2   | DPC in Active Target Mode:<br>0: disabled,<br>1: enabled             |
|               |                   | 1   | DPC in Active Initiator Mode:<br>0: disabled,<br>1: enabled          |
|               |                   | 0   | DPC in Reader/ Passive Initiator Mode:<br>0: disabled,<br>1: enabled |

9.26.104 DPC\_TARGET\_CURRENT (077h)

Table 207. DPC\_TARGET\_CURRENT (address 077h) EEPROM configuration bit description

| Address (hex) | Function          | Bit  | Description   |
|---------------|-------------------|------|---|
| 77            | DPC Configuration | 15:0 | VDDPA target current in mA. The target current +/- hysteresis defines the limiting maximum current for the DPC.<br>This configuration shall not exceed 350 mA - hysteresis. |

**Note:** The resulting current that is driven by the transmitter can be further reduced based on the current reduction lookup table entries.

9.26.105 DPC\_HYSTERESIS\_LOADING (079h)

The hysteresis (DPC\_HYSTERESIS\_LOADING, DPC\_HYSTERESIS\_UNLOADING) together with the target current (DPC\_TARGET\_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC\_TARGET\_CURRENT + DPC\_HYSTERESIS\_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC\_TARGET\_CURRENT – DPC\_HYSTERESIS\_UNLOADING.

Table 208. DPC\_HYSTERESIS\_LOADING (address 079h) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description   |
|---------------|-------------------|-----|---|
| 79            | DPC Configuration | 7:0 | Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during loading. |

**Note:** If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.

**Note:** In most application, the default values work well and do not need to be modified.

### 9.26.106 DPC\_HYSTERESIS\_UNLOADING (07Ch)

The hysteresis (DPC\_HYSTERESIS\_LOADING, DPC\_HYSTERESIS\_UNLOADING) together with the target current (DPC\_TARGET\_CURRENT) defines the current limit, at which the DPC automatically decreases or increases the VDDPA.

The VDDPA is automatically reduced, as soon as the current exceeds the DPC\_TARGET\_CURRENT + DPC\_HYSTERESIS\_LOADING, and the VDDPA is automatically increased again, as soon as the current is below DPC\_TARGET\_CURRENT – DPC\_HYSTERESIS\_UNLOADING.

Table 209. DPC\_HYSTERESIS\_UNLOADING (address 07Ch) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description   |
|---------------|-------------------|-----|---|
| 7C            | DPC Configuration | 7:0 | Absolute difference of measured transmitter current (target current incl. current reduction) in mA that triggers a DPC update event during unloading. |

**Note:** If the hysteresis is configured too small, it might cause an oscillation of the transmitted field.

**Note:** In most application, the default values work well and do not need to be modified.

### 9.26.107 DPC\_TXLDOVDDPALow (007Dh)

Table 210. DPC\_TXLDOVDDPALow (address 007Dh) EEPROM configuration register bit description

| Address (hex) | Function          | Bit | Description              |
|---------------|-------------------|-----|--------------------------|
| 7D            | DPC Configuration | 7:0 | VDDPA Low Limit for RDON |

### 9.26.108 DPC\_TXGSN (007Eh)

Table 211. DPC\_TXGSN (address 007Eh) EEPROM configuration register bit description

| Address (hex) | Function          | Bit | Description  |
|---------------|-------------------|-----|--|
| 7E            | DPC Configuration | 7:0 | for tx1_gsn < 20: resistance = 10 Ohm / (tx1_gsn + 1)<br>for tx1_gsn >= 20: resistance = 0.5 Ohm |

### 9.26.109 DPC\_RDON\_Control (007Fh)

Table 212. DPC\_RDON\_Control (address 007Fh) EEPROM configuration register bit description

| Address (hex) | Function          | Bit | Description                      |
|---------------|-------------------|-----|----------------------------------|
| 7F            | DPC Configuration | 7:0 | 00: Disabled<br>01: RdON Control |

Table 212. DPC\_RDON\_Control (address 007Fh) EEPROM configuration register bit description

| Address (hex) | Function | Bit | Description |
|---------------|----------|-----|-------------|
|               |          |     | 02-FF: RFU  |

### 9.26.110 DPC\_InitialRDOOn\_RFOn (0080h)

Table 213. DPC\_InitialRDOOn\_RFOn (address 0080h) EEPROM configuration register bit description

| Address (hex) | Function          | Bit | Description                              |
|---------------|-------------------|-----|--|
| 80            | DPC Configuration | 7:0 | Initial GSP TX1/TX2 value during FieldON |

### 9.26.111 DPC\_TXLDO\_MAX\_DROP (0081h)

Table 214. DPC\_TXLDO\_MAX\_DROP (address 0081h) EEPROM configuration register bit description

| Address (hex) | Function          | Bit | Description  |
|---------------|-------------------|-----|--|
| 81            | DPC Configuration |     | At DPC start (on initial RF ON), if TXLDO drop out is higher to this value then VDDPA is reduced to: eVddpaSafe if no boost bypass on going else Vddpa is stopped. Unit is mV. Default = E10h = 3600mV |

### 9.26.112 DPC\_GUARD\_TIME (087h)

Table 215. DPC\_GUARD\_TIME (address 087h) EEPROM configuration bit description

| Address (hex) | Function                     | Bit | Description  |
|---------------|------------------------------|-----|--|
| 87            | DPC guard time configuration | 7:0 | Guard time before TX and after RX. 1unit = 1us.<br>The DPC regulation is done once before TX and once after RX.<br>The guard time parameter is the time between DPC regulation completion and TX start.<br>The guard time parameter is the time between RX stop and DPC regulation start.<br>The guard time is always enabled for TX |

**Note:** Recommendation is not to modify the default value.

### 9.26.113 DPC\_ENABLE\_DURING\_FDT (088h)

Table 216. DPC\_ENABLE\_DURING\_FDT (address 088h) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description   |
|---------------|-------------------|-----|---|
| 88            | RFU               | 7-1 | -   |
|               | DPC Configuration | 0   | DPC regulation enable during FDT<br>0: DPC disabled during FDT (debug purpose only)<br>1: DPC enabled during FDT (recommendation) |

## 9.26.114 DPC\_GUARD\_TIME\_AFTER\_RX (089h)

Table 217. DPC\_GUARD\_TIME\_AFTER\_RX (address 089h) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description   |
|---------------|-------------------|-----|---|
| 89            | RFU               | 7:1 | -   |
| 89            | DPC Configuration | 0   | Enable DPC guard time after RX<br>0: disable (debug purposes)<br>1: enable (recommended)<br>The guard time can be configured in register DPC_GUARD_TIME |

**Note:** The guard time is always enabled for TX and cannot be disabled.

## 9.26.115 DPC\_LOOKUP\_TABLE (008Bh-0133h)

Table 218. DPC\_LOOKUP\_TABLE (008Bh-0133h) EEPROM configuration bit description

| Address (hex) | Function                                 | Bit   | Description   |
|---------------|--|-------|---|
|               | ENTRY 0                                  | 31:0  | This is the entry for 1.5 V   |
| 08B           | Target current reduction                 | 31:23 | ENTRY 0 -LSB - byte 0<br>Voltage step between DPC entries = 100 mV. Voltage offset start = 1.5 V bEntry_00 = 1V5 ... bEntry_42 = 5V7<br>Bits[7:0] = Target current reduction in mA (unsigned) |
| 08C           | AWC amp mod change                       | 23:16 | ENTRY 0 - byte 1<br>Bits[7:0] = Relative change of modulated amplitude level (signed)   |
| 08D           | AWC edge time constant for ASK100        | 15:8  | ENTRY 0 - byte 2<br>Bits[3:0] = ASK100, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK100, Relative change of rising edge time constant (signed)                   |
| 08E           | AWC falling edge time constant for ASK10 | 7:0   | ENTRY 0 -MSB - byte 4<br>Bits[3:0] = ASK10, Relative change of falling edge time constant (signed)<br>Bits[7:4] = ASK10, Relative change of rising edge time constant (signed)                |
| 08F           | ENTRY 1                                  | 31:0  | This is the entry for 1.6 V   |
| ....          |  |       | ....  |
| 093           | ENTRY 2                                  | 31:0  | This is the entry for 1.7 V   |
| .....         |  |       | ....  |
| ....          |  |       | This is the entry for 5.6 V   |
| 0133          | ENTRY 42                                 | 31:0  | This is the entry for 5.7 V   |

## 9.26.116 ARC\_CONFIG (0137h)

Table 219. ARC\_CONFIG (address 0137h) EEPROM configuration bit description

| Address (hex) | Function                  | Bit | Description                        |
|---------------|---------------------------|-----|------------------------------------|
| 137           | ARC Setting configuration | 7   | ARC algorithm enable<br>0: Disable |

Table 219. ARC\_CONFIG (address 0137h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 1: Enable  |
|               |          | 6:3 | RFU  |
|               |          | 2:0 | Number of entries in ARC table. (value between 0 to 4)<br>0: one entry<br>1: two entries<br>2: three entries<br>3: four entries<br>4: five entries |

9.26.117 ARC\_VDDPA (0139h)

Table 220. ARC\_VDDPA (0139Eh) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
| 13D           | VDDPA_4  | 7:0 | Byte[4] = VDDPA_range_index 4: if VDDPA voltage between VDDPA_3 to ARC_VDDPA_4         |
| 13C           | VDDPA_3  | 7:0 | Byte[3] = VDDPA_range_index 3: if VDDPA voltage between VDDPA_2 to ARC_VDDPA_3 - 0.1   |
| 13B           | VDDPA_2  | 7:0 | Byte[2] = VDDPA_range_index 2: if VDDPA voltage between VDDPA_1 to ARC_VDDPA_2 - 0.1   |
| 13A           | VDDPA_1  | 7:0 | Byte[1] = VDDPA_range_index 1: if VDDPA voltage between VDDPA_0 to (ARC_VDDPA_1 - 0.1) |
| 139           | VDDPA_0  | 7:0 | Byte[0] = VDDPA_range_index 0: if VDDPA voltage between 1.5 to (VDDPA_0 - 0.1)         |

**Note:** VDDPA setting for Bytes 0...4:

- 0x00: 1V50
- 0x01: 1V60
- 0x02: 1V70
- 0x03: 1V80
- 0x04: 1V90
- 0x05: 2V00
- 0x06: 2V10
- 0x07: 2V20
- 0x08: 2V30
- 0x09: 2V40
- 0x0A: 2V50
- 0x0B: 2V60
- 0x0C: 2V70
- 0x0D: 2V80

*0x0E: 2V90**0x0F: 3V00**0x10: 3V10**0x11: 3V20**0x12: 3V30**0x13: 3V40**0x14: 3V50**0x15: 3V60**0x16: 3V70**0x17: 3V80**0x18: 3V90**0x19: 4V00**0x1A: 4V10**0x1B: 4V20**0x1C: 4V30**0x1D: 4V40**0x1E: 4V50**0x1F: 4V60**0x20: 4V70**0x21: 4V80**0x22: 4V90**0x23: 5V00**0x24: 5V10**0x25: 5V20**0x26: 5V30**0x27: 5V40**0x28: 5V50**0x29: 5V60**0x2A: 5V70***9.26.118 ARC\_RM\_A106 (013Eh)**

This is the setting for type A-106.

**Table 221. ARC\_RM\_A106 (address 013Eh) EEPROM configuration bit description**

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 146           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>This setting is only taken into account if bit 14 of address 13E is set. |



Table 221. ARC\_RM\_A106 (address 013Eh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 144           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>This setting is only taken into account if bit 14 of address 13E is set.<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 142           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>This setting is only taken into account if bit 14 of address 13E is set.<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 140           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>This setting is only taken into account if bit 14 of address 13E is set.<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 13E           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>This setting is only taken into account if bit 14 of address 13E is set.<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A106_FDT are used, else bits 0..9 of table ARC_RM_A106 are used<br>Bit [14]:  |

Table 221. ARC\_RM\_A106 (address 013Eh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | 1: ARC enabled for this Tech and Baudrate.<br>0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

9.26.119 ARC\_RM\_A212 (0148h)

This is the setting for type A-212.

Table 222. ARC\_RM\_A212 (address 0148h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 150           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 14E           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 14C           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)   |

Table 222. ARC\_RM\_A212 (address 0148h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 14A           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A212 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 148           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                               |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.120 ARC\_RM\_A424 (0152h)

This is the setting for type A-424.

Table 223. ARC\_RM\_A424 (address 0152h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 15A           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

Table 223. ARC\_RM\_A424 (address 0152h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 158           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 156           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 154           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_A424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A424 are used, else settings will be used from LoadProtocol A424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 152           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.121 ARC\_RM\_A848 (015Ch)

This is the setting for type A-848.

Table 224. ARC\_RM\_A848 (address 015Ch) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 164           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 162           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 160           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 15E           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_A848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_A848 are used, else settings will be used from LoadProtocol A848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 15C           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.  |

Table 224. ARC\_RM\_A848 (address 015Ch) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.122 ARC\_RM\_B106 (0166h)

This is the setting for type B-106.

Table 225. ARC\_RM\_B106 (address 0166h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 16E           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 16C           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 16A           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 168           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B106 are used   |

Table 225. ARC\_RM\_B106 (address 0166h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B106 are used, else settings will be used from LoadProtocol B106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 166           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.123 ARC\_RM\_B212 (0170h)

This is the setting for type B-212.

Table 226. ARC\_RM\_B212 (address 0170h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 178           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 176           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.  |

Table 226. ARC\_RM\_B212 (address 0170h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 174           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 172           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B212 are used, else settings will be used from LoadProtocol B212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 170           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.124 ARC\_RM\_B424 (017Ah)

This is the setting for type B-424.

Table 227. ARC\_RM\_B424 (address 017Ah) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description |
|---------------|-------------|------|-------------|
| 182           | RM_RX_ARC_4 | 15:0 | Bit[15]     |



Table 227. ARC\_RM\_B424 (address 017Ah) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 0: ARC settings always apply, bits 0..9 from the table ARC_RM_B424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)            |
| 180           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_B424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 17E           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_B424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 17C           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_B424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B424 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 17A           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)   |

Table 227. ARC\_RM\_B424 (address 017Ah) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.125 ARC\_RM\_B848 (0184h)

This is the setting for type B-848.

Table 228. ARC\_RM\_B848 (address 0184h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 18C           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 18A           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 188           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 186           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_B848 are used   |

Table 228. ARC\_RM\_B848 (address 0184h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 1: ARC settings during FDT, bits 0..9 of table ARC_RM_B848 are used, else settings will be used from LoadProtocol B848<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 184           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.126 ARC\_RM\_F212 (018Eh)

This is the setting for type F-212.

Table 229. ARC\_RM\_F212 (address 018Eh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 196           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 194           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.  |

Table 229. ARC\_RM\_F212 (address 018Eh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 192           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 190           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_F212 are used, else settings will be used from LoadProtocol F212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 18E           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)               |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

**9.26.127 ARC\_RM\_F424 (0198h)**

This is the setting for type F-424.

Table 230. ARC\_RM\_F424 (address 0198h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 1A0           | RM_RX_ARC_4 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F424 are used<br/>           1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 19E           | RM_RX_ARC_3 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F424 are used<br/>           1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 19C           | RM_RX_ARC_2 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F424 are used<br/>           1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 19A           | RM_RX_ARC_1 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0..9 from the table ARC_RM_F424 are used<br/>           1: ARC settings during FDT, bits 0..9 of table ARC_RM_F424 are used, else settings will be used from LoadProtocol F424</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 198           | RM_RX_ARC_0 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply<br/>           1: ARC settings applicable during FDT and DPC change</p> <p>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate</p> <p>Bits[13:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p>  |

Table 230. ARC\_RM\_F424 (address 0198h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.128 ARC\_RM\_V\_6p6 (01A2h)

This is the setting for type A-106.

Table 231. ARC\_RM\_V\_6p6 (address 01A2h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 1AA           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1A8           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1A6           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1A4           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V6P6 are used   |

Table 231. ARC\_RM\_V\_6p6 (address 01A2h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 1: ARC settings during FDT, bits 0..9 of table ARC_RM_V6P6 are used, else settings will be used from LoadProtocol V6P6<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 1A2           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.129 ARC\_RM\_V\_26 (01ACh)

This is the setting for type V 26.

Table 232. ARC\_RM\_V\_26 (address 01ACh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 1B4           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V26 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1B2           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V26 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.  |

Table 232. ARC\_RM\_V\_26 (address 01ACh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)  |
| 1B0           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1AE           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_V26 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V26 are used, else settings will be used from LoadProtocol V26<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1AC           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)             |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

### 9.26.130 ARC\_RM\_V53 (01B6h)

This is the setting for type V53.

Table 233. ARC\_RM\_V53(address 01B6h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description |
|---------------|-------------|------|-------------|
| 1BE           | RM_RX_ARC_4 | 15:0 | Bit[15]     |



Table 233. ARC\_RM\_V53(address 01B6h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | 0: ARC settings always apply, bits 0..9 from the table ARC_RM_V53 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)            |
| 1BC           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V53 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1BA           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V53 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1B8           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V53 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V53 are used, else settings will be used from LoadProtocol V53<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1B6           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)  |

Table 233. ARC\_RM\_V53(address 01B6h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
|               |          |     | Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.131 ARC\_RM\_V106 (01C0h)

This is the setting for type V106.

Table 234. ARC\_RM\_V106(address 01C0h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1C8           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1C6           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1C4           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1C2           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V106 are used, else settings will be used from LoadProtocol A212   |

Table 234. ARC\_RM\_V106(address 01C0h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 1C0           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.132 ARC\_RM\_V212 (01CAh)

This is the setting for type V212.

Table 235. ARC\_RM\_V212(address 01CAh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1D2           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1D0           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)   |

Table 235. ARC\_RM\_V212(address 01CAh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 1CE           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1CC           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_V212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_V212 are used, else settings will be used from LoadProtocol V212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1CA           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)               |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

### 9.26.133 ARC\_RM\_180003m3\_SC424\_4Man (01D4h)

This is the setting for type 180003m3\_SC424\_4Man.

Table 236. ARC\_RM\_180003m3\_SC424\_4Man (address 01D4h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description |
|---------------|-------------|------|-------------|
| 1DC           | RM_RX_ARC_4 | 15:0 | Bit[15]     |

Table 236. ARC\_RM\_180003m3\_SC424\_4Man (address 01D4h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | <p>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used</p> <p>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p>                |
| 1DA           | RM_RX_ARC_3 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used</p> <p>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 1D8           | RM_RX_ARC_2 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used</p> <p>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 1D6           | RM_RX_ARC_1 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_4MAN are used</p> <p>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_4MAN</p> <p>Bits[14:10] = RFU</p> <p>Bit [9] = Enable the IIR filter.</p> <p>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)</p> <p>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)</p> |
| 1D4           | RM_RX_ARC_0 | 15:0 | <p>Bit[15]</p> <p>0: ARC settings always apply</p> <p>1: ARC settings applicable during FDT and DPC change</p> <p>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate</p> <p>Bits[13:10] = RFU</p>  |

Table 236. ARC\_RM\_180003m3\_SC424\_4Man (address 01D4h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.134 ARC\_RM\_180003m3\_SC424\_2Man (01DEh)

This is the setting for type 180003m3\_SC424\_2Man.

Table 237. ARC\_RM\_180003m3\_SC424\_2Man (address 01DEh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1E6           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1E4           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1E2           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN<br>Bits[14:9] = RFU<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)  |

Table 237. ARC\_RM\_180003m3\_SC424\_2Man (address 01DEh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 1E0           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC424_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC424_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC424_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1DE           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.135 ARC\_RM\_180003m3\_SC848\_4Man (01E8h)

This is the setting for type 180003m3\_SC848\_4Man.

Table 238. ARC\_RM\_180003m3\_SC848\_4Man (address 01E8h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1F0           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1EE           | RM_RX_ARC_3 | 15:0 | Bit[15]  |

Table 238. ARC\_RM\_180003m3\_SC848\_4Man (address 01E8h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
|               |             |      | 0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)            |
| 1EC           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1EA           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_4MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_4MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_4MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1E8           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.



9.26.136 ARC\_RM\_180003m3\_SC848\_2Man (01F2h)

This is the setting for type 180003m3\_SC848\_2Man.

Table 239. ARC\_RM\_180003m3\_SC848\_2Man (address 01F2h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1FA           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                                     |
| 1F8           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                                     |
| 1F6           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1F4           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_180003M3_SC848_2MAN are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_180003M3_SC848_2MAN are used, else settings will be used from LoadProtocol 180003M3_SC848_2MAN<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                                     |

Table 239. ARC\_RM\_180003m3\_SC848\_2Man (address 01F2h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 1F2           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.137 ARC\_RM\_AI106 (01FCh)

This is the setting for type AI106.

Table 240. ARC\_RM\_AI106 (address 01FCh) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 204           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 202           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 200           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106<br>Bits[14:10] = RFU  |

Table 240. ARC\_RM\_AI106 (address 01FCh) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
|               |             |      | Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| 1FE           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_AI106 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI106 are used, else settings will be used from LoadProtocol AI106<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 1FC           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                  |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.138 ARC\_RM\_AI212 (0206h)

This is the setting for type AI212.

Table 241. ARC\_RM\_AI212 (0206h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 20E           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_AI212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

Table 241. ARC\_RM\_AI212 (0206h) EEPROM configuration bit description...continued

| Address (hex) | Function    | Bit  | Description   |
|---------------|-------------|------|---|
| 20C           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_AI212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 20A           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_AI212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 208           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0..9 from the table ARC_RM_AI212 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI212 are used, else settings will be used from LoadProtocol AI212<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 206           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change<br>Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)                  |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.139 ARC\_RM\_AI424 (0210h)

This is the setting for type AI424.

Table 242. ARC\_RM\_AI424 (0210h) EEPROM configuration bit description

| Address (hex) | Function    | Bit  | Description  |
|---------------|-------------|------|--|
| 218           | RM_RX_ARC_4 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 216           | RM_RX_ARC_3 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 214           | RM_RX_ARC_2 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 212           | RM_RX_ARC_1 | 15:0 | Bit[15]<br>0: ARC settings always apply, bits 0...9 from the table ARC_RM_AI424 are used<br>1: ARC settings during FDT, bits 0..9 of table ARC_RM_AI424 are used, else settings will be used from LoadProtocol AI424<br>Bits[14:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| 210           | RM_RX_ARC_0 | 15:0 | Bit[15]<br>0: ARC settings always apply<br>1: ARC settings applicable during FDT and DPC change  |

Table 242. ARC\_RM\_AI424 (0210h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | Bit [14]: 1: ARC Enabled for this Tech and Baudrate. 0: ARC disabled for this Tech and Baudrate<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

**Note:** Bit15 of all RM\_RX\_ARC\_n is recommended to be "0" always.

9.26.140 RF\_DEBOUNCE\_TIMEOUT (02B2h)

Table 243. RF\_DEBOUNCE\_TIMEOUT (address 02B2h) EEPROM configuration bit description

| Address (hex) | Function         | Bit | Description  |
|---------------|------------------|-----|--|
| 2B2           | DEBOUNCE_TIMEOUT | 7:0 | Timeout used after the RF detection during the AUTOCOLL to detect if there is a glitch or continuous RF<br>Value is entered in micro seconds, each bit represents 1 micro second |

9.26.141 SENSE\_RES (02B3h)

Table 244. SENSE\_RES (address 02B3) EEPROM configuration bit description

| Address (hex) | Function               | Bit  | Description                  |
|---------------|------------------------|------|------------------------------|
| 2B3           | AUTOCOLL configuration | 16:0 | ATQA in order byte 0, byte 1 |
|               |                        | 16:8 | Byte1                        |
|               |                        | 7:0  | Byte0                        |

9.26.142 NFC\_ID1 (02B5h)

Table 245. NFC\_ID1 (address 2B5h) EEPROM configuration bit description

| Address (hex) | Function               | Bit   | Description  |
|---------------|------------------------|-------|--|
| 2B5           | AUTOCOLL configuration |       | If Random UID is disabled (EEPROM address 0x2CB), the content of these addresses is used to generate a Fixed UID.<br>The order is byte 0, Byte 1, Byte 2; Byte3 - which is the first NFCID1 byte - is fixed to 08h, the check byte is calculated automatically |
|               |                        | 23:16 | Byte2  |
|               |                        | 15:8  | Byte1:   |
|               |                        | 7:0   | Byte0:   |

### 9.26.143 SEL\_RES (02B8h)

Table 246. SEL\_RES (address 2B8h) EEPROM configuration bit description

| Address (hex) | Function               | Bit | Description             |
|---------------|------------------------|-----|-------------------------|
| 2B8           | AUTOCOLL configuration | 7:0 | Response to Select: SAK |

### 9.26.144 FELICA\_POLL\_RES (02B9h)

The FeliCa response is configured by 18 bytes.

Table 247. FELICA\_POLL\_RES (address 02B9) EEPROM configuration bit description

| Address (hex) | Function               | Bit  | Description  |
|---------------|------------------------|------|--|
| 2B9           | AUTOCOLL configuration | 15:0 | FeliCa polling response: shall be 01h, FEh (2 bytes) |
| 2BB           |                        | 47:0 | FeliCa polling response: NFCID2 (6 bytes)            |
| 2C1           |                        | 63:0 | FeliCa polling response: PAD (8 bytes)               |
| 2C9           |                        | 15:0 | FeliCa polling response: system code (2 bytes)       |

### 9.26.145 RANDOM\_UID\_ENABLE (02CBh)

Table 248. RANDOM\_UID\_ENABLE (address 2CBh) EEPROM configuration bit description

| Address (hex) | Function          | Bit | Description   |
|---------------|-------------------|-----|---|
| 2CB           | RFU               | 7:1 | -   |
|               | Random UID Enable | 0   | 0: Use UID stored in EEPROM<br>1: Randomly generate the UID in which the first byte is fixed and the remaining 3 bytes are random<br>A new random number is generated after each RF-OFF to RF-ON. |

### 9.26.146 MFC\_AUTH\_TIMEOUT (02CCh)

Table 249. MFC\_AUTH\_TIMEOUT (address 2CCh) EEPROM configuration bit description

| Address (hex) | Function | Bit  | Description   |
|---------------|----------|------|---|
| 2CC           | RFU      | 15:0 | Timeout value in micro seconds used for Auth1 and Auth2 stages during MIFARE Classic Authenticate |

### 9.26.147 RSSI\_TIMER (02DAh)

Configuration for Card Emulation mode only.

Table 250. RSSI\_TIMER (address 2DAh) EEPROM configuration bit description

| Address (hex) | Function   | Bit  | Description  |
|---------------|------------|------|--------------|
| 2DA           | RSSI_TIMER | 15:0 | Default: 423 |

## 9.26.148 RSSI\_TIMER\_FIRST\_PERIOD (02DCh)

Table 251. RSSI\_TIMER\_FIRST\_PERIOD (address 2DCh) EEPROM configuration bit description

| Address (hex) | Function | Bit  | Description   |
|---------------|----------|------|---|
| 2DC           | RSSI     | 15:0 | First period duration after Rffield ON. Unit is 128/fc (106 kHz) if set to 0 it means that feature is not used 0D2 => ~2 ms |

## 9.26.149 RSSI\_CTRL\_00\_AB (02DEh)

Table 252. RSSI\_CTRL\_00\_AB (address 2DEh) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
| 2DE           | RSSI     | 7:6 | Bits [6:7] = RFU  |
|               |          | 5:0 | Bits [0:5] = (APC_ID_REF_AB) ID of APC_TX entry that is equiv to RSSI = 0 (for Type AB) |

## 9.26.150 RSSI\_NB\_ENTRIES\_AB (02DFh)

Table 253. RSSI\_NB\_ENTRIES\_AB (address 2DFh) EEPROM configuration bit description

| Address (hex) | Function | Bit | Description  |
|---------------|----------|-----|--|
| 2DF           | RSSI     | 7:5 | RFU  |
|               |          | 4:0 | For Initial RF ON, CEA and CEB<br>Number of entries in RSSI lookup table (it refers to dwRssiEntryAB_01 to dwRssiEntryAB_X); |

## 9.26.151 RSSI\_THRESHOLD\_PHASE\_TABLE (02E0h)

Table 254. RSSI\_THRESHOLD\_PHASE\_TABLE (address 2E0h) EEPROM configuration bit description

| Address (hex) | Function           | Bit  | Description  |
|---------------|--------------------|------|--|
| 2E0           | wRssiThresholdF_01 | 15:0 | bit[0:12] - RSSI Value<br>bit[13:15] - RFU Note: dwRssiEntryAB_00 = 0 (not in EEPROM) Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2) |
| 2E2           | ArbPhaseF_01       | 15:0 | wArbPhaseF_xx: Signed phase compensation with 1/4 degree resolution: 16 bits signed value (using complement of 2)  |
|               | RssiThresholdF_02  | 15:0 |  |
|               | ArbPhaseF_02       | 15:0 |  |
|               | RssiThresholdF_03  | 15:0 |  |
|               | ArbPhaseF_03       | 15:0 |  |
|               | RssiThresholdF_04  | 15:0 |  |
|               | ArbPhaseF_04       | 15:0 |  |
|               | RssiThresholdF_05  | 15:0 |  |
|               | ArbPhaseF_05       | 15:0 |  |



Table 254. RSSI\_THRESHOLD\_PHASE\_TABLE (address 2E0h) EEPROM configuration bit description...continued

| Address (hex) | Function          | Bit  | Description |
|---------------|-------------------|------|-------------|
|               | RssiThresholdF_06 | 15:0 |             |
|               | ArbPhaseF_06      | 15:0 |             |
|               | RssiThresholdF_07 | 15:0 |             |
|               | ArbPhaseF_07      | 15:0 |             |
|               | RssiThresholdF_08 | 15:0 |             |
|               | ArbPhaseF_08      | 15:0 |             |
|               | RssiThresholdF_09 | 15:0 |             |
|               | ArbPhaseF_09      | 15:0 |             |
|               | RssiThresholdF_0A | 15:0 |             |
|               | ArbPhaseF_0A      | 15:0 |             |
|               | RssiThresholdF_0B | 15:0 |             |
|               | ArbPhaseF_0B      | 15:0 |             |
|               | RssiThresholdF_0C | 15:0 |             |
|               | ArbPhaseF_0C      | 15:0 |             |
|               | RssiThresholdF_0D | 15:0 |             |
|               | ArbPhaseF_0D      | 15:0 |             |
|               | RssiThresholdF_0E | 15:0 |             |
|               | ArbPhaseF_0E      | 15:0 |             |
|               | RssiThresholdF_0F | 15:0 |             |
|               | ArbPhaseF_0F      | 15:0 |             |
|               | RssiThresholdF_10 | 15:0 |             |
|               | ArbPhaseF_10      | 15:0 |             |
|               | RssiThresholdF_11 | 15:0 |             |
|               | ArbPhaseF_11      | 15:0 |             |
|               | RssiThresholdF_12 | 15:0 |             |
|               | ArbPhaseF_12      | 15:0 |             |
|               | RssiThresholdF_13 | 15:0 |             |
|               | ArbPhaseF_13      | 15:0 |             |
|               | RssiThresholdF_14 | 15:0 |             |
|               | ArbPhaseF_14      | 15:0 |             |
|               | RssiThresholdF_15 | 15:0 |             |
|               | ArbPhaseF_15      | 15:0 |             |
|               | RssiThresholdF_16 | 15:0 |             |
|               | ArbPhaseF_16      | 15:0 |             |
|               | RssiThresholdF_17 | 15:0 |             |
|               | ArbPhaseF_17      | 15:0 |             |

Table 254. RSSI\_THRESHOLD\_PHASE\_TABLE (address 2E0h) EEPROM configuration bit description...continued

| Address (hex) | Function          | Bit  | Description |
|---------------|-------------------|------|-------------|
|               | RssiThresholdF_18 | 15:0 |             |
|               | ArbPhaseF_18      | 15:0 |             |

9.26.152 TX\_PARAM\_ENTRY\_TABLE (03A2h)

Table 255. TX\_PARAM\_ENTRY\_TABLE (address 3A2h) EEPROM configuration bit description

| Address (hex) | Function             | Bit                  | Description  |
|---------------|----------------------|----------------------|--|
| 3A2           | TxParamEntry_00_ID   | 7                    | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6                    | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0                  | ID   |
|               |                      | bTxParamEntry_00_Tx1 | 7:6  |
|               |                      | 5:0                  | PMU VDDPA setting: $VDDPA(v) = (val * 10) + 1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                           |
|               | bTxParamEntry_00_Tx2 | 7:0                  | Scaling factor for TX1 and TX2   |
| 3A5           | TxParamEntry_01_ID   | 7                    | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6                    | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0                  | ID   |
|               |                      | bTxParamEntry_01_Tx1 | 7:6  |
|               |                      | 5:0                  | PMU VDDPA setting: $VDDPA(v) = (val * 10) + 1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                           |
|               | bTxParamEntry_01_Tx2 | 7:0                  | Scaling factor for TX1 and TX2   |
| 3A8           | TxParamEntry_02_ID   | 7                    | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6                    | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0                  | ID   |
|               |                      | bTxParamEntry_02_Tx1 | 7:6  |
|               |                      | 5:0                  | PMU VDDPA setting: $VDDPA(v) = (val * 10) + 1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                           |
|               | bTxParamEntry_02_Tx2 | 7:0                  | Scaling factor for TX1 and TX2   |
| 3AB           | TxParamEntry_03_ID   | 7                    | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |

Table 255. TX\_PARAM\_ENTRY\_TABLE (address 3A2h) EEPROM configuration bit description...continued

| Address (hex) | Function             | Bit | Description  |
|---------------|----------------------|-----|--|
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_03_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_03_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3AE           | TxParamEntry_04_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_04_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_04_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3B1           | TxParamEntry_05_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_05_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_05_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3B4           | TxParamEntry_06_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_06_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_06_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3B7           | TxParamEntry_07_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |

Table 255. TX\_PARAM\_ENTRY\_TABLE (address 3A2h) EEPROM configuration bit description...continued

| Address (hex) | Function             | Bit | Description  |
|---------------|----------------------|-----|--|
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_07_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_07_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3BA           | TxParamEntry_08_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_08_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_08_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3BD           | TxParamEntry_09_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_09_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_09_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3C1           | TxParamEntry_0A_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled                    |
|               |                      | 5:0 | ID   |
|               | bTxParamEntry_0A_Tx1 | 7:6 | RFU  |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V                               |
|               | bTxParamEntry_0A_Tx2 | 7:0 | Scaling factor for TX1 and TX2   |
| 3C3           | TxParamEntry_0B_ID   | 7   | bit[7] Driver count (CLIF_TX_CONTROL_REG.TX_ALM_TYPE_SELECT):<br>0 - Dual driver,<br>1 - Single driver |

Table 255. TX\_PARAM\_ENTRY\_TABLE (address 3A2h) EEPROM configuration bit description...continued

| Address (hex) | Function             | Bit | Description   |
|---------------|----------------------|-----|---|
|               |                      | 6   | BPSK mode (CLIF_TX_CONTROL_REG.TX_ALM_BPSK_ENABLE):<br>0 - Disabled,<br>1 - Enabled |
|               |                      | 5:0 | ID  |
|               | bTxParamEntry_0B_Tx1 | 7:6 | RFU   |
|               |                      | 5:0 | PMU VDDPA setting: $VDDPA(v) = (val*10)+1,5$ 0 = 1.50 V ... 2Ah = 5.70 V            |
|               | bTxParamEntry_0B_Tx2 | 7:0 | Scaling factor for TX1 and TX2  |

### 9.26.153 LPCD\_AVG\_SAMPLES (0492h)

Configuration for the Switch mode LPCD

Table 256. LPCD\_AVG\_SAMPLES (address 0492h) EEPROM configuration bit description

| Address (hex) | Function     | Bit | Description   |
|---------------|--------------|-----|---|
| 492           | LPCD setting | 7:0 | Defining how many samples of the I and Q values are used for the averaging.<br>Average of samples in power of 2<br>0->1 sample<br>1->2 samples<br>2->4 samples<br>3->8 samples<br>4->16 samples<br>5-> 32 samples<br>6-> 64 samples |

### 9.26.154 LPCD\_RSSI\_TARGET (0494h)

Table 257. LPCD\_RSSI\_TARGET (address 0494h) EEPROM configuration bit description

| Address (hex) | Function     | Bit   | Description   |
|---------------|--------------|-------|---|
| 494           | RFU          | 15:10 |   |
|               | LPCD setting | 9:0   | This value is used for the LPCD as DGRM_RSSI_TARGET.<br>Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used. |

### 9.26.155 LPCD\_RSSI\_HYST (0496h)

Table 258. LPCD\_RSSI\_HYST (address 0496h) EEPROM configuration bit description

| Address (hex) | Function     | Bit | Description   |
|---------------|--------------|-----|---|
| 496           | LPCD setting | 7:0 | This value is used for the LPCD as DGRM_RSSI_HYST<br>Typically the same values as for Type A106 LOAD_RF_CONFIGURATION(0x0D) (DGRM_RSSI register) are used |

## 9.26.156 LPCD\_CONFIG (0497h)

Table 259. LPCD\_CONFIG (address 0497h) EEPROM configuration register bit description

| Address (hex) | Function              | Bit  | Description   |
|---------------|-----------------------|------|---|
| 497           | RFU                   | 15:6 | -   |
|               |                       | 5    | Immediate RF OFF before TXLDO shutdown to save power 0 - Disable 1 - Enable |
|               |                       | 4    | VDDPA fast discharge 0 - Disable 1 - Enable                                 |
|               |                       | 3    | TX Drivers 0 - Enable Single driver 1 - Enable both drivers                 |
|               | Acquisition channels: | 2:0  | 0:1 = RFU<br>2 = Magnitude<br>3 = I and Q<br>4 =M, I and Q<br>5:7 = RFU     |

## 9.26.157 LPCD\_THRESHOLD\_COARSE (049Ah)

Table 260. LPCD\_THRESHOLD\_COARSE (address 049Ah) EEPROM configuration bit description

| Address (hex) | Function                 | Bit   | Description   |
|---------------|--------------------------|-------|---|
| 49A           | LPCD Q channel threshold | 31:16 | ADC LSB granularity of threshold depends on avg_samples_meas value<br>5: unit 1/32;<br>4: unit 1/16;<br>3: unit 1/8;<br>2: unit 1/4;<br>1: unit 1/2;<br>0: unit 1 |
|               | LPCD I channel threshold | 0:15  | ADC LSB granularity of threshold depends on avg_samples_meas value<br>5: unit 1/32;<br>4: unit 1/16;<br>3: unit 1/8;<br>2: unit 1/4;<br>1: unit 1/2;<br>0: unit 1 |

**Note:** If the difference between the measured value and the reference is greater than the threshold on either channels, then a card is detected.

## 9.26.158 WAIT\_RX\_SETTLE (04ABh)

Table 261. WAIT\_RX\_SETTLE (address 04ABh) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description   |
|---------------|------------|-----|---|
| 4AB           | LPCD Delay | 7:0 | Delay between Field-On and starting ADC data averaging for the LPCD.<br>Value in us, default 14h = 20us |

9.26.159 LPCD\_VDDPA (04AFh)

Table 262. LPCD\_VDDPA (address 04AFh) EEPROM configuration bit description

| Address (hex) | Function   | Bit | Description   |
|---------------|--|-----|---|
| 4AF           | VDDPA voltage during LPCD when DC-DC (internal or external) or external power source is used to feed TXLDO | 7:0 | TXLDO output voltage:<br>0x00: 1V50<br>0x01: 1V60<br>0x02: 1V70<br>0x03: 1V80<br>0x04: 1V90<br>0x05: 2V00<br>0x06: 2V10<br>0x07: 2V20<br>0x08: 2V30<br>0x09: 2V40<br>0x0A: 2V50<br>0x0B: 2V60<br>0x0C: 2V70<br>0x0D: 2V80<br>0x0E: 2V90<br>0x0F: 3V00<br>0x10: 3V10<br>0x11: 3V20<br>0x12: 3V30<br>0x13: 3V40<br>0x14: 3V50<br>0x15: 3V60<br>0x16: 3V70<br>0x17: 3V80<br>0x18: 3V90<br>0x19: 4V00<br>0x1A: 4V10<br>0x1B: 4V20<br>0x1C: 4V30<br>0x1D: 4V40<br>0x1E: 4V50<br>0x1F: 4V60<br>0x20: 4V70<br>0x21: 4V80<br>0x22: 4V90<br>0x23: 5V00<br>0x24: 5V10<br>0x25: 5V20<br>0x26: 5V30<br>0x27: 5V40<br>0x28: 5V50<br>0x29: 5V60<br>0x2A: 5V70 |

9.26.160 ULPCD\_VDDPA\_CTRL (04BFh)

Table 263. ULPCD\_VDDPA\_CTRL (address 4BFh) EEPROM configuration bit description

| Address (hex) | Function           | Bit  | Description  |
|---------------|--------------------|------|--|
|               | RFU                | 15:9 | -  |
|               | LDO_VDDPA_VOUT_SEL | 8:3  | TXLDO output voltage during ULPCD polling<br>VDDPA_1V50 /* 0x00 */<br>VDDPA_1V60 /* 0x01 */<br>VDDPA_1V70 /* 0x02 */<br>VDDPA_1V80 /* 0x03 */<br>VDDPA_1V90 /* 0x04 */<br>VDDPA_2V00 /* 0x05 */<br>VDDPA_2V10 /* 0x06 */<br>VDDPA_2V20 /* 0x07 */<br>VDDPA_2V30 /* 0x08 */<br>VDDPA_2V40 /* 0x09 */<br>VDDPA_2V50 /* 0x0A */<br>VDDPA_2V60 /* 0x0B */<br>VDDPA_2V70 /* 0x0C */<br>VDDPA_2V80 /* 0x0D */<br>VDDPA_2V90 /* 0x0E */<br>VDDPA_3V00 /* 0x0F */<br>VDDPA_3V10 /* 0x10 */<br>VDDPA_3V20 /* 0x11 */<br>VDDPA_3V30 /* 0x12 */<br>VDDPA_3V40 /* 0x13 */<br>VDDPA_3V50 /* 0x14 */<br>VDDPA_3V60 /* 0x15 */<br>VDDPA_3V70 /* 0x16 */<br>VDDPA_3V80 /* 0x17 */<br>VDDPA_3V90 /* 0x18 */<br>VDDPA_4V00 /* 0x19 */<br>VDDPA_4V10 /* 0x1A */<br>VDDPA_4V20 /* 0x1B */<br>VDDPA_4V30 /* 0x1C */<br>VDDPA_4V40 /* 0x1D */<br>VDDPA_4V50 /* 0x1E */<br>VDDPA_4V60 /* 0x1F */<br>VDDPA_4V70 /* 0x20 */<br>VDDPA_4V80 /* 0x21 */<br>VDDPA_4V90 /* 0x22 */<br>VDDPA_5V00 /* 0x23 */<br>VDDPA_5V10 /* 0x24 */<br>VDDPA_5V20 /* 0x25 */<br>VDDPA_5V30 /* 0x26 */<br>VDDPA_5V40 /* 0x27 */<br>VDDPA_5V50 /* 0x28 */<br>VDDPA_5V60 /* 0x29 */<br>VDDPA_5V70 /* 0x2A */ |



Table 263. ULPCD\_VDDPA\_CTRL (address 4BFh) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description |
|---------------|----------|-----|-------------|
| 4BF           | RFU      | 2:0 | -           |

### 9.26.161 ULPCD\_TIMING\_CTRL (04C2h)

Table 264. ULPCD\_TIMING\_CTRL (address 4C2h) EEPROM configuration bit description

| Address (hex) | Function        | Bit | Description  |
|---------------|-----------------|-----|--|
| 4C2           | RFON_GUARD_TIME | 7:4 | RFON guard time: $(\text{RFON\_GUARD\_TIME} + 2) * \text{LFO-Freq}$ (380 kHz)<br>Guard time: Time between RF-ON and first sampling of data |
|               | RFU             | 3:0 | -  |

### 9.26.162 ULPCD\_VOLTAGE\_CTRL (04C6h)

Table 265. ULPCD\_VOLTAGE\_CTRL (address 4C6h) EEPROM configuration bit description

| Address (hex) | Function            | Bit | Description   |
|---------------|---------------------|-----|---|
| 4C6           | ULPCD configuration | 7:5 | RFU   |
|               |                     | 4:2 | RFU   |
|               |                     | 1   | TX_SUPPLY by VUP_TX<br>0: VUP externally supplied (2.8 V to 6.0 V)<br>1: VUP supplied by PN5190B1 itself (pin VUP_TX connected to VBAT/VBATPWR) |
|               |                     | 0   | RFU   |

### 9.26.163 ULPCD\_RSSI\_GUARD\_TIME (04C9h)

Table 266. ULPCD\_RSSI\_GUARD\_TIME (address 4C9h) EEPROM configuration bit description

| Address (hex) | Function                       | Bit  | Description   |
|---------------|--------------------------------|------|---|
| 4C9           | ULPCD RSSI sampling guard time | 15   | RFU   |
|               |                                | 14:0 | This is the time between consecutive RSSI samples:<br>Range: 0 - 127 in micro seconds |

### 9.26.164 ULPCD\_RSSI\_SAMPLE\_CFG (04CAh)

Table 267. ULPCD\_RSSI\_SAMPLE\_CFG (address 4CAh) EEPROM configuration bit description

| Address (hex) | Function            | Bit | Description  |
|---------------|---------------------|-----|--|
| 4CA           | ULPCD configuration | 7:0 | Number of RSSI Samples which are internally averaged:<br>0: 4 samples,<br>1: 8 samples<br>2: 16 samples<br>3: 32 samples |

## 9.26.165 ULPCD\_THRESH\_LVL(04CBh)

Table 268. ULPCD\_THRESH\_LVL (address 4CBh) EEPROM configuration bit description

| Address (hex) | Function            | Bit | Description  |
|---------------|---------------------|-----|--|
| 4CB           | ULPCD configuration | 8:0 | RSSI Threshold level Range 0 - 31<br>If the difference between the measured RSSI value and the reference (which is derived during calibration) is greater than the threshold, then a card is detected. |

## 9.26.166 ULPCD\_GPIO3 (04CCh)

Table 269. ULPCD\_GPIO3 (address 4CCh) EEPROM configuration bit description

| Address (hex) | Function                  | Bit | Description  |
|---------------|---------------------------|-----|--|
| 4CC           | RFU                       | 7:1 | -  |
| 4CC           | ULPCD GPIO3 configuration | 0   | GPIO3 abort polarity configuration. If PN5190B1 is using the ULPCD, GPIO3 cannot be used for any other purpose than aborting the ULPCD.<br>1: high-level aborts ULPCD<br>0: low-level aborts ULPCD |

## 9.26.167 TXIRQ\_GuardTime (0559h)

Table 270. TXIRQ\_GuardTime (address 0559) EEPROM configuration bit description

| Address (hex) | Function         | Bit  | Description   |
|---------------|------------------|------|---|
| 559           | TXIRQ_Guard Time | 31:0 | 0 - Disabled<br>0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s |

## 9.26.168 FDT\_default\_val (055Dh)

Table 271. FDT\_default\_val (address 055D) EEPROM configuration bit description

| Address (hex) | Function        | Bit  | Description   |
|---------------|-----------------|------|---|
| 55D           | FDT_default_val | 31:0 | 0x00 - Disabled<br>others - enabled (1 unit is 18.86us) Default fixed to 5.5 secs |

## 9.26.169 RXIRQ\_GuardTime (0561h)

Table 272. RXIRQ\_GuardTime (address 0561h) EEPROM configuration bit description

| Address (hex) | Function         | Bit  | Description   |
|---------------|------------------|------|---|
| 561           | RXIRQ_Guard Time | 31:0 | 0x00 Disabled<br>0x1-0xFFFFF (Enabled - 1 unit corresponds to 1 us) Maximum timeout of 1.048 s<br>Default value = 0xF4240 (1 s) |

## 9.26.170 NFCLD\_RFLD\_Valid (006D3h)

Table 273. NFCLD\_RFLD\_Valid (address 006D3h) EEPROM configuration register bit description

| Address (hex) | Function       | Bit | Description  |
|---------------|----------------|-----|--|
| 6D3           | RFU            | 7:1 | -  |
|               | RFLD_CALIBRATE | 0   | This bit allows to calibrate the RFLD / NFCLD.<br>This calibration is required only once in the lifetime of the chip for increased RFLD / NFCLD accuracy, independent from the value of this bit (0 or 1).<br>Clearing this bit (0) will calibrate the RFLD /RFLD during the next boot-up, precondition for the proper calibration is an unloaded condition and no external field applied.<br>After calibration this bit is set (1) and indicates that the RFLD /RFLD Threshold is a valid data. |

## 9.26.171 CORRECTION\_ENTRY\_TABLE (0BADh)

Table 274. CORRECTION\_ENTRY\_TABLE (address 0BADh) EEPROM configuration bit description

| Address (hex) | Function            | Bit  | Description   |
|---------------|---------------------|------|---|
| 0BAD          | sCorrection_Entry0  | 15:0 | The correction that is applied when lookup table based shaping with scaling is enabled.<br>Range is -128 to +127,<br>sCorrection_Entry0 corresponds to correction applied at VDDPA = 1V5,<br>Correction_Entry42 corresponds to correction applied at VDDPA = 5V7<br>For each entry:<br>BYTE 0: Bits[7:0] = define the correction which is applied for ASK100<br>BYTE 1: Bits[15:8] = define the correction which is applied for ASK10 |
| BAF           | sCorrection_Entry1  | 15:0 |   |
| BB1           | sCorrection_Entry2  | 15:0 |   |
| BB3           | sCorrection_Entry3  | 15:0 |   |
| BB5           | sCorrection_Entry4  | 15:0 |   |
| BB7           | sCorrection_Entry5  | 15:0 |   |
| BB9           | sCorrection_Entry6  | 15:0 |   |
| BBB           | sCorrection_Entry7  | 15:0 |   |
| BBD           | sCorrection_Entry8  | 15:0 |   |
| BBF           | sCorrection_Entry9  | 15:0 |   |
| BC1           | sCorrection_Entry10 | 15:0 |   |
| BC3           | sCorrection_Entry11 | 15:0 |   |
| BC5           | sCorrection_Entry12 | 15:0 |   |
| BC7           | sCorrection_Entry13 | 15:0 |   |
| BC9           | sCorrection_Entry14 | 15:0 |   |
| BCB           | sCorrection_Entry15 | 15:0 |   |

Table 274. CORRECTION\_ENTRY\_TABLE (address 0BADh) EEPROM configuration bit description...continued

| Address (hex) | Function            | Bit  | Description |
|---------------|---------------------|------|-------------|
| BCD           | sCorrection_Entry16 | 15:0 |             |
| BCF           | sCorrection_Entry17 | 15:0 |             |
| BD1           | sCorrection_Entry18 | 15:0 |             |
| BD3           | sCorrection_Entry19 | 15:0 |             |
| BD5           | sCorrection_Entry20 | 15:0 |             |
| BD7           | sCorrection_Entry21 | 15:0 |             |
| BD9           | sCorrection_Entry22 | 15:0 |             |
| BDB           | sCorrection_Entry23 | 15:0 |             |
| BDD           | sCorrection_Entry24 | 15:0 |             |
| BDF           | sCorrection_Entry25 | 15:0 |             |
| BE1           | sCorrection_Entry26 | 15:0 |             |
| BE3           | sCorrection_Entry27 | 15:0 |             |
| BE5           | sCorrection_Entry28 | 15:0 |             |
| BE7           | sCorrection_Entry29 | 15:0 |             |
| BE9           | sCorrection_Entry30 | 15:0 |             |
| BEB           | sCorrection_Entry31 | 15:0 |             |
| BED           | sCorrection_Entry32 | 15:0 |             |
| BEF           | sCorrection_Entry33 | 15:0 |             |
| BF1           | sCorrection_Entry34 | 15:0 |             |
| BF3           | sCorrection_Entry35 | 15:0 |             |
| BF5           | sCorrection_Entry36 | 15:0 |             |
| BF7           | sCorrection_Entry37 | 15:0 |             |
| BF9           | sCorrection_Entry38 | 15:0 |             |
| BFB           | sCorrection_Entry39 | 15:0 |             |
| BFD           | sCorrection_Entry40 | 15:0 |             |
| BFF           | sCorrection_Entry41 | 15:0 |             |
| C01           | sCorrection_Entry42 | 15:0 |             |

### 9.26.172 RTRANS\_FTRANS\_TABLE (0C03h)

Table 275. RTRANS\_FTRANS\_TABLE (address C03h) EEPROM configuration bit description

| Address (hex) | Function | Bit  | Description   |
|---------------|----------|------|---|
| C03           | RTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| C07           | RTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| C0B           | RTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |
| C0F           | RTRANS3  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the rising edge |

Table 275. RTRANS\_FTRANS\_TABLE (address C03h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit  | Description  |
|---------------|----------|------|--|
| C13           | FTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| C17           | FTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| C1B           | FTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| C1F           | FTRANS3  | 31:0 | These values apply in case EDGE_STYLE = 0 is configured for the falling edge |
| C23           | RTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the rising edge  |
| C27           | RTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the rising edge  |
| C2B           | RTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the rising edge  |
| C2F           | RTRANS03 | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the rising edge  |
| C33           | FTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the falling edge |
| C37           | FTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the falling edge |
| C3B           | FTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the falling edge |
| C3F           | FTRANS3  | 31:0 | These values apply in case EDGE_STYLE = 1 is configured for the falling edge |
| C43           | RTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the rising edge  |
| C47           | RTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the rising edge  |
| C4B           | RTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the rising edge  |
| C4F           | RTRANS03 | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the rising edge  |
| C53           | FTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the falling edge |
| C57           | FTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the falling edge |
| C5B           | FTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the falling edge |
| C5F           | FTRANS3  | 31:0 | These values apply in case EDGE_STYLE = 2 is configured for the falling edge |
| C63           | RTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the rising edge  |
| C67           | RTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the rising edge  |
| C6B           | RTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the rising edge  |
| C6F           | RTRANS03 | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the rising edge  |
| C73           | FTRANS0  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the falling edge |
| C77           | FTRANS1  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the falling edge |
| C7B           | FTRANS2  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the falling edge |
| C7F           | FTRANS3  | 31:0 | These values apply in case EDGE_STYLE = 3 is configured for the falling edge |

This table applies only, if the transmitter shaping configuration is (EDGE\_TYPE\_xx) 4, 5, or 6.

Which of the entries RTRANS0..3 (rising transition) / FTRANS0..3 (falling transition) is applied, is defined by the EDGE\_STYLE.

### 9.26.173 CFG\_NOV\_CAL (0C83h)

TX non-overlap feature - defines the non-overlap time of TX1, TX2.

Table 276. CFG\_NOV\_CAL (address 0083h) EEPROM configuration bit description

| Address (hex) | Function         | Bit | Description  |
|---------------|------------------|-----|--|
| 1             | RFU              | 7:2 | -  |
|               | CALIBRATION_TYPE | 1:0 | 00 = No calibration performed, needs to be updated to 01 or 10 before the first RF on of the chip is performed<br>01 = Enable FW calibration after every cold boot<br>10 = Use calibration value coming from EEPROM NOV_CAL_VAL1, NOV_CAL_VAL2<br><b>(Default)</b><br>11 = RFU |

9.26.174 NOV\_CAL\_VAL1 (0C84h)

Table 277. NOV\_CAL\_VAL1 (address 0C84h) EEPROM configuration bit description

| Address (hex) | Function     | Bit | Description  |
|---------------|--------------|-----|--|
| 1             | VddpaCalVal1 | 7:0 | It defines the VDDPA value that FW uses to perform NOV calibration group #1.<br>value = 03h (1.8 V)<br>value = 0Dh (2.8 V)<br>See "TxLdoVddpaHigh" parameter for list of voltage |

9.26.175 NOV\_CAL\_VAL2 (0C85h)

Table 278. NOV\_CAL\_VAL2 (0C85h) EEPROM configuration bit description

| Address (hex) | Function     | Bit | Description  |
|---------------|--------------|-----|--|
| 1             | VddpaCalVal2 | 7:0 | It defines the VDDPA value that FW uses to perform NOV calibration group #2.<br>default value = 15h (3.6 V)<br>default value = 24h (5.1 V)<br>See "TxLdoVddpaHigh" parameter for list of voltage |

9.26.176 NOV\_CAL\_THRESHOLD (0C86h)

Table 279. NOV\_CAL\_THRESHOLD (address 0C86h) EEPROM configuration bit description

| Address (hex) | Function     | Bit | Description   |
|---------------|--------------|-----|---|
| 1             | CfgThreshold | 7:0 | It defines VDDPA threshold that FW will use to select Group #1 or Group #2 NOV offset values.<br>default value = 08h (2.3 V)<br>default value = 16h (3.7 V)<br>See "TxLdoVddpaHigh" parameter for list of voltage |

9.26.177 NOV\_CAL\_OFFSET1 (0C87h)

Table 280. NOV\_CAL\_OFFSET1 (address 0C87h) EEPROM configuration bit description

| Address (hex) | Function     | Bit   | Description  |
|---------------|--------------|-------|--|
| C87           | RFU          | 31:29 |  |
|               | UserOffsets1 | 28:0  | It defines user static offsets applied if CFG_NOV_CAL[1:0] = 10b |

Table 280. NOV\_CAL\_OFFSET1 (address 0C87h) EEPROM configuration bit description...continued

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | bits[04:00] Group #1 (CfgThreshold to VDDPA max), offset_3l<br>bits[12:08] Group #1 (CfgThreshold to VDDPA max), offset_3l_p2<br>bits[20:16] Group #1 (CfgThreshold to VDDPA max), offset_2l<0><br>bits[28:24] Group #1 (CfgThreshold to VDDPA max), offset_2l<1> |

9.26.178 NOV\_CAL\_OFFSET2 (0C8Bh)

Table 281. NOV\_CAL\_OFFSET1 (address 0C8Bh) EEPROM configuration bit description

| Address (hex) | Function     | Bit   | Description  |
|---------------|--------------|-------|--|
| C8B           | RFU          | 31:29 |  |
|               | UserOffsets2 | 28:0  | It defines user static offsets applied if CFG_NOV_CAL1:0] = 10b<br>bits[04:00] Group #2 (CfgThreshold to VDDPA max), offset_3l<br>bits[12:08] Group #2 (CfgThreshold to VDDPA max), offset_3l_p2<br>bits[20:16] Group #2 (CfgThreshold to VDDPA max), offset_2l<0><br>bits[28:24] Group #2 (CfgThreshold to VDDPA max), offset_2l<1> |

9.26.179 VDDPA\_DISCHARGE (0C8Fh)

Table 282. VDDPA\_DISCHARGE (address 0C8Fh) EEPROM configuration bit description

| Address (hex) | Function                 | Bit | Description   |
|---------------|--------------------------|-----|---|
| C8F           | RFU                      | 7:1 | RFU   |
|               | EnableFastVDDPADischarge | 0   | 1 - Enables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF (default)<br>0 - Disables fast discharge of VDDPA by setting VDDPA=5.7 and then to 1.5 V, during RF OFF |

9.26.180 ARC\_RM\_A106\_FDT (0C9Dh)

This is the setting for type A-106.

Table 283. ARC\_RM\_A106\_FDT (address 0C9Dh) EEPROM configuration bit description

| Address (hex) | Function        | Bit  | Description  |
|---------------|-----------------|------|--|
| CA5           | RM_RX_ARC_FDT_4 | 15:0 | Bit[15]: RFU<br>Bit [14]: Has to be always "0"<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| CA3           | RM_RX_ARC_FDT_3 | 15:0 | Bit[15]: RFU<br>Bit [14]: Has to be always "0"   |

Table 283. ARC\_RM\_A106\_FDT (address 0C9Dh) EEPROM configuration bit description...continued

| Address (hex) | Function        | Bit  | Description  |
|---------------|-----------------|------|--|
|               |                 |      | Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled)   |
| CA1           | RM_RX_ARC_FDT_2 | 15:0 | Bit[15]: RFU<br>Bit [14]: Has to be always "0"<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| C9F           | RM_RX_ARC_FDT_1 | 15:0 | Bit[15]: RFU<br>Bit [14]: Has to be always "0"<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |
| C9D           | RM_RX_ARC_FDT_0 | 15:0 | Bit[15]: RFU<br>Bit [14]: Has to be always "0"<br>Bits[13:10] = RFU<br>Bit [9] = Enable the IIR filter.<br>Bits[8:7] = MF_GAIN (this value will be applied to the SIGPR_RM_TECH register, applies as soon as the ARC is enabled)<br>Bits[6:0] = DPC_SIGNAL_DETECT_TH_OVR_VAL (this value will be applied to the DGRM_RSSI register, applies as soon as the ARC is enabled) |

**Note:** For ISO14443-A: In case ARC is disabled, it requires DPC\_SIGNAL\_DETECT\_TH\_OVR\_VAL larger than 0x50 (with MF\_GAIN = 2 (default))

**Note:** For ISO14443-A: In case Bit[15] is configured to 0, it requires DPC\_SIGNAL\_DETECT\_TH\_OVR\_VAL larger than 0x50 (with MF\_GAIN = 2 (default)) if the ARC is enabled.

**Note:** The IIR settings define an all pass filter with approximately -10 dB gain. This can be used to limit the LMA sensitivity of the RX.

9.26.181 Tx\_Symbol23\_Mod\_Reg\_BR\_53 (0CC5h)

Table 284. Tx\_Symbol23\_Mod\_Reg\_BR\_53 (0CC5Eh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description  |
|---------------|--------------|------|--|
| CC5           | 15693_BR_CFG | 31:0 | CLIF_TX_SYMBOL23_MOD_REG value loaded for 15693 BR 53 kbit/s |



### 9.26.182 Tx\_Data\_Mod\_Reg\_BR\_53 (0CC9h)

Table 285. Tx\_Data\_Mod\_Reg\_BR\_53 (0CC9Eh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description  |
|---------------|--------------|------|--|
| CC9           | 15693_BR_CFG | 31:0 | CLIF_TX_Data_MOD_REG value loaded for 15693 BR 53 kbit/s |

### 9.26.183 Tx\_Symbol23\_Mod\_Reg\_BR\_106 (0CCDh)

Table 286. Tx\_Symbol23\_Mod\_Reg\_BR\_106 (0CCDEh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description   |
|---------------|--------------|------|---|
| CCD           | 15693_BR_CFG | 31:0 | CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 106 kbit/s |

### 9.26.184 Tx\_Data\_Mod\_Reg\_BR\_106 (0CD1h)

Table 287. Tx\_Data\_Mod\_Reg\_BR\_106 (0CD1Eh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description   |
|---------------|--------------|------|---|
| CD1           | 15693_BR_CFG | 31:0 | CLIF_TX_Data_MOD_REG value loaded for 15693 BR 106 kbit/s |

### 9.26.185 Tx\_Symbol23\_Mod\_Reg\_BR\_212 (0CD5h)

Table 288. Tx\_Symbol23\_Mod\_Reg\_BR\_212 (0CD5Eh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description   |
|---------------|--------------|------|---|
| CD5           | 15693_BR_CFG | 31:0 | CLIF_TX_Symbol23_MOD_REG value loaded for 15693 BR 212 kbit/s |

### 9.26.186 Tx\_Data\_Mod\_Reg\_BR\_212 (0CD9h)

Table 289. Tx\_Data\_Mod\_Reg\_BR\_212 (0CD9Eh) EEPROM configuration bit description

| Address (hex) | Function     | Bit  | Description   |
|---------------|--------------|------|---|
| CD9           | 15693_BR_CFG | 31:0 | CLIF_TX_Data_MOD_REG value loaded for 15693 BR 212 kbit/s |

### 9.26.187 CardModeUltraLowPowerEnabled (0CDFh)

Table 290. CardModeUltraLowPowerEnabled (address 00DFh) EEPROM configuration bit description

| Address (hex) | Function         | Bit | Description                                  |
|---------------|------------------|-----|--|
| CDF           | RFU              | 7:1 | -  |
|               | CALIBRATION_TYPE | 0   | Enable Ultra Low-Power standby for CardMode. |

**Note:** Note: When bit 0 = 1, Switch Standby instruction with ULP mode cannot be used

## 9.26.188 LPCD\_EXT\_DCDC\_ENABLE (0CE0h)

Table 291. LPCD\_EXT\_DCDC\_ENABLE (0CE0h) EEPROM configuration register bit description

| Address (hex) | Function  | Bit | Description   |
|---------------|---|-----|---|
| CE0           | up to FW 2.02:<br>RFU   | 7:0 | -   |
|               | from FW 2.03.<br>onwards:<br>RFU                                | 7:1 | -   |
|               | from FW 2.03.<br>onwards:<br>GPIO1<br>configuration for<br>LPCD | 0   | Enables the use of GPIO to wake up EXT DC-DC from power saving during LPCD. This function is not available for the ULPCD. |

## 9.26.189 LPCD\_EXT\_DCDC\_DELAY\_TO\_ON (0CE1h)

Table 292. LPCD\_EXT\_DCDC\_DELAY\_TO\_ON (0CE1h) EEPROM configuration register bit description

| Address (hex) | Function  | Bit | Description   |
|---------------|---|-----|---|
| CE1           | up to FW 2.02:<br>RFU   | 7:0 | -   |
|               | from FW 2.03.<br>onwards:<br>GPIO1<br>configuration for<br>LPCD | 7:0 | The value defines the time between setting GPIO1 until Field is switched on. Time in us * 8 to wait for the Ext DC-DC to be started |

## 9.26.190 LPCD\_EXT\_DCDC\_DELAY\_TO\_OFF (0CE2h)

Table 293. LPCD\_EXT\_DCDC\_DELAY\_TO\_OFF (0CE2h) EEPROM configuration register bit description

| Address (hex) | Function  | Bit | Description  |
|---------------|---|-----|--|
| CE2           | until FW2.02:<br>RFU  | 7:0 | -  |
|               | from FW 2.03.<br>onwards:<br>GPIO1<br>configuration for<br>LPCD | 7:0 | Value defines the time between Field Off and clear GPIO1. Time in us * 8 to wait for the Ext DC-DC to be shut down |

## 9.26.191 RxGuardTO\_Multiple (0CE8h)

Table 294. RxGuardTO\_Multiple (address 00CE8h) EEPROM configuration bit description

| Address (hex) | Function           | Bit | Description   |
|---------------|--------------------|-----|---|
| 0CE8          | RxGuardTO_Multiple | 7:0 | This field configures the RxGuard Timeout configuration in multiple of Timeout configured using RXIRQ_GuardTime EEPROM Field (Address 0561h). |

**Table 294. RxGuardTO\_Multiple (address 00CE8h) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
|               |          |     | Default value is 1.<br>Indicating RX_TIMEOUT shall be triggered due to expiry of RXIRQ_GUARD first time only. |

**9.26.192 DigitalTBSignalIndex (0CE9h)**

Available from FW 2.05 onwards:

Test bus number to be configured. Selected from the list of exposed test busses described in Instruction layer document.

**Table 295. DigitalTBSignalIndex (address 0CE9h) EEPROM configuration bit description**

| Address (hex) | Function        | Bit | Description   |
|---------------|-----------------|-----|---|
| CE9           | TB signal index | 7:0 | Digital signal test bus number from table "CTS and test bus signals" in instruction layer document<br>Valid data as described in table, all others: RFU |

**9.26.193 DigitalTBSignalBit (0CEAh)**

Available from FW 2.05 onwards:

Test bus bit number to be configured. Selected from the list of exposed test busses described in Instruction layer document.

**Table 296. DigitalTBSignalBit (address 0CEAh) EEPROM configuration bit description**

| Address (hex) | Function      | Bit | Description   |
|---------------|---------------|-----|---|
| CEA           | TB signal bit | 7:0 | Digital signal test bus bit number from table "CTS and test bus signals" in instruction layer document<br>Valid data as described in table, all others: RFU |

**9.26.194 AnalogTBSignalIndex (0CEBh)**

Available from FW 2.05 onwards:

Analog test bus to be configured. Selected from the list of exposed test busses described in Instruction layer document.

**Table 297. AnalogTBSignalIndex (address 0CEBh) EEPROM configuration bit description**

| Address (hex) | Function | Bit | Description   |
|---------------|----------|-----|---|
| CEB           |          | 7:0 | Analog signal test bus number:<br>0x78 - obs_clif_tbcontrol_patchbox0<br>0x79 - obs_clif_tbcontrol_patchbox1<br>0x7A - obs_clif_tbcontrol_patchbox2<br>0x7B - obs_clif_tbcontrol_patchbox3<br>all others: RFU |

## 9.26.195 ENABLE\_ULFO\_TRIM\_CALIBRATION (0CECh)

Table 298. SEL\_RES (address 2B8h) EEPROM configuration bit description

| Address (hex) | Function                     | Bit | Description   |
|---------------|------------------------------|-----|---|
| CEC           | ENABLE_ULFO_TRIM_CALIBRATION | 7:1 | RFU   |
|               |                              | 0   | <p>until FW 2.06: RFU<br/>           from FW 2.07 onwards:<br/>           1: Enable<br/>           0: Disable</p> <p>The internal calibration of the wake-up counter value is done based on the ULFO accuracy measured with Xtal as reference clock and the entered wake-up time.<br/>           The calibration is done each time when the ULPCD mode is entered and the bit 1 is set.<br/>           Note: This feature shall be used only when Xtal is available on the board, otherwise an accurate reference clock for the ULFO accuracy measurement is not available. No other user input is required to achieve a higher accuracy of the ULFO.</p> |

## 9.26.196 USER\_DATA (0D2Dh)

Table 299. USER\_DATA (0D2Dh) EEPROM configuration bit description

available only from FW 2.5 onwards

| Address (hex) | Function         | Bit | Description   |
|---------------|------------------|-----|---|
| 0D2D          | USER_DATA Byte1  | 7:0 | Custom defined R/W user data. Content does not have any impact on the functionality of the device.  |
|               | USER_DATA Byte2  | 7:0 | <p>Note that frequent (e.g. automatic triggered) R/W cycles to this DWORD have an impact on the lifetime of the EEPROM as described in the chapter "EEPROM characteristics".<br/>           ATTENTION: Any user data will be erased during a Firmware update.</p> |
|               | USER_DATA Byte3  | 7:0 |   |
|               | USER_DATA Byte4  | 7:0 |   |
|               | USER_DATA Byte5  | 7:0 |   |
|               | USER_DATA Byte6  | 7:0 |   |
|               | USER_DATA Byte7  | 7:0 |   |
|               | USER_DATA Byte8  | 7:0 |   |
|               | USER_DATA Byte9  | 7:0 |   |
|               | USER_DATA Byte10 | 7:0 |   |
|               | USER_DATA Byte11 | 7:0 |   |

**Table 299. USER\_DATA (0D2Dh) EEPROM configuration bit description...continued**  
available only from FW 2.5 onwards

| Address (hex) | Function            | Bit | Description |
|---------------|---------------------|-----|-------------|
|               | USER_DATA<br>Byte12 | 7:0 |             |
|               | USER_DATA<br>Byte13 | 7:0 |             |
|               | USER_DATA<br>Byte14 | 7:0 |             |
|               | USER_DATA<br>Byte15 | 7:0 |             |
|               | USER_DATA<br>Byte16 | 7:0 |             |

## 10 Limiting values

**Table 300. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol            | Parameter                       | Conditions  | Min   | Max   | Unit |
|-------------------|---------------------------------|---|-------|-------|------|
| $V_{DD(VUP\_TX)}$ | supply voltage on pin VUP_TX    | -   | -0.3  | 6.3   | V    |
| $V_{DD(VBAT)}$    | supply voltage on pin VBAT      | -   | -0.3  | 5.8   | V    |
| $V_{DD(VDDIO)}$   | supply voltage on pin VDDIO     | on pin VDDIO, power supply for host interface and GPIOs                   | -0.3  | 3.8   | V    |
| $V_{DD(VDDPA)}$   | supply voltage on pin VDDPA     | maximum limiting values for $I_{DD(VDDPA)}$ and $T_{j(max)}$ not violated | -     | 6.0   | V    |
| $V_{i(RXP)}$      | input voltage on pin RXP        | -   | -0.3  | + 2.0 | V    |
| $V_{i(RXN)}$      | input voltage on pin RXN        | -   | -0.3  | + 2.0 | V    |
| $V_{ESD}$         | electrostatic discharge voltage | human body model (HBM) <sup>[1]</sup>                                     | -2000 | 2000  | V    |
|                   |                                 | charge device model (CDM) <sup>[2]</sup>                                  | -500  | +500  | V    |
| $T_{j(max)}$      | junction temperature            | -   | -     | 125   | °C   |
| $T_{stg}$         | storage temperature             | no supply voltage applied   | -55   | +150  | °C   |

[1] According to ANSI/ESDA/JEDEC JS-001

[2] According to ANSI/ESDA/JEDEC JS-002

Stress above one or more of the limiting values may cause permanent damage to the device or limit the lifetime. Product might not behave according to specification.

## 11 Characteristics

This chapter describes the electrical characteristics for the usage of the product.

Functionality according to this specification and compliancy to referred standards is guaranteed if the device is operated within the limits.

For further information, refer to the PQP (product qualification package) which summarizes the results of the characterization and qualification performed.

### 11.1 Thermal characteristics

Table 301. Operating conditions

| Symbol           | Parameter                     | Conditions  | Min | Typ | Max  | Unit |
|------------------|-------------------------------|---|-----|-----|------|------|
| T <sub>amb</sub> | ambient operating temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB, transmitter output current up to 350 mA | -40 | +25 | +85  | °C   |
|                  |                               | in still air with exposed pins soldered on a 4 layer JEDEC PCB, TX current = 120 mA @ VDDPA=3.6 V       | -40 | +25 | +105 | °C   |

Table 302. Thermal characteristics VFLGA40 package

| Symbol               | Parameter                                   | Conditions  | Typ  | Unit |
|----------------------|---|---|------|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFLGA40 | 44.2 | K/W  |
| R <sub>th(j-c)</sub> | thermal resistance from junction to case    | -   | 24.2 | K/W  |

Table 303. Thermal characteristics VFBGA64 package

| Symbol               | Parameter                                   | Conditions  | Typ | Unit |
|----------------------|---|---|-----|------|
| R <sub>th(j-a)</sub> | thermal resistance from junction to ambient | in free air with exposed pad soldered on a 4 layer JEDEC PCB, package VFBGA64 | 53  | K/W  |
| R <sub>th(j-c)</sub> | thermal resistance from junction to case    | -   | 22  | K/W  |

Table 304. Junction Temperature

| Symbol             | Parameter                    | Conditions | Min | Max  | Unit |
|--------------------|------------------------------|------------|-----|------|------|
| T <sub>l_max</sub> | maximum junction temperature | -          | -   | +125 | °C   |

Table 305. Thermal Shutdown Temperature

| Symbol                | Parameter  | Conditions | Typ | Unit |
|-----------------------|--|------------|-----|------|
| T <sub>shutdown</sub> | shutdown of chip due to high temperature detected by temp sensor | -          | 125 | °C   |

11.2 Static characteristics

Table 306. Supply voltage

| Symbol                     | Parameter  | Conditions   | Min  | Typ | Max  | Unit |
|----------------------------|--|--|------|-----|------|------|
| V <sub>DD</sub> (VBAT_PWR) | supply voltage on pin VBAT_PWR (DC-DC input pin)                       | DC-DC disabled   | 2.4  | -   | 5.5  | V    |
|                            |  | DC-DC enabled  | 2.8  | -   | 4.8  | V    |
| V <sub>DD</sub> (VUP_TX)   | supply voltage on pin VUP_TX (TX_LDO input pin)                        | Remark: If DC-DC is used, its output V <sub>DD</sub> (BOOST) Min is limited to 3.1 V | 2.4  | -   | 6.0  | V    |
| V <sub>DD</sub> (VDDPA)    | supply voltage on pin VDDPA (input of the transmitter power amplifier) | -  | 1.5  | -   | 5.7  | V    |
| V <sub>DD</sub> (VBAT)     | supply voltage on pin VBAT (analog and digital supply)                 | VBAT >= VDDIO  | 2.4  | -   | 5.5  | V    |
| V <sub>DD</sub> (VDDIO)    | supply voltage on pin VDDIO (supply for host interface and GPIOs)      | typical 1.8 V interface supply voltage   | 1.62 | -   | 1.98 | V    |
|                            |  | typical 3.3 V interface supply voltage   | 2.4  | -   | 3.6  | V    |
| V <sub>I</sub> (RXP)       | input voltage on pin RXP   | -  | -0.5 | -   | 1.8  | V    |
| V <sub>I</sub> (RXN)       | input voltage on pin RXN   | -  | -0.5 | -   | 1.8  | V    |

**Note:** The voltage on pin VDDIO must always be smaller or equal to the voltage on pin VBAT.

Table 307. Current consumption in active mode

| Symbol                     | Parameter                                | Conditions   | Min | Typ | Max | Unit |
|----------------------------|--|--|-----|-----|-----|------|
| I <sub>DD</sub> (VBAT)     | system supply                            |  | -   | -   | 20  | mA   |
| I <sub>DD</sub> (VDDIO)    |  | This current depends on the output current of peripherals. At no time, the sum of the maximum output currents shall exceed I <sub>DD</sub> (VDDIO) max | -   | -   | 30  | mA   |
| I <sub>DD</sub> (BOOST_IN) | DC-DC boost supply                       | average input current  | -   | -   | 1.0 | A    |
|                            |  | peak input current (short peak)  | -   | -   | 1.7 | A    |
| I <sub>DD</sub> (VUP_TX)   | input supply for transmitter LDO         | -  | -   | -   | 350 | mA   |
| I <sub>DD</sub> (VDDPA)    | RF power amplifier (transmitter) current | supplied via VUP_TX (TX_LDO active)  | -   | -   | 350 | mA   |
|                            |  | supplied without DC-DC and without TXLDO active  | -   | -   | 400 | mA   |



Table 308. Current consumption during power-saving modes

| Symbol                                       | Parameter   | Conditions   | Min | Typ | Max | Unit |
|--|---|--|-----|-----|-----|------|
| $I_{\text{OFF Plus Mode (VDDIO+VBAT)}}$      | sum of supply current on pin VDDIO and VBAT in OFF Plus mode  | 25 °C ambient operating temperature  | -   | 5   | -   | μA   |
| $I_{\text{OFF Plus ULFO Mode (VDDIO+VBAT)}}$ | sum of supply current on pin VDDIO and VBAT in OFF Plus mode, ULFO active (ULPCD during RF-OFF)   | 25 °C ambient operating temperature  | -   | 5   | -   | μA   |
| $I_{\text{hard power down (VDDIO+VBAT)}}$    | sum of supply current on pin VDDIO and VBAT in hard Power-down mode   | 25 °C ambient operating temperature  | -   | 40  | 105 | μA   |
| $I_{\text{standby (VDDIO+VBAT)}}$            | sum of supply current on pin VDDIO and VBAT in Standby mode   | 25 °C ambient operating temperature  | -   | 45  | 110 | μA   |
| $I_{\text{suspend (VBAT)}}$                  | supply current on pin VBAT in suspend mode  | 25 °C ambient operating temperature  | -   | 2.5 | -   | mA   |
| $I_{\text{ULPCD (VDDIO+VBAT)}}$              | sum of supply current on pin VDDIO and VBAT in ULPCD (Ultra Low-Power Card Detection) mode  | 25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second | -   | 22  | -   | μA   |
| $I_{\text{LPCD (VDDIO+VBAT)}}$               | sum of supply current on pin VDDIO and VBAT in LPCD (Enhanced Low-Power Card Detection with highest sensitivity) mode, without DC-DC used | 25 °C ambient operating temperature, VBAT supply voltage 3.3 V, antenna matching 50 R, 3.3 V antenna supply voltage, 3x RF-on per second | -   | 240 | -   | μA   |

Table 309. Overcurrent detection function <sup>[1]</sup>

| Symbol                   | Parameter  | Conditions | Min | Typ | Max | Unit |
|--------------------------|--|------------|-----|-----|-----|------|
| $I_{\text{DD(VUP\_TX)}}$ | current of overcurrent detection becoming active | -          | 450 | 550 | 650 | mA   |

[1] Refer to the Errata sheet. In normal operation within spec limits, this flag shall not be triggered under any circumstances. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active. The overcurrent protection shall be treated as an additional safety feature only.

This is a safety feature only. A design shall not functionally rely on this feature since the operating conditions will be violated if the overcurrent detection becomes active.

Table 310. VEN pin

| Symbol          | Parameter                | Conditions                                      | Min                          | Typ | Max                          | Unit |
|-----------------|--------------------------|---|------------------------------|-----|------------------------------|------|
| $V_{\text{IH}}$ | HIGH-level input voltage | $V_{\text{DD(VDDIO)}} \leq V_{\text{DD(VBAT)}}$ | 0.7 * $V_{\text{DD(VDDIO)}}$ | -   | $V_{\text{DD(VDDIO)}}$       | V    |
| $V_{\text{IL}}$ | LOW-level input voltage  |   | 0                            | -   | 0.3 * $V_{\text{DD(VDDIO)}}$ | V    |

Table 310. VEN pin ...continued

| Symbol                     | Parameter                        | Conditions                             | Min | Typ | Max | Unit |
|----------------------------|----------------------------------|--|-----|-----|-----|------|
| I <sub>IH</sub>            | HIGH-level input current         | V <sub>I</sub> = V <sub>DD(VBAT)</sub> | -   | -   | 1   | μA   |
| I <sub>IL</sub>            | LOW-level input current          | V <sub>I</sub> = 0 V                   | -1  | -   | -   | μA   |
| C <sub>i</sub>             | input capacitance                |  | -   | 5   | -   | pF   |
| t <sub>(ULPCD_abort)</sub> | VEN time required to abort ULPCD |  | 5   | -   | -   | ms   |

Table 311. GPIO input / output pins (GPIO\_0 - 5, SWDIO)

| Symbol          | Parameter                 | Conditions  | Min         | Typ | Max          | Unit |
|-----------------|---------------------------|---|-------------|-----|--------------|------|
| V <sub>IH</sub> | HIGH-level input voltage  | V <sub>DD(VDDIO)</sub> ≤ V <sub>DD(VBAT)</sub> ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6 | 0.65x VDDIO | -   | VDDIO+0.5    | V    |
| V <sub>IL</sub> | LOW-level input voltage   | V <sub>DD(VDDIO)</sub> ≤ V <sub>DD(VBAT)</sub> ; 1.62 ≤ VDDIO ≤ 1.98 or 2.4 ≤ VDDIO ≤ 3.6 | - 0.5       | -   | 0.35 × VDDIO | V    |
| V <sub>OH</sub> | HIGH-level output voltage | V <sub>DD(VDDIO)</sub> = 3.3 V<br>2.4 ≤ VDDIO ≤ 3.6                                       | VDDIO - 0.4 | -   | VDDIO        | V    |
| V <sub>OL</sub> | LOW-level output voltage  | V <sub>DD(VDDIO)</sub> = 3.3 V<br>2.4 ≤ VDDIO ≤ 3.6                                       | 0           | -   | 0.4          | V    |
| I <sub>OH</sub> | HIGH-level output current | V <sub>DD(VDDIO)</sub> = 3.3 V<br>2.4 ≤ VDDIO ≤ 3.6                                       | -           | -   | 3            | mA   |
| I <sub>OL</sub> | LOW-level output current  | V <sub>DD(VDDIO)</sub> = 3.3 V<br>2.4 ≤ VDDIO ≤ 3.6                                       | -           | -   | 3            | mA   |
| R <sub>PU</sub> | Weak pullup resistor      |   | 40          | 50  | 62           | kΩ   |
| R <sub>PD</sub> | Weak pulldown resistor    |   | 40          | 50  | 62           | kΩ   |

Table 312. XTAL1, XTAL2 pins

| Symbol               | Parameter                     | Conditions  | Min | Typ | Max  | Unit |
|----------------------|-------------------------------|---|-----|-----|------|------|
| V <sub>i(p-p)</sub>  | peak-to-peak input voltage    | -   | 0.4 | -   | 1.65 | V    |
| I <sub>IH</sub>      | HIGH-level input current      | V <sub>I</sub> = 1.65 V, no power saving, active mode | -   | -   | 5    | μA   |
| I <sub>IL</sub>      | LOW-level input current       | V <sub>I</sub> = 0 V, no power saving, active mode    | -   | -   | 1    | μA   |
| δ                    | duty cycle                    | -   | 35  | -   | 65   | %    |
| C <sub>i(CLK1)</sub> | input capacitance on pin CLK1 | VDD = 1.8 V,<br>VDC = 0.65 V,<br>VAC = 0.9 V (p-p)    | -   | 1   | -    | pF   |
| C <sub>i(CLK2)</sub> | input capacitance on pin CLK2 | VDD = 1.8 V,<br>VDC = 0.65 V,<br>VAC = 0.9 V (p-p)    | -   | 1   | -    | pF   |

Table 313. IRQ pin

| Symbol          | Parameter                 | Conditions                 | Min                            | Typ | Max                    | Unit |
|-----------------|---------------------------|----------------------------|--------------------------------|-----|------------------------|------|
| V <sub>OH</sub> | HIGH-level output voltage | I <sub>OH</sub> < 3 mA     | V <sub>DD(VDDIO)</sub><br>-0.4 | -   | V <sub>DD(VDDIO)</sub> | V    |
| V <sub>OL</sub> | LOW-level output voltage  | I <sub>OL</sub> < 3 mA     | 0                              | -   | 0.4                    | V    |
| I <sub>OH</sub> | HIGH-level output current |                            | -                              | -   | 3                      | mA   |
| I <sub>OL</sub> | LOW-level output current  |                            | -                              | -   | 3                      | mA   |
| C <sub>L</sub>  | load capacitance          |                            | -                              | -   | 10                     | pF   |
| t <sub>f</sub>  | fall time                 | C <sub>L</sub> = 12 pF max | 1                              | -   | 3                      | ns   |
| t <sub>r</sub>  | rise time                 | C <sub>L</sub> = 12 pF max | 1                              | -   | 3                      | ns   |
| R <sub>pd</sub> | pull-down resistance      |                            | 40                             | -   | 62                     | kΩ   |

Table 314. ATX\_B, ATX\_C, ATX\_D pins (SPI (SCLK, COTI, NTS))

| Symbol          | Parameter                | Conditions                          | Min                              | Typ | Max                              | Unit |
|-----------------|--------------------------|-------------------------------------|----------------------------------|-----|----------------------------------|------|
| V <sub>IH</sub> | HIGH-level input voltage |                                     | 0.65 x<br>V <sub>DD(VDDIO)</sub> | -   | V <sub>DD(VDDIO)</sub>           | V    |
| V <sub>IL</sub> | LOW-level input voltage  |                                     | - 0.5                            | -   | 0.35 x<br>V <sub>DD(VDDIO)</sub> | V    |
| I <sub>IH</sub> | HIGH-level input current | V <sub>I</sub> = V <sub>VDDIO</sub> | -                                | -   | 1                                | μA   |
| I <sub>IL</sub> | LOW-level input current  | V <sub>I</sub> = 0 V                | -                                | -   | 1                                | μA   |
| C <sub>i</sub>  | input capacitance        |                                     | -                                | 5   | -                                | pF   |

Table 315. ATX\_A pin (SPI (CITO))

| Symbol          | Parameter                 | Conditions                 | Min                            | Typ | Max                    | Unit |
|-----------------|---------------------------|----------------------------|--------------------------------|-----|------------------------|------|
| V <sub>OH</sub> | HIGH-level output voltage | I <sub>OH</sub> < 3 mA     | V <sub>DD(VDDIO)</sub><br>-0.4 | -   | V <sub>DD(VDDIO)</sub> | V    |
| V <sub>OL</sub> | LOW-level output voltage  | I <sub>OL</sub> < 3 mA     | 0                              | -   | 0.4                    | V    |
| I <sub>OH</sub> | HIGH-level output current |                            | -                              | -   | 3                      | mA   |
| I <sub>OL</sub> | LOW-level output current  |                            | -                              | -   | 3                      | mA   |
| C <sub>L</sub>  | load capacitance          |                            | -                              | -   | 10                     | pF   |
| t <sub>f</sub>  | fall time                 | C <sub>L</sub> = 12 pF max | 1                              | -   | 3                      | ns   |
| t <sub>r</sub>  | rise time                 | C <sub>L</sub> = 12 pF max | 1                              | -   | 3                      | ns   |

Table 316. RXp, RXn pins

| Symbol              | Parameter                                  | Conditions                  | Min | Typ | Max | Unit |
|---------------------|--|-----------------------------|-----|-----|-----|------|
| V <sub>i(dyn)</sub> | dynamic input voltage                      |                             | -   | -   | 1.8 | V    |
| C <sub>i</sub>      | input capacitance                          |                             | -   | 1   | -   | pF   |
| Z <sub>i</sub>      | input impedance from RXN, RXP pins to VMID | Reader, card, and P2P modes | -   | -   | 15  | kΩ   |

Table 317. TX1, TX2 pins

| Symbol          | Parameter                 | Conditions   | Min | Typ                            | Max                    | Unit |
|-----------------|---------------------------|--|-----|--------------------------------|------------------------|------|
| V <sub>OH</sub> | HIGH-level output voltage | V <sub>DD(VDDPA)</sub> =5.0 V; with internal VDDPA LDO | -   | V <sub>DD(VDDPA)</sub> -150 mV | V <sub>DD(VDDPA)</sub> | V    |
| V <sub>OL</sub> | LOW-level output voltage  | V <sub>DD(VDDPA)</sub> =5.0 V; with internal VDDPA LDO | 0   | 200                            | -                      | m    |

Table 318. AUX1, AUX2, AUX3 pins (Debug output)

| Symbol              | Parameter                      | Conditions                      | Min        | Typ | Max   | Unit |
|---------------------|--------------------------------|---------------------------------|------------|-----|-------|------|
| V <sub>AUX_OH</sub> | HIGH-level output voltage      | pin used as debug signal output | VDDIO -0.4 | -   | VDDIO | V    |
| V <sub>AUX_OL</sub> | LOW-level output voltage       | pin used as debug signal output | 0          | -   | 0.4   | V    |
| I <sub>AUX_OH</sub> | HIGH-level output current      | V <sub>DD(VDDIO)</sub> = 3.3 V  | -          | -   | 3.0   | mA   |
| I <sub>AUX_OL</sub> | LOW-level output current       | V <sub>DD(VDDIO)</sub> = 3.3 V  | -          | -   | 3.0   | mA   |
| C <sub>O_LOAD</sub> | output capacitance load of pin |                                 | -          | 5   | 10    | pF   |

Table 319. VTUNE0 and VTUNE1 output pins (Tuning DAC)

| Symbol                    | Parameter                                | Conditions  | Min  | Typ                    | Max  | Unit |
|---------------------------|--|---|------|------------------------|------|------|
| V <sub>O_VTUNE1_max</sub> | HIGH-level maximum output voltage VTUNE1 | connected to a variable capacitor (varicap), VDDIO = 3.3 V<br>Remark: Output voltage is limited by VDDIO and cannot be higher than this supply. | -    | V <sub>DD(VDDIO)</sub> | 3.65 | V    |
| V <sub>O_VTUNE0_max</sub> | HIGH-level maximum output voltage VTUNE0 | connected to a variable capacitor (varicap), VBAT = 3.3 V<br>Remark: Output voltage is limited by VBAT and cannot be higher than this supply.   | -    | V <sub>DD(VBAT)</sub>  | 3.65 | V    |
| V <sub>O_min</sub>        | LOW-level minimum output voltage         | connected to a variable capacitor (varicap)   | -0.3 | 0                      | 200  | mV   |
|                           | DAC resolution                           |   | -    | -                      | 8    | bits |
| C <sub>O_LOAD</sub>       | output capacitance load of pin           |   | 0    | -                      | 4    | nF   |

## 11.3 Timing characteristics

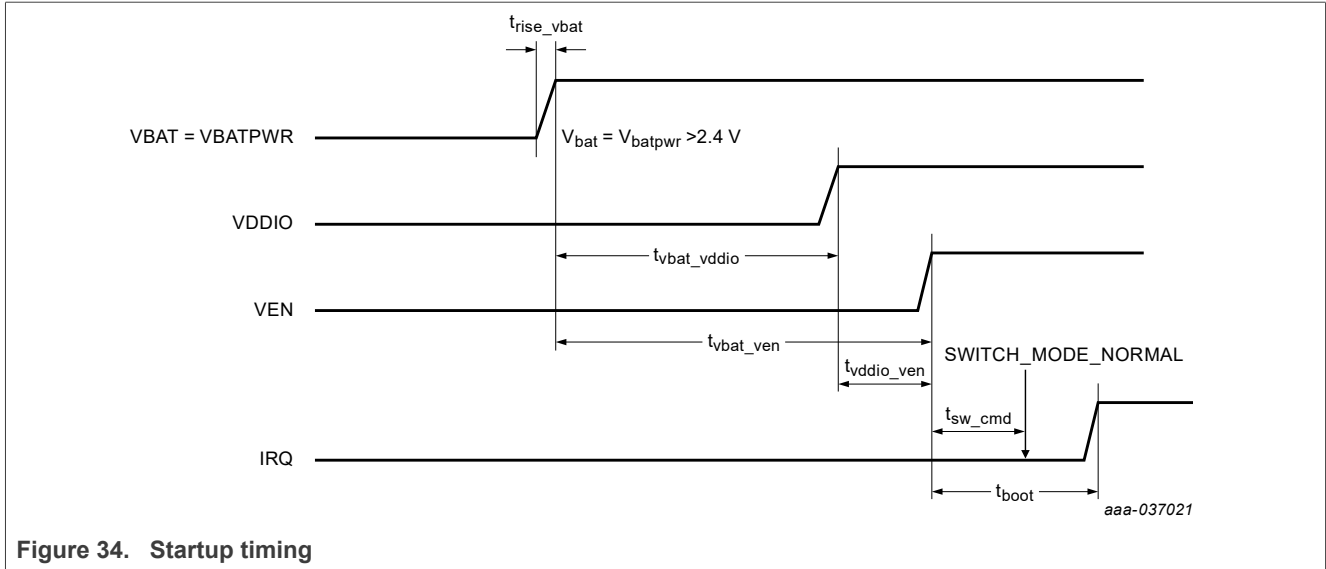


Figure 34. Startup timing

After VEN reset and  $t_{swcmd}$  are lapsed, SWITCH\_MODE\_NORMAL command shall be issued to enter normal mode of operation. Recommended value of  $t_{swcmd} = 500\ \mu\text{s}$ .

Table 320. Power supply connection timing

| Symbol            | Parameter                                      | Conditions  | Min | Typ   | Max  | Unit             |
|-------------------|--|---|-----|-------|--|------------------|
| $t_{rise\_vbat}$  | VBAT supply ramp                               | VEN = Low   | 0   | -     | 2.75   | V/ $\mu\text{s}$ |
| $t_{vbat\_vddio}$ | time between ramping up VBAT and ramping VDDIO | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 0   | 500   | 1000   | ms               |
| $t_{vbat\_ven}$   | time between ramping VBAT and VEN              | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 0   | 500.5 | 1001   | ms               |
| $t_{boot}$        | start-up time <sup>[1]</sup>                   | vddio condition: VBAT>2.4 V, VDDIO supply (External), hpd_off_sel = x | 3.2 | 3.27  | dependent on configuration of XTAL_CHECK_DELAY (0013h) in EEPROM. This configuration can be used to optimize the boot time for crystals which allow a fast settling. This allows to optimize the average current consumption during ULPCD and LPCD.<br>default EEPROM configuration: 3.4 | ms               |

[1] (PN5190B1 ready to receive commands on the host interface). For ULPCD and LPCD, the PN5190B1 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 321. Pulse length

| Symbol          | Parameter  | Conditions | Min | Typ | Max | Unit    |
|-----------------|--|------------|-----|-----|-----|---------|
| $t_{(VEN)}$     | on Pin VEN, pulse width to reset the chip or exit from ULPCD / Hard power down State | -          | 5   | -   | -   | ms      |
| $t_{(wake-up)}$ | on pin GPIOx, pulse width to wake up   | -          | 1   | -   | -   | $\mu$ s |
| $t_{VEN(GPIO)}$ | time from VEN high to GPIO's available for use                                       | -          | 100 | -   | -   | ms      |

Table 322. DAC1, DAC2 conversion timing (Tuning DAC)

| Symbol           | Parameter                            | Conditions  | Min | Typ | Max  | Unit |
|------------------|--------------------------------------|---|-----|-----|------|------|
| $t_{conversion}$ | Conversion speed of 8-bit DAC1, DAC2 | 1 LSB rising falling, (depends on capacitive load)<br>RF cut resistance: 100 kOhm (max),<br>Cin: 8 nF (max)                 | -   | -   | 0.15 | ms   |
|                  |                                      | Full signal rising from 0.0 V to 3 V, (depends on capacitive load)<br>RF cut resistance: 100 kOhm (max),<br>Cin: 8 nF (max) | -   | -   | 0.15 | ms   |
|                  |                                      | falling from 3 V to 300 mV, (depends on capacitive load)<br>RF cut resistance: 100 kOhm (max),<br>Cin: 8 nF (max)           | -   | -   | 2    | ms   |

Table 323. SPI interface

| Symbol           | Parameter                          | Min   | Typ | Max | Unit |
|------------------|------------------------------------|-------|-----|-----|------|
| $t_{SCKL}$       | SCK LOW time                       | 33.3  | -   | -   | ns   |
| $t_{SCKH}$       | SCK HIGH time                      | 33.3  | -   | -   | ns   |
| $t_{h(SCKH-D)}$  | SCK HIGH to data input hold time   | 16.65 | -   | -   | ns   |
| $t_{su(D-SCKH)}$ | data input to SCK HIGH set-up time | 16.65 | -   | -   | ns   |
| $t_{h(SCKL-Q)}$  | SCK LOW to data output hold time   | -     | -   | 25  | ns   |

Table 323. SPI interface...continued

| Symbol            | Parameter                | Min  | Typ | Max | Unit |
|-------------------|--------------------------|------|-----|-----|------|
| $t_{(SCKL-NSSH)}$ | SCK LOW to NTS HIGH time | 0    | -   | -   | ns   |
| $t_{NSSH}$        | NTS HIGH time            | 33.3 | -   | -   | ns   |

Table 324. RF\_ON command timing following a previous RF\_OFF

| Symbol                 | Parameter            | Conditions  | Min | Typ | Max | Unit |
|------------------------|----------------------|---|-----|-----|-----|------|
| $t_{(RF\_OFF-RF\_ON)}$ | RF_ON command timing | guard time between command sends for RF_OFF and command send for RF_ON, capacitors on transmitter must be fully de-charged before RF_ON command is sent | 5.1 | 5.6 | -   | ms   |

## 11.4 DPC characteristics

Table 325. Dynamic power control characteristics

| Symbol | Parameter   | Conditions  | Min                                      | Typ | Max            | Unit |
|--------|---|---|--|-----|----------------|------|
|        | Minimum hysteresis configured in EEPROM DPC_HYSTERESIS (address 079h) | Depends on application target current                     | ApplicationTargetCurrent * 0.0609 + 2 mA | -   | -              | mA   |
|        | Max target current configured in EEPROM DPC_TARGET_CURRENT (077h)     | Hysteresis as configured in DPC_HYSTERESIS (address 079h) |  | -   | 350-Hysteresis | mA   |

## 11.5 Clock input

Table 326. Crystal requirements for ISO/IEC14443 compliant operation

| Symbol                   | Parameter                    | Conditions                  | Min | Typ   | Max | Unit          |
|--------------------------|------------------------------|-----------------------------|-----|-------|-----|---------------|
| $f_{\text{xtal}}$        | crystal frequency            | ISO/IEC compliancy          | -   | 27.12 | -   | MHz           |
| $\Delta f_{\text{xtal}}$ | crystal frequency accuracy   | for full RF operating range | -40 | -     | +40 | ppm           |
| ESR                      | equivalent series resistance | -                           | 10  | 30    | 100 | $\Omega$      |
| $C_L$                    | load capacitance             | -                           | 6   | 8     | 10  | pF            |
| $t_{\text{startup}}$     | crystal startup time         | -                           | -   | -     | 1   | ms            |
| $P_{\text{xtal}}$        | crystal power dissipation    | -                           | -   | -     | 100 | $\mu\text{W}$ |

Table 327. Frequency requirements for a direct clock input (no crystal)

| Symbol                  | Parameter                  | Conditions                                | Min | Typ   | Max           | Unit   |
|-------------------------|----------------------------|---|-----|-------|---------------|--------|
| $f_{\text{clk}}$        | clock frequency            | ISO/IEC compliancy                        | -   | 24    | -             | MHz    |
|                         |                            |   | -   | 32    | -             |        |
|                         |                            |   | -   | 48    | -             |        |
| $\Delta f_{\text{clk}}$ | clock frequency accuracy   | for full RF operating range               | -40 | -     | +40           | ppm    |
| $\varphi_n$             | phase noise                | input phase noise floor at 100 kHz offset | -   | - 150 | -145          | dBc/Hz |
| $\varphi_n$             | phase noise                | input phase noise floor at 1 MHz offset   | -   | - 152 | -149          | dBc/Hz |
| $V_i$                   | Input voltage boundary     | sinus signal                              | 0   | -     | 1.8           | V      |
| $V_{i(p-p)}$            | peak-to-peak Input voltage | sinus signal                              | 0.4 | -     | 1.8           | V      |
| $V_{i(\text{clk})}$     | clock input voltage        | square signal                             | 0   | -     | 1.8<br>+/-10% | V      |



## 11.6 EEPROM characteristics

Table 328. EEPROM characteristics

| Symbol               | Parameter       | Conditions                                      | Min | Typ | Max | Unit     |
|----------------------|-----------------|---|-----|-----|-----|----------|
| $N_{\text{endu(W)}}$ | write endurance | at ambient temperature<br>$T_a = +25\text{ °C}$ | 100 | -   | -   | K cycles |
| $t_{\text{ret}}$     | retention time  | at ambient temperature<br>$T_a = +25\text{ °C}$ | 25  | -   | -   | years    |

## 12 Package outline

### 12.1 VFBGA64 package

Table 329. Package outline VFBGA64 (SOT1307-2)

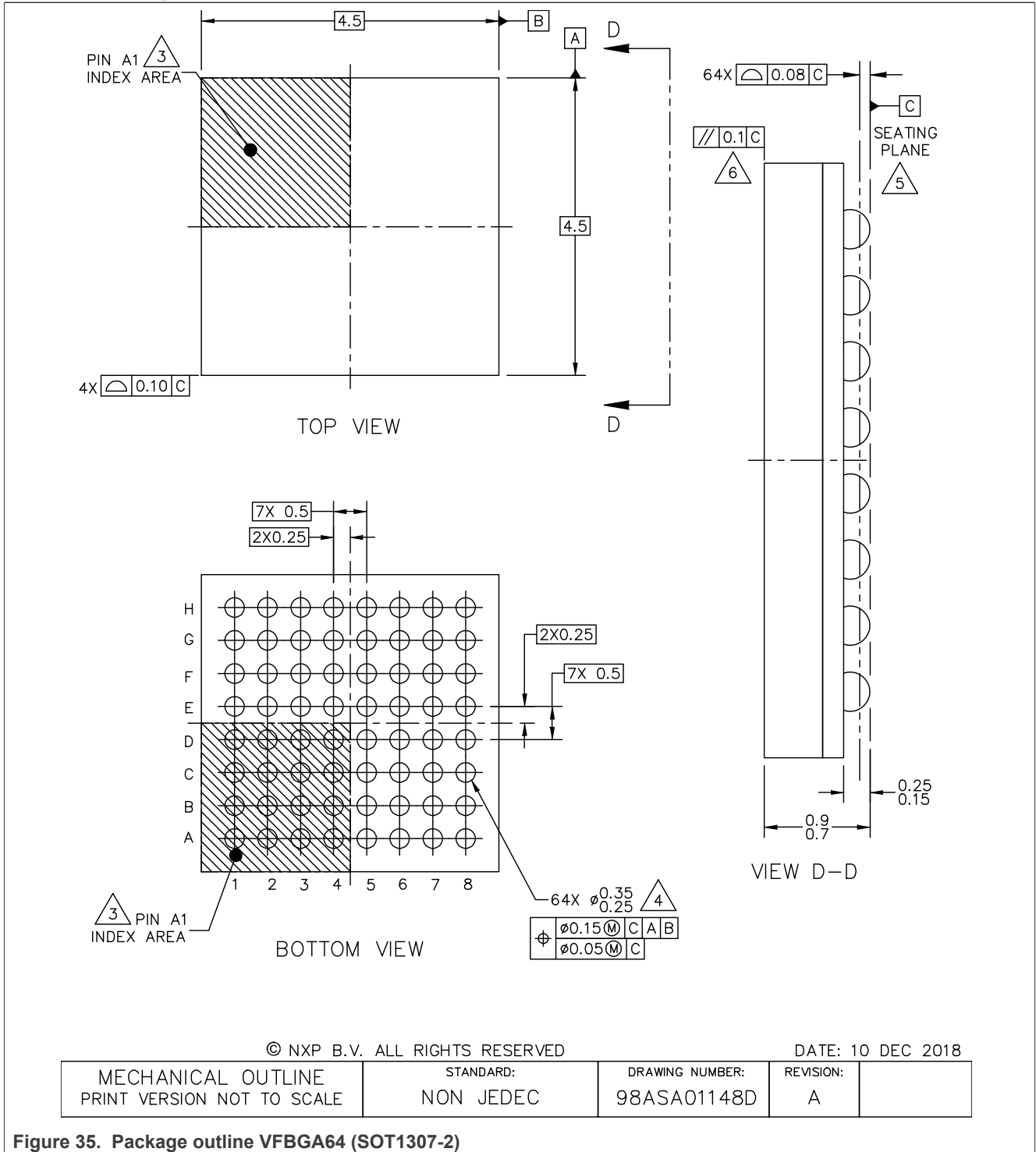


Figure 35. Package outline VFBGA64 (SOT1307-2)

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

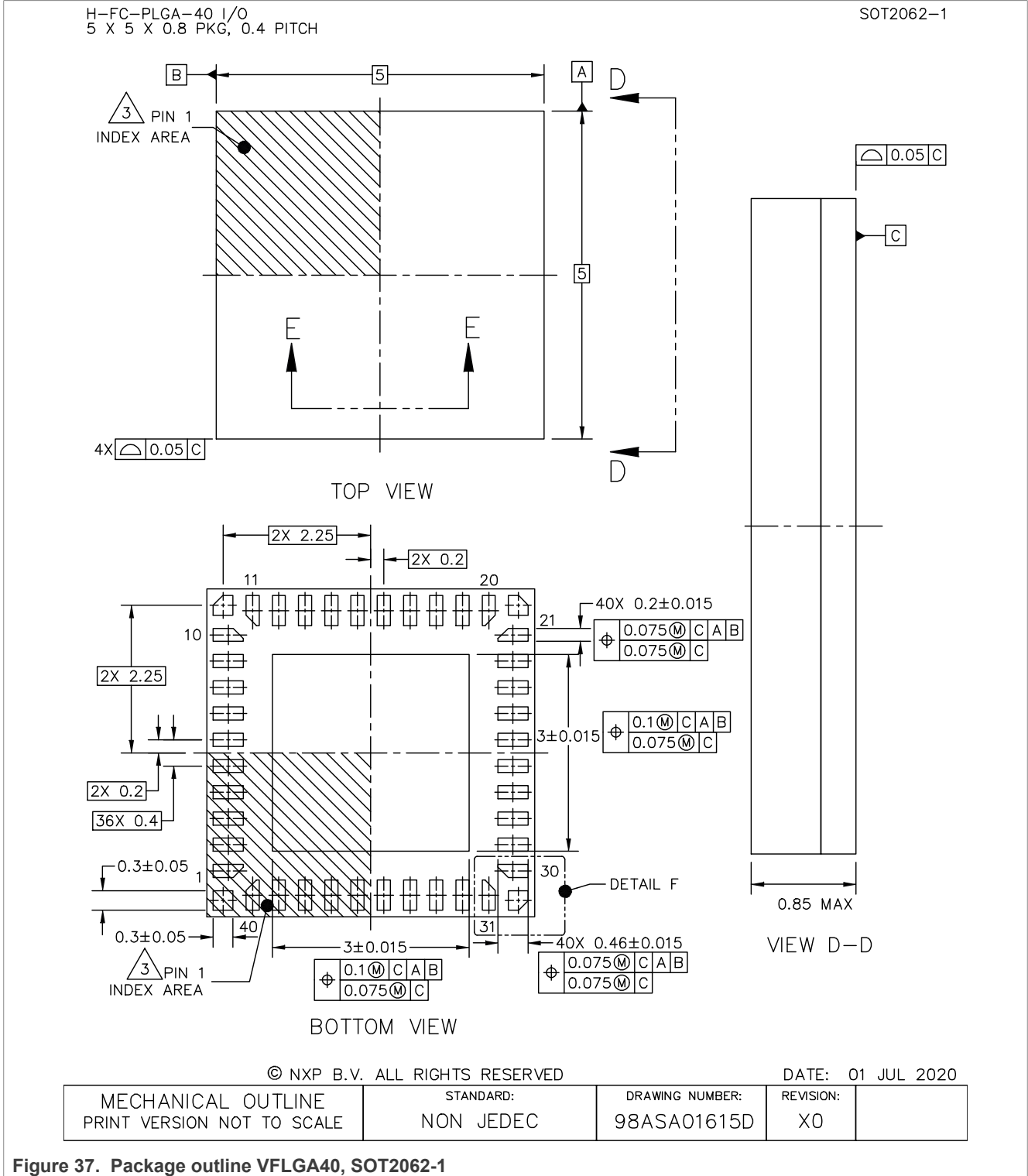
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DATE: 10 DEC 2018

|  |                        |                                |                |  |
|--|------------------------|--------------------------------|----------------|--|
| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01148D | REVISION:<br>A |  |
|--|------------------------|--------------------------------|----------------|--|

Figure 36. Package outline note VFBGA64 (SOT1307-2)

12.2 VFLGA40 package



H-FC-PLGA-40 I/O  
5 X 5 X 0.8 PKG, 0.4 PITCH

SOT2062-1

NOTES:

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. DIMENSION APPLIES TO ALL LEADS.

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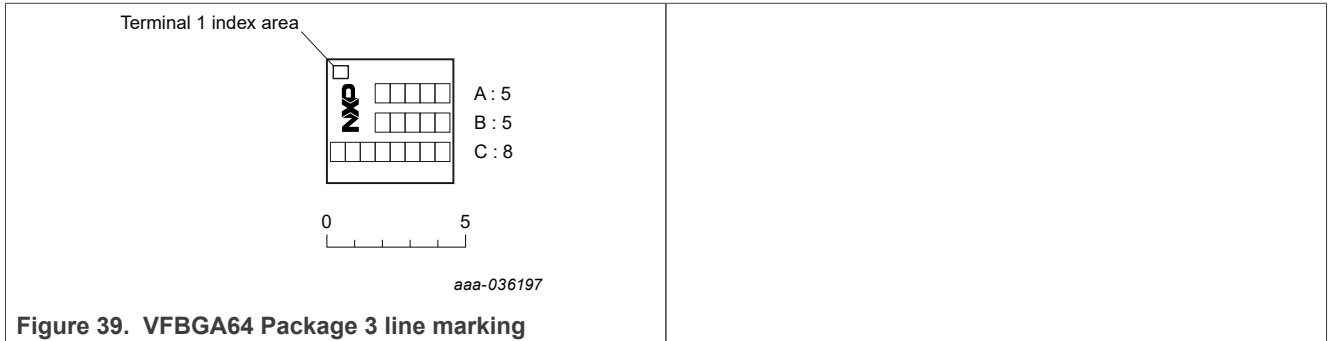
DATE: 01 JUL 2020

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| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01615D | REVISION:<br>X0 |  |
|--|------------------------|--------------------------------|-----------------|--|

Figure 38. Package outline detail VFLGA40, SOT2062-1

### 13 Package marking

#### 13.1 Package marking drawing VFBGA64

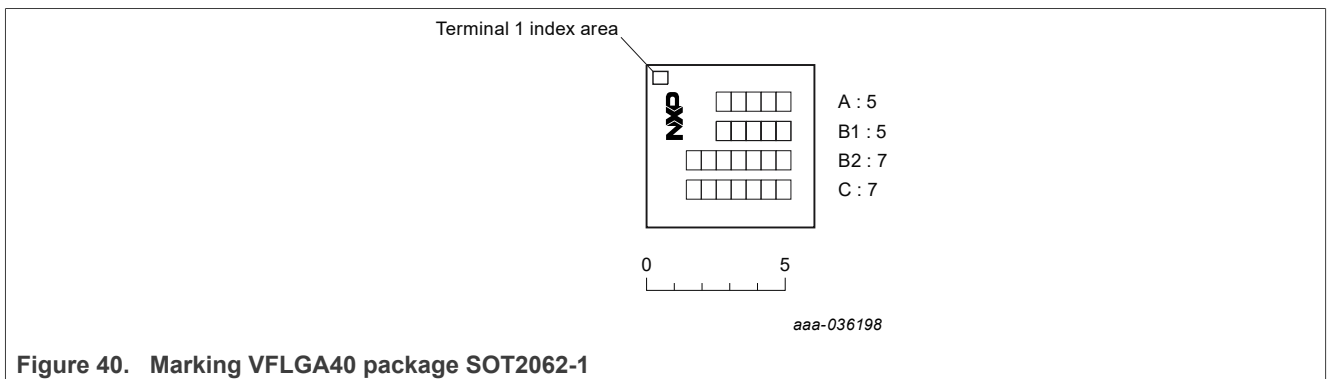


Line A: 5 characters; "PN5190D" (FW2.0) or "5190E" (FW2.1)

Line B: 5 characters; contains the DB ID and AS ID

Line C: 8 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level ("X" = engineering samples, " " = released product)

#### 13.2 Package marking drawing VFLGA40



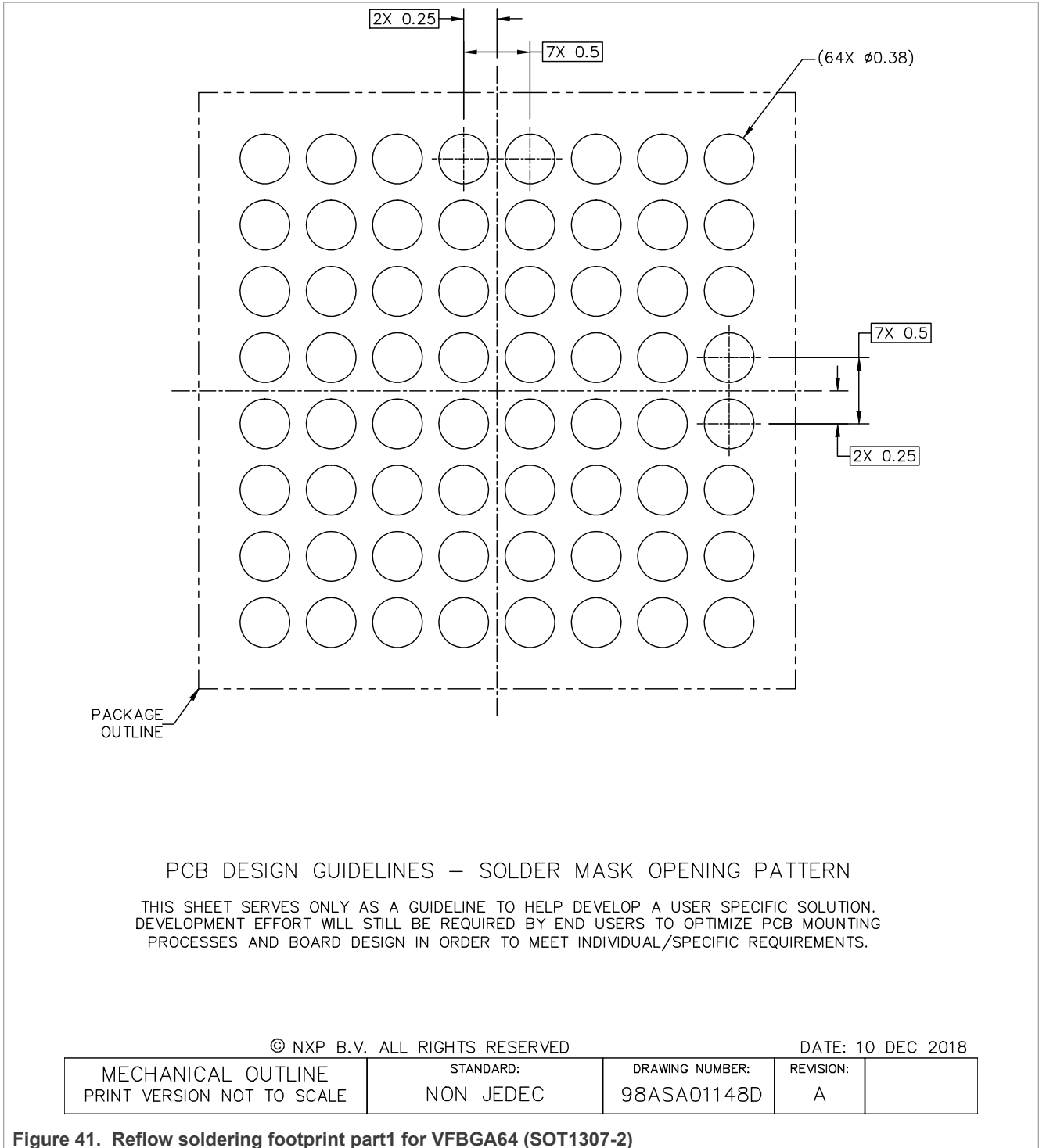
Line A: 5 characters; "PN5190D" (FW2.0) or "5190E" (FW2.1)

Line B1: 5 characters; contains the DB ID

Line B2: 7 characters; contains the DB ID (continued) and AS ID (2 digits)

Line C: 7 characters; stDYYWW(X) - contains information assembly center, date code, and maturity level ("X" = engineering samples, "Y" = customer qualification samples, " " = released product)

### 14 Reflow soldering footprint VFBGA64



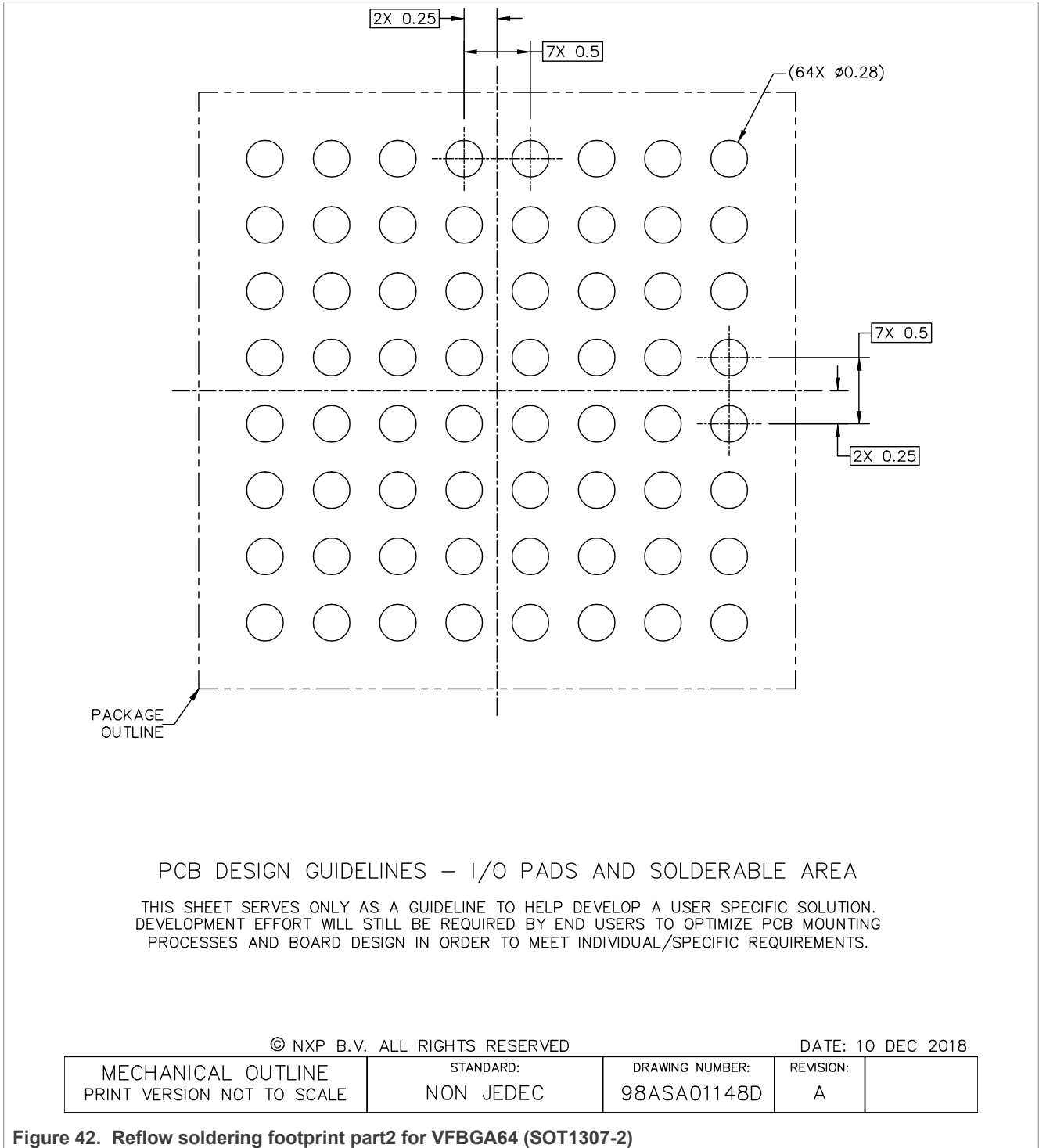


Figure 42. Reflow soldering footprint part2 for VFBGA64 (SOT1307-2)



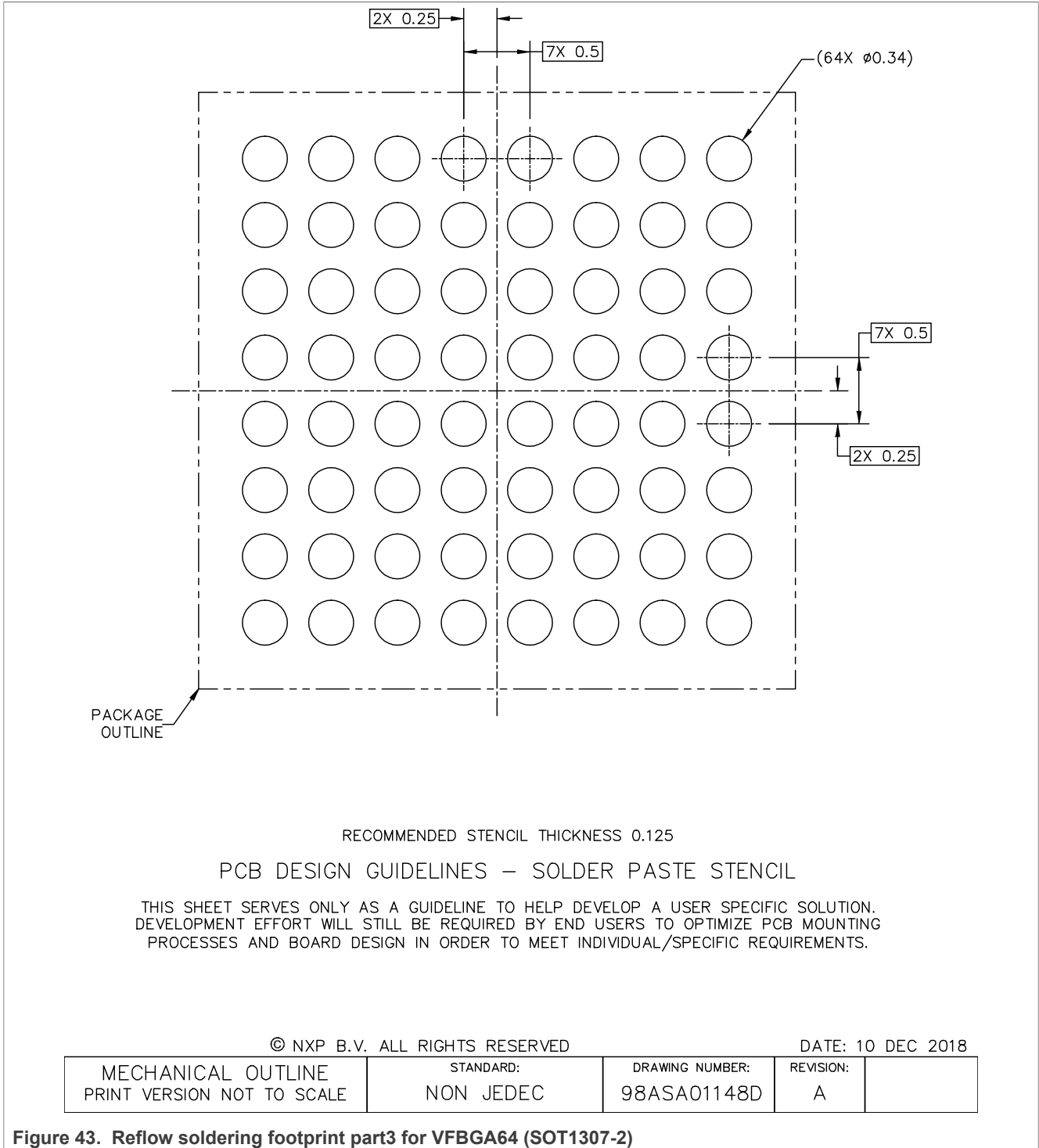


Figure 43. Reflow soldering footprint part3 for VFBGA64 (SOT1307-2)

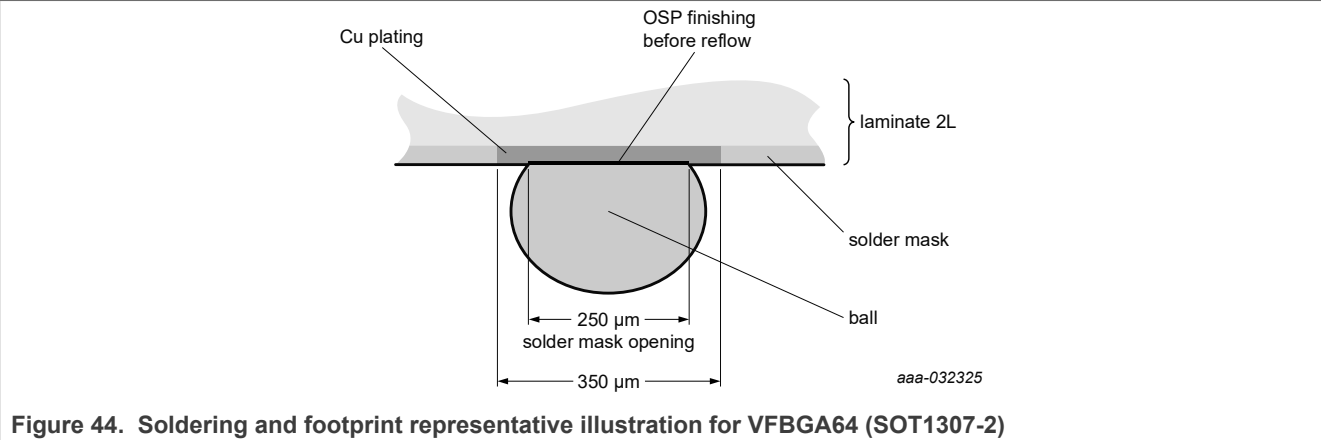


Figure 44. Soldering and footprint representative illustration for VFBGA64 (SOT1307-2)

15 Reflow soldering footprint VFLGA40

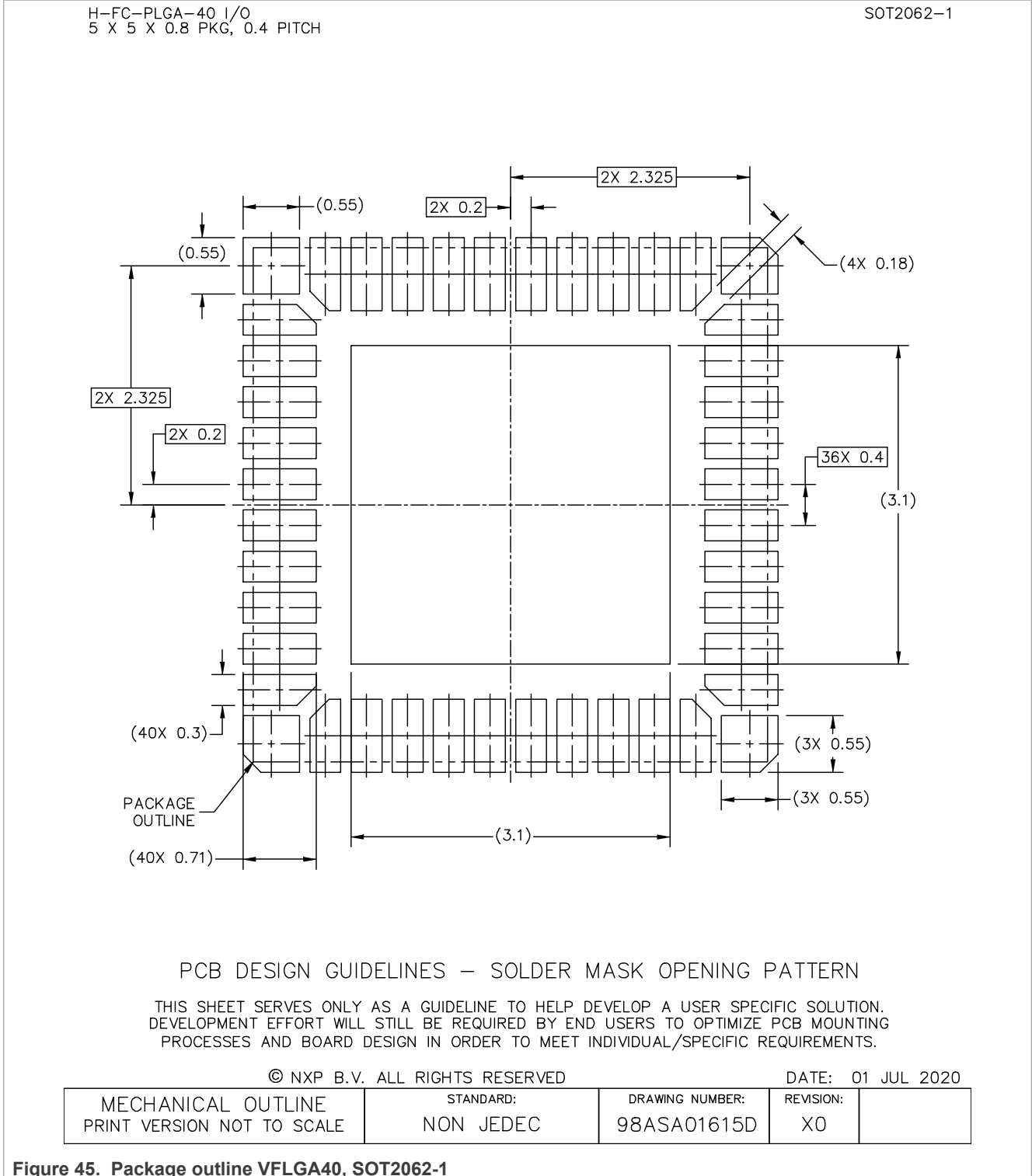
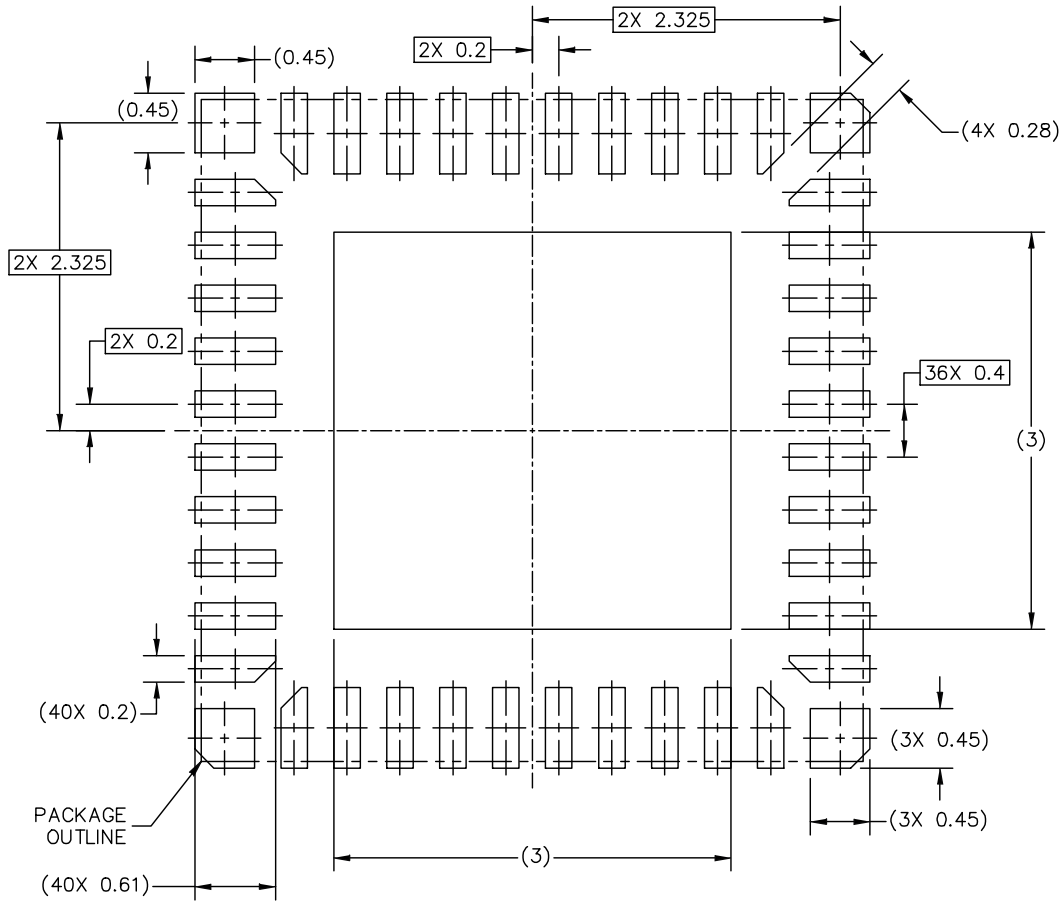


Figure 45. Package outline VFLGA40, SOT2062-1

H-FC-PLGA-40 I/O  
5 X 5 X 0.8 PKG, 0.4 PITCH

SOT2062-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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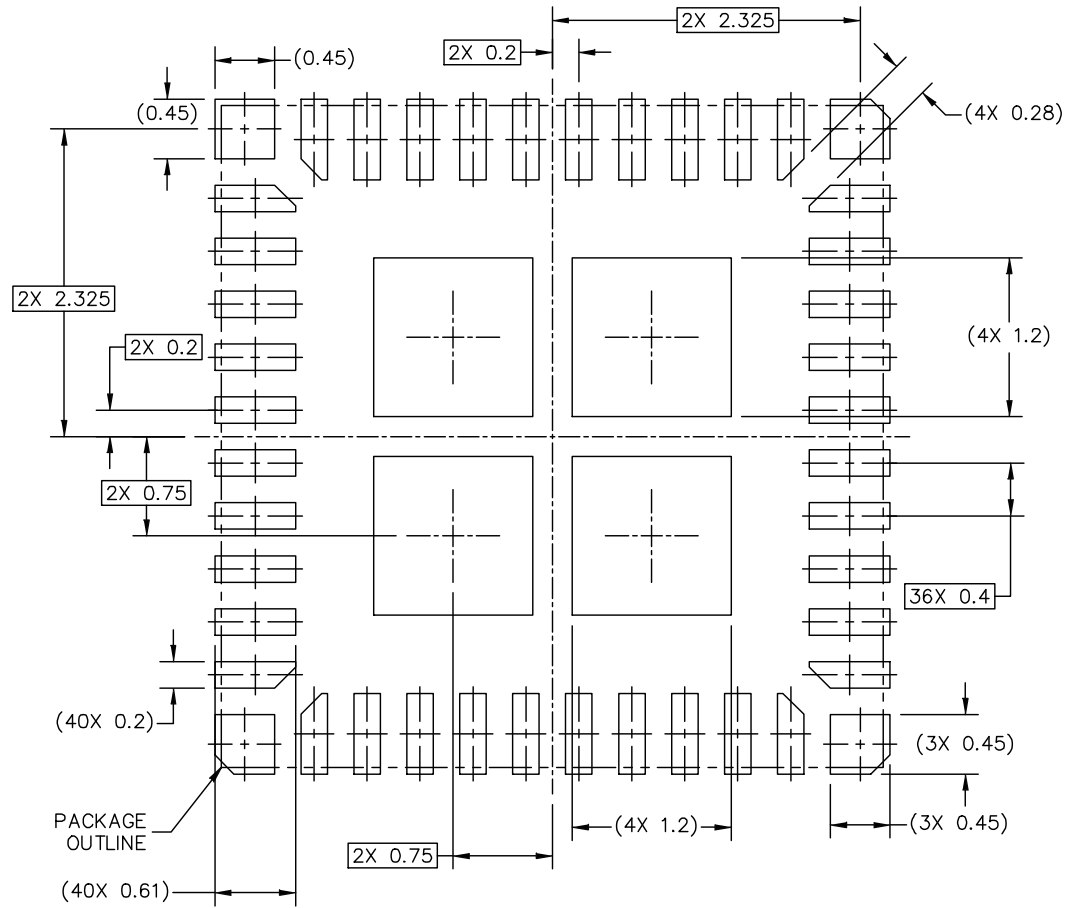
DATE: 01 JUL 2020

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| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON JEDEC | DRAWING NUMBER:<br>98ASA01615D | REVISION:<br>X0 |  |
|--|------------------------|--------------------------------|-----------------|--|

Figure 46. Package outline VFLGA40, SOT2062-1

H-FC-PLGA-40 I/O  
5 X 5 X 0.8 PKG, 0.4 PITCH

SOT2062-1



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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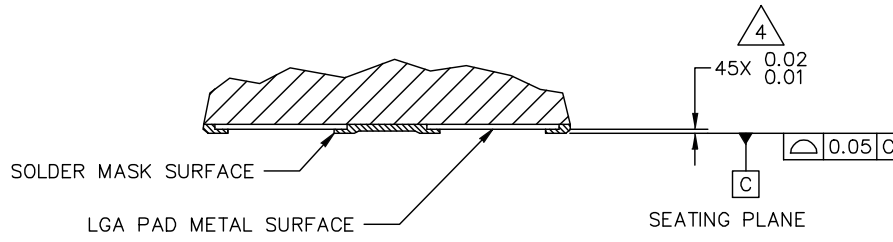
DATE: 01 JUL 2020

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|--|------------------------|--------------------------------|-----------------|--|

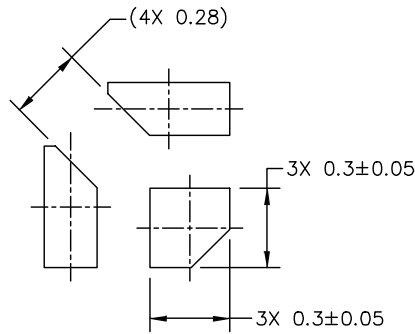
Figure 47. Package outline VFLGA40, SOT2062-1

H-FC-PLGA-40 I/O  
5 X 5 X 0.8 PKG, 0.4 PITCH

SOT2062-1



SECTION E-E



DETAIL F

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|  |                        |                                |                 |  |
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|--|------------------------|--------------------------------|-----------------|--|

Figure 48. Package outline VFLGA40, SOT2062-1

## 16 Surface mount reflow soldering

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For information on surface mount, reflow soldering and component handling please refer to the related application note.

This application note provides guidelines for the board mounting and handling of NXP Semiconductor packages:

<https://www.nxp.com/docs/en/application-note/AN10365.pdf>

## 17 Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*.

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow soldering, in order to remove any moisture that might have soaked into the package.

### For MSL3:

168h out-of-pack floor life at maximum ambient temperature, conditions < 30 °C / 60 % RH.

### For MSL2:

- 1 year out-of-pack floor life at maximum ambient temperature, conditions < 30 °C° / 60 % RH.

### For MSL1:

- No out-of-pack floor live spec. required. Conditions: <30 °C° / 85 % RH.

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.



## 18 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.00

```

Firmware 2.0
<?xml version="1.0" encoding="utf-8"?>
<EEPROM>
  <Region RegionName="USER_PMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PwrConfig" Offset="0x00" Value="0xE4" />
    <Parameter Name="DcdcConfig" Offset="0x01" Value="0x31" />
    <Parameter Name="TxLdoConfig" Offset="0x02" Value="0xFFFFAE7" />
    <Parameter Name="TxLdoVddpaHigh" Offset="0x06" Value="0x00" />
    <Parameter Name="TxLdoVddpaLow" Offset="0x07" Value="0x00" />
    <Parameter Name="TxLdoVddpaMaxRdr" Offset="0x08" Value="0x2A" />
    <Parameter Name="TxLdoVddpaMaxCard" Offset="0x09" Value="0x2A" />
    <Parameter Name="BoostDefaultVoltage" Offset="0x0A" Value="0x1D" />
  </Region>

  <Region RegionName="CLKGEN" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="XtalConfig" Offset="0x10" Value="0x00" />
    <Parameter Name="XtalTimeOut" Offset="0x11" Value="0xFF" />
  </Region>

  <Region RegionName="RF_CLOCK_CFG" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PLLClkInputFrq" Offset="0x12" Value="0x08" />
    <Parameter Name="XtalCheckDelay" Offset="0x13" Value="0xF6" />
  </Region>

  <Region RegionName="USER_SMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="TempWarning" Offset="0x14" Value="0x99" />
    <Parameter Name="EnableGpio0OnOverTemp" Offset="0x16" Value="0x01" />
  </Region>

  <Region RegionName="RM_TECHNO_TX_SHAPING" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="ResidualAmplitudeLevel_A106" Offset="0x22" Value="0x00" />
    <Parameter Name="EdgeType_A106" Offset="0x23" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A106" Offset="0x24" Value="0x64" />
    <Parameter Name="EdgeLength_A106" Offset="0x25" Value="0x10" />
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    <Parameter Name="EdgeLength_B212" Offset="0x39" Value="0x10" />
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    <Parameter Name="EdgeLength_F424" Offset="0x49" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_26" Offset="0x4A" Value="0x00" />
    <Parameter Name="EdgeType_V100_26" Offset="0x4B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_26" Offset="0x4C" Value="0x66" />
    <Parameter Name="EdgeLength_V100_26" Offset="0x4D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_53" Offset="0x4E" Value="0x00" />
    <Parameter Name="EdgeType_V100_53" Offset="0x4F" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_53" Offset="0x50" Value="0x66" />
    <Parameter Name="EdgeLength_V100_53" Offset="0x51" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_106" Offset="0x52" Value="0x00" />
    <Parameter Name="EdgeType_V100_106" Offset="0x53" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_106" Offset="0x54" Value="0x66" />
    <Parameter Name="EdgeLength_V100_106" Offset="0x55" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_212" Offset="0x56" Value="0x00" />
    <Parameter Name="EdgeType_V100_212" Offset="0x57" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_212" Offset="0x58" Value="0x22" />
    <Parameter Name="EdgeLength_V100_212" Offset="0x59" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V10_26" Offset="0x5A" Value="0xC0" />
    <Parameter Name="EdgeType_V10_26" Offset="0x5B" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_V10_26" Offset="0x5C" Value="0x66" />
    <Parameter Name="EdgeLength_V10_26" Offset="0x5D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V10_53" Offset="0x5E" Value="0xC0" />
    <Parameter Name="EdgeType_V10_53" Offset="0x5F" Value="0x22" />
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<Parameter Name="EdgeStyleConfiguration_V10_106" Offset="0x64" Value="0x23" />
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<Parameter Name="EdgeType_V10_212" Offset="0x67" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_212" Offset="0x68" Value="0x23" />
<Parameter Name="EdgeLength_V10_212" Offset="0x69" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_180003m3_tari18p88" Offset="0x6A" Value="0xC0" />
<Parameter Name="EdgeType_180003m3_tari18p88" Offset="0x6B" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_180003m3_tari18p88" Offset="0x6C" Value="0x66" />
<Parameter Name="EdgeLength_180003m3_tari18p88" Offset="0x6D" Value="0x10" />
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<Parameter Name="EdgeStyleConfiguration_180003m3_tari9p44" Offset="0x70" Value="0x66" />
<Parameter Name="EdgeLength_180003m3_tari9p44" Offset="0x71" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_B_prime106" Offset="0x72" Value="0xCF" />
<Parameter Name="EdgeType_B_prime106" Offset="0x73" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_B_prime106" Offset="0x74" Value="0x67" />
<Parameter Name="EdgeLength_B_prime106" Offset="0x75" Value="0x10" />
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<Parameter Name="Config" Offset="0x76" Value="0x77" />
<Parameter Name="TargetCurrent" Offset="0x77" Value="0x0132" />
<Parameter Name="Hysteresis" Offset="0x79" Value="0x14" />
<Parameter Name="Hysteresis Unloading" Offset="0x7C" Value="0x0A" />
<Parameter Name="TXLDVDDPA_Low" Offset="0x7D" Value="0x07" />
<Parameter Name="TXGSM" Offset="0x7E" Value="0x03" />
<Parameter Name="VDDPA_LowLimitControl" Offset="0x7F" Value="0x01" />
<Parameter Name="InitialRDOn_RFOn" Offset="0x80" Value="0x03" />
<Parameter Name="GuardTimeBeforeTx" Offset="0x87" Value="0x64" />
<Parameter Name="EnableDPCDuringFDT" Offset="0x88" Value="0x01" />
<Parameter Name="GuardTimeAfterRx" Offset="0x89" Value="0x01" />
<Parameter Name="Entry_00" Offset="0x8B" Value="0x0000137F" />
<Parameter Name="Entry_01" Offset="0x8F" Value="0x0000137F" />
<Parameter Name="Entry_02" Offset="0x93" Value="0x0000137F" />
<Parameter Name="Entry_03" Offset="0x97" Value="0x0000137F" />
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<Parameter Name="Entry_06" Offset="0xA3" Value="0x0000007F" />
<Parameter Name="Entry_07" Offset="0xA7" Value="0x0000007F" />
<Parameter Name="Entry_08" Offset="0xAB" Value="0x0000007F" />
<Parameter Name="Entry_09" Offset="0xAF" Value="0x0000007F" />
<Parameter Name="Entry_10" Offset="0xB3" Value="0x0000007F" />
<Parameter Name="Entry_11" Offset="0xB7" Value="0x0000007F" />
<Parameter Name="Entry_12" Offset="0xBB" Value="0x0000007F" />
<Parameter Name="Entry_13" Offset="0xBF" Value="0x0000007F" />
<Parameter Name="Entry_14" Offset="0xC3" Value="0x0000007F" />
<Parameter Name="Entry_15" Offset="0xC7" Value="0x0000007F" />
<Parameter Name="Entry_16" Offset="0xCB" Value="0x0000007F" />
<Parameter Name="Entry_17" Offset="0xCF" Value="0x0000007F" />
<Parameter Name="Entry_18" Offset="0xD3" Value="0x0000007F" />
<Parameter Name="Entry_19" Offset="0xD7" Value="0x0000007F" />
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<Parameter Name="Entry_21" Offset="0xDF" Value="0x0000007F" />
<Parameter Name="Entry_22" Offset="0xE3" Value="0x0000007F" />
<Parameter Name="Entry_23" Offset="0xE7" Value="0x0000007D" />
<Parameter Name="Entry_24" Offset="0xEB" Value="0x0000007B" />
<Parameter Name="Entry_25" Offset="0xEF" Value="0x00000079" />
<Parameter Name="Entry_26" Offset="0xF3" Value="0x00000077" />
<Parameter Name="Entry_27" Offset="0xF7" Value="0x00000075" />
<Parameter Name="Entry_28" Offset="0xFB" Value="0x00000073" />
<Parameter Name="Entry_29" Offset="0xFF" Value="0x00000071" />
<Parameter Name="Entry_30" Offset="0x103" Value="0x0000006F" />
<Parameter Name="Entry_31" Offset="0x107" Value="0x0000006E" />
<Parameter Name="Entry_32" Offset="0x10B" Value="0x0000006C" />
<Parameter Name="Entry_33" Offset="0x10F" Value="0x0000006A" />
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<Parameter Name="Entry_36" Offset="0x11B" Value="0x00000057" />
<Parameter Name="Entry_37" Offset="0x11F" Value="0x0000004B" />
<Parameter Name="Entry_38" Offset="0x123" Value="0x0000003F" />
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<Parameter Name="Entry_42" Offset="0x133" Value="0x00000000" />
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<Parameter Name="ArcConfig" Offset="0x137" Value="0x00E4" />
<Parameter Name="ArcVddpa" Offset="0x139" Value="0x2A24130E07" />
<Parameter Name="RmArcA_106" Offset="0x13E" Value="0x81348015802A8220C250" />
<Parameter Name="RmArcA_212" Offset="0x148" Value="0x001A00200030007F407F" />
<Parameter Name="RmArcA_424" Offset="0x152" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcA_848" Offset="0x15C" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcB_106" Offset="0x166" Value="0x001A0020003000404050" />
<Parameter Name="RmArcB_212" Offset="0x170" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_424" Offset="0x17A" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_848" Offset="0x184" Value="0x001A002000400050407F" />
<Parameter Name="RmArcF_212" Offset="0x18E" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcF_424" Offset="0x198" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcV_6p6" Offset="0x1A2" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArcV_26" Offset="0x1AC" Value="0x000A000A002F002F402E" />
<Parameter Name="RmArcV_53" Offset="0x1B6" Value="0x001A010A011F011F411F" />
<Parameter Name="RmArcV_106" Offset="0x1C0" Value="0x000A000A002F002F402E" />
<Parameter Name="RmArcV_212" Offset="0x1CA" Value="0x000A000A002F002F402E" />
<Parameter Name="RmArc180003m3_SC424_4Man" Offset="0x1D4" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC424_2Man" Offset="0x1DE" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc180003m3_SC848_4Man" Offset="0x1E8" Value="0x0114011F011F001F401F" />

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<Parameter Name="RmArc_AI_106" Offset="0x1FC" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_212" Offset="0x206" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_424" Offset="0x210" Value="0x000A000A000A000A400A" />
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  <Parameter Name="DPLL_INIT_Default" Offset="0x2A6" Value="0x002D1327" />
  <Parameter Name="DPLL_GEAR_Default" Offset="0x2AA" Value="0x04C1FEFE" />
  <Parameter Name="DPLL_CONTROL" Offset="0x2AE" Value="0x00000C03" />
</Region>

<Region RegionName="AUTOCOLL_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RfDebounceTimeout" Offset="0x2B2" Value="0x10" />
  <Parameter Name="SensRes" Offset="0x2B3" Value="0x0042" />
  <Parameter Name="NfcID1" Offset="0x2B5" Value="0xCCBBAA" />
  <Parameter Name="SelRes" Offset="0x2B8" Value="0x60" />
  <Parameter Name="PollRes" Offset="0x2B9" Value="0xFFD08584424B0B100814119814011401FE01" />
  <Parameter Name="RandomUIDEnable" Offset="0x2CB" Value="0x00" />
</Region>

<Region RegionName="MFC_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="MfcAuthTimeout" Offset="0x2CC" Value="0x0500" />
</Region>

<Region RegionName="AFC_RSSI" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RssiTimer" Offset="0x2DA" Value="0x0423" />
  <Parameter Name="RssiTimerFirstPeriod" Offset="0x2DC" Value="0x013D" />
  <Parameter Name="RssiCtrl_00_AB" Offset="0x2DE" Value="0x09" />
  <Parameter Name="RssiNbEntriesAB" Offset="0x2DF" Value="0x16" />
  <Parameter Name="RssiThresholdAB_01" Offset="0x2E0" Value="0x2816" />
  <Parameter Name="ArbPhaseAB_01" Offset="0x2E2" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_02" Offset="0x2E4" Value="0x3215" />
  <Parameter Name="ArbPhaseAB_02" Offset="0x2E6" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_03" Offset="0x2E8" Value="0x3B6E" />
  <Parameter Name="ArbPhaseAB_03" Offset="0x2EA" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_04" Offset="0x2EC" Value="0x456A" />
  <Parameter Name="ArbPhaseAB_04" Offset="0x2EE" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_05" Offset="0x2F0" Value="0x4FDC" />
  <Parameter Name="ArbPhaseAB_05" Offset="0x2F2" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_06" Offset="0x2F4" Value="0x5983" />
  <Parameter Name="ArbPhaseAB_06" Offset="0x2F6" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_07" Offset="0x2F8" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_07" Offset="0x2FA" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_08" Offset="0x2FC" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_08" Offset="0x2FE" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_09" Offset="0x300" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_0A" Offset="0x304" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_0C" Offset="0x30C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0C" Offset="0x30E" Value="0x0000" />
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  <Parameter Name="RssiThresholdAB_0E" Offset="0x314" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_14" Offset="0x32C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_14" Offset="0x32E" Value="0x0000" />
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  <Parameter Name="ArbPhaseAB_16" Offset="0x336" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_17" Offset="0x338" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_17" Offset="0x33A" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_18" Offset="0x33C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_18" Offset="0x33E" Value="0x0000" />
  <Parameter Name="RssiCtrl_00_F" Offset="0x340" Value="0x09" />
  <Parameter Name="RssiNbEntriesF" Offset="0x341" Value="0x16" />
  <Parameter Name="RssiThresholdF_01" Offset="0x342" Value="0x2816" />
  <Parameter Name="ArbPhaseF_01" Offset="0x344" Value="0x0000" />
  <Parameter Name="RssiThresholdF_02" Offset="0x346" Value="0x3215" />
  <Parameter Name="ArbPhaseF_02" Offset="0x348" Value="0x0000" />
  <Parameter Name="RssiThresholdF_03" Offset="0x34A" Value="0x3B6E" />
  <Parameter Name="ArbPhaseF_03" Offset="0x34C" Value="0x0000" />
  <Parameter Name="RssiThresholdF_04" Offset="0x34E" Value="0x456A" />
  <Parameter Name="ArbPhaseF_04" Offset="0x350" Value="0x0000" />
  <Parameter Name="RssiThresholdF_05" Offset="0x352" Value="0x4FDC" />
  <Parameter Name="ArbPhaseF_05" Offset="0x354" Value="0x0000" />
  <Parameter Name="RssiThresholdF_06" Offset="0x356" Value="0x5983" />
  <Parameter Name="ArbPhaseF_06" Offset="0x358" Value="0x0000" />
  <Parameter Name="RssiThresholdF_07" Offset="0x35A" Value="0x96F9" />
  <Parameter Name="ArbPhaseF_07" Offset="0x35C" Value="0x0000" />
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  <Parameter Name="RssiThresholdF_09" Offset="0x362" Value="0x96F9" />
  <Parameter Name="ArbPhaseF_09" Offset="0x364" Value="0x0000" />
  <Parameter Name="RssiThresholdF_0A" Offset="0x366" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_0D" Offset="0x372" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_0E" Offset="0x376" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_0F" Offset="0x37A" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_13" Offset="0x38A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_13" Offset="0x38C" Value="0x0000" />
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<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
<Parameter Name="RssiThresholdF_15" Offset="0x392" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
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<Parameter Name="TxParamEntry_00_Tx1" Offset="0x3A3" Value="0x00" />
<Parameter Name="TxParamEntry_00_Tx2" Offset="0x3A4" Value="0x64" />
<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
<Parameter Name="TxParamEntry_04_ID" Offset="0x3AE" Value="0x44" />
<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
<Parameter Name="TxParamEntry_05_ID" Offset="0x3B1" Value="0x45" />
<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
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<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
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<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
<Parameter Name="TxParamEntry_08_ID" Offset="0x3BA" Value="0x48" />
<Parameter Name="TxParamEntry_08_Tx1" Offset="0x3BB" Value="0x00" />
<Parameter Name="TxParamEntry_08_Tx2" Offset="0x3BC" Value="0x64" />
<Parameter Name="TxParamEntry_09_ID" Offset="0x3BD" Value="0x49" />
<Parameter Name="TxParamEntry_09_Tx1" Offset="0x3BE" Value="0x00" />
<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
<Parameter Name="TxParamEntry_0A_ID" Offset="0x3C0" Value="0x4A" />
<Parameter Name="TxParamEntry_0A_Tx1" Offset="0x3C1" Value="0x00" />
<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x64" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
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<Parameter Name="TxParamEntry_0C_ID" Offset="0x3C6" Value="0x4C" />
<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
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<Parameter Name="TxParamEntry_0D_Tx1" Offset="0x3CA" Value="0x00" />
<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x64" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x64" />
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<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
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<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
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<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
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<Parameter Name="TxParamEntry_49_ID" Offset="0x47D" Value="0x7F" />
<Parameter Name="TxParamEntry_49_Tx1" Offset="0x47E" Value="0x00" />
<Parameter Name="TxParamEntry_49_Tx2" Offset="0x47F" Value="0x37" />
<Parameter Name="TxParamEntry_4A_ID" Offset="0x480" Value="0x7E" />
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<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7E" />
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<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
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<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7E" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
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<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
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<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
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<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
</Region>

<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_ivl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
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<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x000FFFFFF" />
</Region>

<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
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<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RXIRQ_GuardTime" Offset="0x561" Value="0x000F4240" />
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<Region RegionName="TX_SHAPING_PROPRIETARY_CORR" RegionAccess="RW" RegionType="DATA">

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<Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
<Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
<Parameter Name="Correction_Entry39" Offset="0xBF9" Value="0x0000" />
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  <Parameter Name="RTRANS0" Offset="0xC03" Value="0x0DFD9D3CD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xF1EEEEBE5" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0x0FDFAF7F4" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xE7EDF3F9" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xD4D8DBE1" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xC8CACDD1" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xC7C7C7C7" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0x0FAF9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0x0FEFDFDFC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0x0FEFDFDFC" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0x0FCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0x0F4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
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<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>
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  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
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<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfIgNovCal" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
  <Parameter Name="CfIgThreshold" Offset="0xC86" Value="0x08" />
  <Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
  <Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
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<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="EnableFastVDDPDischarge" Offset="0xC8F" Value="0x00" />
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<Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x00000003"></Register>
<Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x20060200"></Register>
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<Protocol ProtocolName="RX_GTM_All" ProtocolIndex="0x9C" ProtocolOffset="0x1226">
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<Register RegisterName="CLIF_DCOC_CONFIG" RegisterLogicalAddress="0x33" RegisterValue="0x00100032"></Register>
<Register RegisterName="CLIF_RXM_CTRL" RegisterLogicalAddress="0x35" RegisterValue="0x0004C935"></Register>
<Register RegisterName="CLIF_GCM_CONFIG2" RegisterLogicalAddress="0x38" RegisterValue="0x00A24820"></Register>
<Register RegisterName="CLIF_GCM_CONFIG1" RegisterLogicalAddress="0x39" RegisterValue="0x4000003F"></Register>
<Register RegisterName="CLIF_GCM_CONFIG0" RegisterLogicalAddress="0x3A" RegisterValue="0x00A93979"></Register>
<Register RegisterName="CLIF_ANA_AGC_DCO_CTRL" RegisterLogicalAddress="0x36" RegisterValue="0x00000000"></Register>
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<Register RegisterName="CLIF_RX_EMD_0_CONFIG" RegisterLogicalAddress="0x48" RegisterValue="0x00280200"></Register>
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<Register RegisterName="CLIF_DCOC_CONFIG" RegisterLogicalAddress="0x33" RegisterValue="0x000000F4"></Register>
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<Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x1FE00001"></Register>
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19 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.01

Firmware 2.1

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<?xml version="1.0" encoding="utf-8"?>
<EEPROM>
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<Parameter Name="RssiThresholdF_14" Offset="0x38E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
<Parameter Name="RssiThresholdF_15" Offset="0x392" Value="0x96F9" />
<Parameter Name="ArbPhaseF_15" Offset="0x394" Value="0x0000" />
<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
<Parameter Name="ArbPhaseF_16" Offset="0x398" Value="0x0000" />
<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
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<Region RegionName="APC_TX" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TxParamEntry_00_ID" Offset="0x3A2" Value="0x40" />
<Parameter Name="TxParamEntry_00_Tx1" Offset="0x3A3" Value="0x00" />
<Parameter Name="TxParamEntry_00_Tx2" Offset="0x3A4" Value="0x64" />
<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
<Parameter Name="TxParamEntry_04_ID" Offset="0x3AE" Value="0x44" />
<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
<Parameter Name="TxParamEntry_05_ID" Offset="0x3B1" Value="0x45" />
<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
<Parameter Name="TxParamEntry_06_Tx1" Offset="0x3B5" Value="0x00" />
<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
<Parameter Name="TxParamEntry_07_ID" Offset="0x3B7" Value="0x47" />
<Parameter Name="TxParamEntry_07_Tx1" Offset="0x3B8" Value="0x00" />
<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
<Parameter Name="TxParamEntry_08_ID" Offset="0x3BA" Value="0x48" />
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<Parameter Name="TxParamEntry_08_Tx2" Offset="0x3BC" Value="0x64" />
<Parameter Name="TxParamEntry_09_ID" Offset="0x3BD" Value="0x49" />
<Parameter Name="TxParamEntry_09_Tx1" Offset="0x3BE" Value="0x00" />
<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
<Parameter Name="TxParamEntry_0A_ID" Offset="0x3C0" Value="0x4A" />
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<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x64" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
<Parameter Name="TxParamEntry_0B_Tx2" Offset="0x3C5" Value="0x64" />
<Parameter Name="TxParamEntry_0C_ID" Offset="0x3C6" Value="0x4C" />
<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
<Parameter Name="TxParamEntry_00C_Tx2" Offset="0x3C8" Value="0x4F" />
<Parameter Name="TxParamEntry_0D_ID" Offset="0x3C9" Value="0x4D" />
<Parameter Name="TxParamEntry_0D_Tx1" Offset="0x3CA" Value="0x00" />
<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x47" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x3F" />
<Parameter Name="TxParamEntry_0F_ID" Offset="0x3CF" Value="0x4F" />
<Parameter Name="TxParamEntry_0F_Tx1" Offset="0x3D0" Value="0x00" />
<Parameter Name="TxParamEntry_0F_Tx2" Offset="0x3D1" Value="0x37" />
<Parameter Name="TxParamEntry_10_ID" Offset="0x3D2" Value="0x50" />
<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
<Parameter Name="TxParamEntry_10_Tx2" Offset="0x3D4" Value="0x37" />
<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
<Parameter Name="TxParamEntry_11_Tx1" Offset="0x3D6" Value="0x00" />
<Parameter Name="TxParamEntry_11_Tx2" Offset="0x3D7" Value="0x37" />
<Parameter Name="TxParamEntry_12_ID" Offset="0x3D8" Value="0x52" />
<Parameter Name="TxParamEntry_12_Tx1" Offset="0x3D9" Value="0x00" />
<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x37" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
<Parameter Name="TxParamEntry_13_Tx1" Offset="0x3DC" Value="0x00" />
<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x37" />
<Parameter Name="TxParamEntry_14_ID" Offset="0x3DE" Value="0x54" />
<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
<Parameter Name="TxParamEntry_14_Tx2" Offset="0x3E0" Value="0x37" />
<Parameter Name="TxParamEntry_15_ID" Offset="0x3E1" Value="0x55" />
<Parameter Name="TxParamEntry_15_Tx1" Offset="0x3E2" Value="0x00" />
<Parameter Name="TxParamEntry_15_Tx2" Offset="0x3E3" Value="0x37" />
<Parameter Name="TxParamEntry_16_ID" Offset="0x3E4" Value="0x56" />
<Parameter Name="TxParamEntry_16_Tx1" Offset="0x3E5" Value="0x00" />
<Parameter Name="TxParamEntry_16_Tx2" Offset="0x3E6" Value="0x37" />
<Parameter Name="TxParamEntry_17_ID" Offset="0x3E7" Value="0x57" />
<Parameter Name="TxParamEntry_17_Tx1" Offset="0x3E8" Value="0x00" />
<Parameter Name="TxParamEntry_17_Tx2" Offset="0x3E9" Value="0x37" />
<Parameter Name="TxParamEntry_18_ID" Offset="0x3EA" Value="0x58" />
<Parameter Name="TxParamEntry_18_Tx1" Offset="0x3EB" Value="0x00" />
<Parameter Name="TxParamEntry_18_Tx2" Offset="0x3EC" Value="0x37" />
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<Parameter Name="TxParamEntry_3B_ID" Offset="0x453" Value="0x7B" />
<Parameter Name="TxParamEntry_3B_Tx1" Offset="0x454" Value="0x00" />
<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
<Parameter Name="TxParamEntry_3C_ID" Offset="0x456" Value="0x7C" />
<Parameter Name="TxParamEntry_3C_Tx1" Offset="0x457" Value="0x00" />
<Parameter Name="TxParamEntry_3C_Tx2" Offset="0x458" Value="0x37" />
<Parameter Name="TxParamEntry_3D_ID" Offset="0x459" Value="0x7D" />
<Parameter Name="TxParamEntry_3D_Tx1" Offset="0x45A" Value="0x00" />
<Parameter Name="TxParamEntry_3D_Tx2" Offset="0x45B" Value="0x37" />
<Parameter Name="TxParamEntry_3E_ID" Offset="0x45C" Value="0x7E" />
<Parameter Name="TxParamEntry_3E_Tx1" Offset="0x45D" Value="0x00" />
<Parameter Name="TxParamEntry_3E_Tx2" Offset="0x45E" Value="0x37" />
<Parameter Name="TxParamEntry_3F_ID" Offset="0x45F" Value="0x7F" />
<Parameter Name="TxParamEntry_3F_Tx1" Offset="0x460" Value="0x00" />
<Parameter Name="TxParamEntry_3F_Tx2" Offset="0x461" Value="0x37" />
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<Parameter Name="TxParamEntry_40_Tx1" Offset="0x463" Value="0x00" />
<Parameter Name="TxParamEntry_40_Tx2" Offset="0x464" Value="0x37" />
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<Parameter Name="TxParamEntry_41_Tx1" Offset="0x466" Value="0x00" />
<Parameter Name="TxParamEntry_41_Tx2" Offset="0x467" Value="0x37" />
<Parameter Name="TxParamEntry_42_ID" Offset="0x468" Value="0x7F" />
<Parameter Name="TxParamEntry_42_Tx1" Offset="0x469" Value="0x00" />
<Parameter Name="TxParamEntry_42_Tx2" Offset="0x46A" Value="0x37" />
<Parameter Name="TxParamEntry_43_ID" Offset="0x46B" Value="0x7F" />
<Parameter Name="TxParamEntry_43_Tx1" Offset="0x46C" Value="0x00" />
<Parameter Name="TxParamEntry_43_Tx2" Offset="0x46D" Value="0x37" />
<Parameter Name="TxParamEntry_44_ID" Offset="0x46E" Value="0x7F" />
<Parameter Name="TxParamEntry_44_Tx1" Offset="0x46F" Value="0x00" />
<Parameter Name="TxParamEntry_44_Tx2" Offset="0x470" Value="0x37" />
<Parameter Name="TxParamEntry_45_ID" Offset="0x471" Value="0x7F" />
<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
<Parameter Name="TxParamEntry_45_Tx2" Offset="0x473" Value="0x37" />
<Parameter Name="TxParamEntry_46_ID" Offset="0x474" Value="0x7F" />
<Parameter Name="TxParamEntry_46_Tx1" Offset="0x475" Value="0x00" />
<Parameter Name="TxParamEntry_46_Tx2" Offset="0x476" Value="0x37" />
<Parameter Name="TxParamEntry_47_ID" Offset="0x477" Value="0x7F" />
<Parameter Name="TxParamEntry_47_Tx1" Offset="0x478" Value="0x00" />
<Parameter Name="TxParamEntry_47_Tx2" Offset="0x479" Value="0x37" />
<Parameter Name="TxParamEntry_48_ID" Offset="0x47A" Value="0x7F" />
<Parameter Name="TxParamEntry_48_Tx1" Offset="0x47B" Value="0x00" />
<Parameter Name="TxParamEntry_48_Tx2" Offset="0x47C" Value="0x37" />
<Parameter Name="TxParamEntry_49_ID" Offset="0x47D" Value="0x7F" />
<Parameter Name="TxParamEntry_49_Tx1" Offset="0x47E" Value="0x00" />
<Parameter Name="TxParamEntry_49_Tx2" Offset="0x47F" Value="0x37" />
<Parameter Name="TxParamEntry_4A_ID" Offset="0x480" Value="0x7F" />
<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
<Parameter Name="TxParamEntry_4B_ID" Offset="0x483" Value="0x7F" />
<Parameter Name="TxParamEntry_4B_Tx1" Offset="0x484" Value="0x00" />
<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7F" />
<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7F" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
<Parameter Name="dummy" Offset="0x48F" Value="0x000000" />
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<Region RegionName="LPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x01F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
</Region>

<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
</Region>

<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
</Region>

<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x000FFFFF" />
</Region>

<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
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<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RXIRQ_GuardTime" Offset="0x561" Value="0x000F4240" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY CORR" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Correction_Entry0" Offset="0xBAD" Value="0x0000" />
<Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
<Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />

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<Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
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<Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
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<Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
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<Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
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<Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
<Parameter Name="Correction_Entry17" Offset="0xBCE" Value="0x0000" />
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<Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
<Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
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<Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
<Parameter Name="Correction_Entry25" Offset="0xBDF" Value="0x0000" />
<Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
<Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
<Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
<Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
<Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
<Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
<Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
<Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
<Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
<Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
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<Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
<Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
<Parameter Name="Correction_Entry39" Offset="0xBF" Value="0x0000" />
<Parameter Name="Correction_Entry40" Offset="0xBFD" Value="0x0000" />
<Parameter Name="Correction_Entry41" Offset="0xBFF" Value="0x0000" />
<Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
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<Region RegionName="TX_SHAPING_PROPRIETARY_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xEAE6DCCD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xFAF6F2EE" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFFFFFFFF" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xCACACACA" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xCACACAD8" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xCACACACA" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xCACACACA" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xFAF9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFDFFDC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>
<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfNovCal1" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
  <Parameter Name="CfThreshold" Offset="0xC86" Value="0x08" />
  <Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
  <Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
</Region>
<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="EnableFastVDDPDischarge" Offset="0xC8F" Value="0x00" />
</Region>
<Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RmArca_106_FDT" Offset="0xC9D" Value="0x812A805080508050C050" />
</Region>
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<Protocol ProtocolName="RX GTM All" ProtocolIndex="0x9C" ProtocolOffset="0x1226">
  <Register RegisterName="CLIF_ANA_RX_CTRL" RegisterLogicalAddress="0x43" RegisterValue="0x0700E437"></Register>
  <Register RegisterName="CLIF_DCOC_CONFIG" RegisterLogicalAddress="0x33" RegisterValue="0x00100032"></Register>
  <Register RegisterName="CLIF_RXM_CTRL" RegisterLogicalAddress="0x35" RegisterValue="0x0004C935"></Register>
  <Register RegisterName="CLIF_GCM_CONFIG2" RegisterLogicalAddress="0x38" RegisterValue="0x00A24820"></Register>
  <Register RegisterName="CLIF_GCM_CONFIG1" RegisterLogicalAddress="0x39" RegisterValue="0x4000003F"></Register>
  <Register RegisterName="CLIF_GCM_CONFIG0" RegisterLogicalAddress="0x3A" RegisterValue="0x00A93979"></Register>
  <Register RegisterName="CLIF_ANA_AGC_DCO_CTRL" RegisterLogicalAddress="0x36" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_CONFIG" RegisterLogicalAddress="0x1F" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_ENABLES" RegisterLogicalAddress="0x21" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_CONFIG" RegisterLogicalAddress="0x1D" RegisterValue="0x00600081"></Register>
  <Register RegisterName="CLIF_SIGPRO_NOISE_CONFIG1" RegisterLogicalAddress="0x23" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_NOISE_CONFIG2" RegisterLogicalAddress="0x24" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_RX_ERROR_CONFIG" RegisterLogicalAddress="0x27" RegisterValue="0x000037FF"></Register>
  <Register RegisterName="CLIF_RX_EMD_0_CONFIG" RegisterLogicalAddress="0x48" RegisterValue="0x00280200"></Register>
  <Register RegisterName="CLIF_SIGPRO_IIR_CONFIG1" RegisterLogicalAddress="0x29" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_IIR_CONFIG0" RegisterLogicalAddress="0x2A" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_DAC_FILTER" RegisterLogicalAddress="0x2B" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_CONFIG" RegisterLogicalAddress="0x2C" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_BBA" RegisterLogicalAddress="0x2D" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_DCO" RegisterLogicalAddress="0x2E" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_HF_ATT" RegisterLogicalAddress="0x2F" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_DGRM_RSSI" RegisterLogicalAddress="0x30" RegisterValue="0x00000000"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x00000003"></Register>
  <Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x0BF9600A"></Register>
</Protocol>
<Protocol ProtocolName="RX B Prime All" ProtocolIndex="0x9D" ProtocolOffset="0x129E">
  <Register RegisterName="CLIF_ANA_RX_CTRL" RegisterLogicalAddress="0x43" RegisterValue="0x0000E407"></Register>
  <Register RegisterName="CLIF_DCOC_CONFIG" RegisterLogicalAddress="0x33" RegisterValue="0x000000F4"></Register>
  <Register RegisterName="CLIF_RXM_CTRL" RegisterLogicalAddress="0x35" RegisterValue="0x0044893E"></Register>
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  <Register RegisterName="CLIF_GCM_CONFIG1" RegisterLogicalAddress="0x39" RegisterValue="0x000000FC"></Register>
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  <Register RegisterName="CLIF_ANA_AGC_DCO_CTRL" RegisterLogicalAddress="0x36" RegisterValue="0x01000008"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_CONFIG" RegisterLogicalAddress="0x1F" RegisterValue="0x02380248"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_ENABLES" RegisterLogicalAddress="0x21" RegisterValue="0x00000055"></Register>
  <Register RegisterName="CLIF_SIGPRO_CONFIG" RegisterLogicalAddress="0x1D" RegisterValue="0x400000BE"></Register>
  <Register RegisterName="CLIF_SIGPRO_NOISE_CONFIG1" RegisterLogicalAddress="0x23" RegisterValue="0x0C082155"></Register>
  <Register RegisterName="CLIF_SIGPRO_NOISE_CONFIG2" RegisterLogicalAddress="0x24" RegisterValue="0x00085510"></Register>
  <Register RegisterName="CLIF_RX_ERROR_CONFIG" RegisterLogicalAddress="0x27" RegisterValue="0x000037FF"></Register>
  <Register RegisterName="CLIF_RX_EMD_0_CONFIG" RegisterLogicalAddress="0x48" RegisterValue="0x1F200000"></Register>
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  <Register RegisterName="CLIF_SIGPRO_IIR_CONFIG0" RegisterLogicalAddress="0x2A" RegisterValue="0x000A85CC"></Register>
  <Register RegisterName="CLIF_DGRM_DAC_FILTER" RegisterLogicalAddress="0x2B" RegisterValue="0x00889238"></Register>
  <Register RegisterName="CLIF_DGRM_CONFIG" RegisterLogicalAddress="0x2C" RegisterValue="0x00E63400"></Register>
  <Register RegisterName="CLIF_DGRM_BBA" RegisterLogicalAddress="0x2D" RegisterValue="0xED4C64A4"></Register>
  <Register RegisterName="CLIF_DGRM_DCO" RegisterLogicalAddress="0x2E" RegisterValue="0xC0F7C1F0"></Register>
  <Register RegisterName="CLIF_DGRM_HF_ATT" RegisterLogicalAddress="0x2F" RegisterValue="0x2A8FFFFF"></Register>
  <Register RegisterName="CLIF_DGRM_RSSI" RegisterLogicalAddress="0x30" RegisterValue="0x393F518A"></Register>
  <Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x95086250"></Register>
  <Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x1FE00001"></Register>
</Protocol>
</Region>
</EEPROM>
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20 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.03

Firmware 2.3

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    <Parameter Name="DcdcConfig" Offset="0x01" Value="0x31" />
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    <Parameter Name="TxLdoVddpaHigh" Offset="0x06" Value="0x00" />
    <Parameter Name="TxLdoVddpaLow" Offset="0x07" Value="0x00" />
    <Parameter Name="TxLdoVddpaMaxRdr" Offset="0x08" Value="0x2A" />
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    <Parameter Name="BoostDefaultVoltage" Offset="0x0A" Value="0x1D" />
  </Region>

  <Region RegionName="CLKGEN" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="XtalConfig" Offset="0x10" Value="0x00" />
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  </Region>

  <Region RegionName="RF_CLOCK_CFG" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PLLClkInputFrq" Offset="0x12" Value="0x08" />
    <Parameter Name="XtalCheckDelay" Offset="0x13" Value="0xF6" />
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  <Region RegionName="USER_SMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="TempWarning" Offset="0x14" Value="0x99" />
    <Parameter Name="EnableGpio0OnOverTemp" Offset="0x16" Value="0x01" />
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  <Region RegionName="RM_TECHNO_TX_SHAPING" RegionAccess="RW" RegionType="DATA">
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    <Parameter Name="EdgeStyleConfiguration_A848" Offset="0x30" Value="0x18" />
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    <Parameter Name="ResidualAmplitudeLevel_B106" Offset="0x32" Value="0xCA" />
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    <Parameter Name="EdgeStyleConfiguration_V100_106" Offset="0x54" Value="0x66" />
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    <Parameter Name="EdgeStyleConfiguration_V10_26" Offset="0x5C" Value="0x66" />
    <Parameter Name="EdgeLength_V10_26" Offset="0x5D" Value="0x10" />
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<Parameter Name="DPC_HYSTERESIS_LOADING" Offset="0x79" Value="0x14" />
<Parameter Name="DPC_HYSTERESIS_UNLOADING" Offset="0x7C" Value="0x0A" />
<Parameter Name="DPC_TXLDOVDDPAlow" Offset="0x7D" Value="0x07" />
<Parameter Name="DPC_TXGSN" offset="0x7E" Value="0x03" />
<Parameter Name="DPC_RDON_Control" Offset="0x7F" Value="0x01" />
<Parameter Name="DPC_InitialRDON_RFOh" Offset="0x80" Value="0x03" />
<Parameter Name="DPC_GAURD_TIME" Offset="0x87" Value="0x64" />
<Parameter Name="DPC_ENABLE_DURING_FDT" Offset="0x88" Value="0x01" />
<Parameter Name="DPC_GAURD_TIME_AFTER_RX" Offset="0x89" Value="0x01" />
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<Parameter Name="ArcConfig" Offset="0x137" Value="0x00E4" />
<Parameter Name="ArcVddpa" Offset="0x139" Value="0x2A24130E07" />
<Parameter Name="RmArcA_106" Offset="0x13E" Value="0x81348015802A8220C250" />
<Parameter Name="RmArcA_212" Offset="0x148" Value="0x001A00200030007F407F" />
<Parameter Name="RmArcA_424" Offset="0x152" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcA_848" Offset="0x15C" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcB_106" Offset="0x166" Value="0x001A0020003000404050" />
<Parameter Name="RmArcB_212" Offset="0x170" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_424" Offset="0x17A" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_848" Offset="0x184" Value="0x001A002000400050407F" />
<Parameter Name="RmArcF_212" Offset="0x18E" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcF_424" Offset="0x198" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcV_6p6" Offset="0x1A2" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArcV_26" Offset="0x1AC" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_53" Offset="0x1B6" Value="0x001A010A011F011F411F" />
<Parameter Name="RmArcV_106" Offset="0x1C0" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_212" Offset="0x1CA" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArc180003m3_SC424_4Man" Offset="0x1D4" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC424_2Man" Offset="0x1DE" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc180003m3_SC848_4Man" Offset="0x1E8" Value="0x0114011F011F001F401F" />

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<Parameter Name="RmArc_AI_106" Offset="0x1FC" Value="0x000A000A000A000A400A" />
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  <Parameter Name="DPLL_CONTROL" Offset="0x2AE" Value="0x00000C03" />
</Region>

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  <Parameter Name="SensRes" Offset="0x2B3" Value="0x0042" />
  <Parameter Name="NfcID1" Offset="0x2B5" Value="0xCCBBAA" />
  <Parameter Name="SelRes" Offset="0x2B8" Value="0x60" />
  <Parameter Name="PollRes" Offset="0x2B9" Value="0xFFD08584424B0B100814119814011401FE01" />
  <Parameter Name="RandomUIDEnable" Offset="0x2CB" Value="0x00" />
</Region>

<Region RegionName="MFC_CFG" RegionAccess="RW" RegionType="DATA">
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</Region>

<Region RegionName="APC_RSSI" RegionAccess="RW" RegionType="DATA">
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  <Parameter Name="RssiCtrl_00_AB" Offset="0x2DE" Value="0x09" />
  <Parameter Name="RssiNbEntriesAB" Offset="0x2DF" Value="0x16" />
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  <Parameter Name="ArbPhaseAB_02" Offset="0x2E6" Value="0x0000" />
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  <Parameter Name="ArbPhaseAB_04" Offset="0x2EE" Value="0x0000" />
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  <Parameter Name="ArbPhaseAB_11" Offset="0x322" Value="0x0000" />
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  <Parameter Name="ArbPhaseAB_13" Offset="0x32A" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_14" Offset="0x32C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_14" Offset="0x32E" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_15" Offset="0x330" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_15" Offset="0x332" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_16" Offset="0x334" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_16" Offset="0x336" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_17" Offset="0x338" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_17" Offset="0x33A" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_18" Offset="0x33C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_18" Offset="0x33E" Value="0x0000" />
  <Parameter Name="RssiCtrl_00_F" Offset="0x340" Value="0x09" />
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  <Parameter Name="RssiThresholdF_01" Offset="0x342" Value="0x2816" />
  <Parameter Name="ArbPhaseF_01" Offset="0x344" Value="0x0000" />
  <Parameter Name="RssiThresholdF_02" Offset="0x346" Value="0x3215" />
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  <Parameter Name="RssiThresholdF_06" Offset="0x356" Value="0x5983" />
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  <Parameter Name="ArbPhaseF_07" Offset="0x35C" Value="0x0000" />
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<Parameter Name="ArbPhaseF_0B" Offset="0x36C" Value="0x0000" />
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<Parameter Name="ArbPhaseF_0C" Offset="0x370" Value="0x0000" />
<Parameter Name="RssiThresholdF_0D" Offset="0x372" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0D" Offset="0x374" Value="0x0000" />
<Parameter Name="RssiThresholdF_0E" Offset="0x376" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0E" Offset="0x378" Value="0x0000" />
<Parameter Name="RssiThresholdF_0F" Offset="0x37A" Value="0x96F9" />
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<Parameter Name="RssiThresholdF_13" Offset="0x38A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_13" Offset="0x38C" Value="0x0000" />
<Parameter Name="RssiThresholdF_14" Offset="0x38E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
<Parameter Name="RssiThresholdF_15" Offset="0x392" Value="0x96F9" />
<Parameter Name="ArbPhaseF_15" Offset="0x394" Value="0x0000" />
<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
<Parameter Name="ArbPhaseF_16" Offset="0x398" Value="0x0000" />
<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
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<Region RegionName="APC_TX" RegionAccess="RW" RegionType="DATA">
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<Parameter Name="TxParamEntry_00_Tx1" Offset="0x3A3" Value="0x00" />
<Parameter Name="TxParamEntry_00_Tx2" Offset="0x3A4" Value="0x64" />
<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
<Parameter Name="TxParamEntry_04_ID" Offset="0x3AE" Value="0x44" />
<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
<Parameter Name="TxParamEntry_05_ID" Offset="0x3B1" Value="0x45" />
<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
<Parameter Name="TxParamEntry_06_Tx1" Offset="0x3B5" Value="0x00" />
<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
<Parameter Name="TxParamEntry_07_ID" Offset="0x3B7" Value="0x47" />
<Parameter Name="TxParamEntry_07_Tx1" Offset="0x3B8" Value="0x00" />
<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
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<Parameter Name="TxParamEntry_08_Tx1" Offset="0x3BB" Value="0x00" />
<Parameter Name="TxParamEntry_08_Tx2" Offset="0x3BC" Value="0x64" />
<Parameter Name="TxParamEntry_09_ID" Offset="0x3BD" Value="0x49" />
<Parameter Name="TxParamEntry_09_Tx1" Offset="0x3BE" Value="0x00" />
<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
<Parameter Name="TxParamEntry_0A_ID" Offset="0x3C0" Value="0x4A" />
<Parameter Name="TxParamEntry_0A_Tx1" Offset="0x3C1" Value="0x00" />
<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x64" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
<Parameter Name="TxParamEntry_0B_Tx2" Offset="0x3C5" Value="0x64" />
<Parameter Name="TxParamEntry_0C_ID" Offset="0x3C6" Value="0x4C" />
<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
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<Parameter Name="TxParamEntry_0D_Tx1" Offset="0x3CA" Value="0x00" />
<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x64" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x64" />
<Parameter Name="TxParamEntry_0F_ID" Offset="0x3CF" Value="0x4F" />
<Parameter Name="TxParamEntry_0F_Tx1" Offset="0x3D0" Value="0x00" />
<Parameter Name="TxParamEntry_0F_Tx2" Offset="0x3D1" Value="0x64" />
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<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
<Parameter Name="TxParamEntry_10_Tx2" Offset="0x3D4" Value="0x64" />
<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
<Parameter Name="TxParamEntry_11_Tx1" Offset="0x3D6" Value="0x00" />
<Parameter Name="TxParamEntry_11_Tx2" Offset="0x3D7" Value="0x64" />
<Parameter Name="TxParamEntry_12_ID" Offset="0x3D8" Value="0x52" />
<Parameter Name="TxParamEntry_12_Tx1" Offset="0x3D9" Value="0x00" />
<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x64" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
<Parameter Name="TxParamEntry_13_Tx1" Offset="0x3DC" Value="0x00" />
<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x64" />
<Parameter Name="TxParamEntry_14_ID" Offset="0x3DE" Value="0x54" />
<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
<Parameter Name="TxParamEntry_14_Tx2" Offset="0x3E0" Value="0x64" />
<Parameter Name="TxParamEntry_15_ID" Offset="0x3E1" Value="0x55" />
<Parameter Name="TxParamEntry_15_Tx1" Offset="0x3E2" Value="0x00" />
<Parameter Name="TxParamEntry_15_Tx2" Offset="0x3E3" Value="0x64" />
<Parameter Name="TxParamEntry_16_ID" Offset="0x3E4" Value="0x56" />
<Parameter Name="TxParamEntry_16_Tx1" Offset="0x3E5" Value="0x00" />
<Parameter Name="TxParamEntry_16_Tx2" Offset="0x3E6" Value="0x64" />
<Parameter Name="TxParamEntry_17_ID" Offset="0x3E7" Value="0x57" />
<Parameter Name="TxParamEntry_17_Tx1" Offset="0x3E8" Value="0x00" />
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<Parameter Name="TxParamEntry_39_Tx1" Offset="0x44E" Value="0x00" />
<Parameter Name="TxParamEntry_39_Tx2" Offset="0x44F" Value="0x37" />
<Parameter Name="TxParamEntry_3A_ID" Offset="0x450" Value="0x7A" />
<Parameter Name="TxParamEntry_3A_Tx1" Offset="0x451" Value="0x00" />
<Parameter Name="TxParamEntry_3A_Tx2" Offset="0x452" Value="0x37" />
<Parameter Name="TxParamEntry_3B_ID" Offset="0x453" Value="0x7B" />
<Parameter Name="TxParamEntry_3B_Tx1" Offset="0x454" Value="0x00" />
<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
<Parameter Name="TxParamEntry_3C_ID" Offset="0x456" Value="0x7C" />
<Parameter Name="TxParamEntry_3C_Tx1" Offset="0x457" Value="0x00" />
<Parameter Name="TxParamEntry_3C_Tx2" Offset="0x458" Value="0x37" />
<Parameter Name="TxParamEntry_3D_ID" Offset="0x459" Value="0x7D" />
<Parameter Name="TxParamEntry_3D_Tx1" Offset="0x45A" Value="0x00" />
<Parameter Name="TxParamEntry_3D_Tx2" Offset="0x45B" Value="0x37" />
<Parameter Name="TxParamEntry_3E_ID" Offset="0x45C" Value="0x7E" />
<Parameter Name="TxParamEntry_3E_Tx1" Offset="0x45D" Value="0x00" />
<Parameter Name="TxParamEntry_3E_Tx2" Offset="0x45E" Value="0x37" />
<Parameter Name="TxParamEntry_3F_ID" Offset="0x45F" Value="0x7F" />
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<Parameter Name="TxParamEntry_3F_Tx2" Offset="0x461" Value="0x37" />
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<Parameter Name="TxParamEntry_40_Tx1" Offset="0x463" Value="0x00" />
<Parameter Name="TxParamEntry_40_Tx2" Offset="0x464" Value="0x37" />
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<Parameter Name="TxParamEntry_41_Tx1" Offset="0x466" Value="0x00" />
<Parameter Name="TxParamEntry_41_Tx2" Offset="0x467" Value="0x37" />
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<Parameter Name="TxParamEntry_42_Tx1" Offset="0x469" Value="0x00" />
<Parameter Name="TxParamEntry_42_Tx2" Offset="0x46A" Value="0x37" />
<Parameter Name="TxParamEntry_43_ID" Offset="0x46B" Value="0x7F" />
<Parameter Name="TxParamEntry_43_Tx1" Offset="0x46C" Value="0x00" />
<Parameter Name="TxParamEntry_43_Tx2" Offset="0x46D" Value="0x37" />
<Parameter Name="TxParamEntry_44_ID" Offset="0x46E" Value="0x7E" />
<Parameter Name="TxParamEntry_44_Tx1" Offset="0x46F" Value="0x00" />
<Parameter Name="TxParamEntry_44_Tx2" Offset="0x470" Value="0x37" />
<Parameter Name="TxParamEntry_45_ID" Offset="0x471" Value="0x7F" />
<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
<Parameter Name="TxParamEntry_45_Tx2" Offset="0x473" Value="0x37" />
<Parameter Name="TxParamEntry_46_ID" Offset="0x474" Value="0x7E" />
<Parameter Name="TxParamEntry_46_Tx1" Offset="0x475" Value="0x00" />
<Parameter Name="TxParamEntry_46_Tx2" Offset="0x476" Value="0x37" />
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<Parameter Name="TxParamEntry_47_Tx1" Offset="0x478" Value="0x00" />
<Parameter Name="TxParamEntry_47_Tx2" Offset="0x479" Value="0x37" />
<Parameter Name="TxParamEntry_48_ID" Offset="0x47A" Value="0x7E" />
<Parameter Name="TxParamEntry_48_Tx1" Offset="0x47B" Value="0x00" />
<Parameter Name="TxParamEntry_48_Tx2" Offset="0x47C" Value="0x37" />
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<Parameter Name="TxParamEntry_49_Tx1" Offset="0x47E" Value="0x00" />
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<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
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<Parameter Name="TxParamEntry_4B_Tx1" Offset="0x484" Value="0x00" />
<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7E" />
<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7E" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
<Parameter Name="dummy" Offset="0x48F" Value="0x000000" />
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<Region RegionName="LPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
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<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
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<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
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<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x00FFFFFF" />
</Region>

<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
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<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
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<Region RegionName="TX_SHAPING_PROPRIETARY CORR" RegionAccess="RW" RegionType="DATA">
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  <Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
  <Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />
  <Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
  <Parameter Name="Correction_Entry4" Offset="0xBB5" Value="0x0000" />
  <Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
  <Parameter Name="Correction_Entry6" Offset="0xBB9" Value="0x0000" />
  <Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
  <Parameter Name="Correction_Entry8" Offset="0xBBD" Value="0x0000" />
  <Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
  <Parameter Name="Correction_Entry10" Offset="0xBC1" Value="0x0000" />
  <Parameter Name="Correction_Entry11" Offset="0xBC3" Value="0x0000" />
  <Parameter Name="Correction_Entry12" Offset="0xBC5" Value="0x0000" />
  <Parameter Name="Correction_Entry13" Offset="0xBC7" Value="0x0000" />
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  <Parameter Name="Correction_Entry15" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
  <Parameter Name="Correction_Entry17" Offset="0xBCF" Value="0x0000" />
  <Parameter Name="Correction_Entry18" Offset="0xBD1" Value="0x0000" />
  <Parameter Name="Correction_Entry19" Offset="0xBD3" Value="0x0000" />
  <Parameter Name="Correction_Entry20" Offset="0xBD5" Value="0x0000" />
  <Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
  <Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
  <Parameter Name="Correction_Entry23" Offset="0xBDE" Value="0x0000" />
  <Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
  <Parameter Name="Correction_Entry25" Offset="0xBDE" Value="0x0000" />
  <Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
  <Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
  <Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
  <Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
  <Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
  <Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
  <Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
  <Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
  <Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
  <Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
  <Parameter Name="Correction_Entry36" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry39" Offset="0xBFB" Value="0x0000" />
  <Parameter Name="Correction_Entry40" Offset="0xBFD" Value="0x0000" />
  <Parameter Name="Correction_Entry41" Offset="0xBFF" Value="0x0000" />
  <Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
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<Region RegionName="TX_SHAPING_PROPRIETARY_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xEAE6DCCD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xFAF6F2EE" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFFFFFFFF" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xCACACACA" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xCACACAD8" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xCACACACA" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xCACACACA" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xFAF9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFDFDFC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFEFDFDFE" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>

<Region RegionName="RF_CLOCK_ACTIVE_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_ActiveInitiator" Offset="0xCA8" Value="0x20050530" />
  <Parameter Name="DPLL_GEAR_ActiveInitiator" Offset="0xCAC" Value="0x0FFDFE9F" />
</Region>

<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfgNovCal" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
  <Parameter Name="CfgThreshold" Offset="0xC86" Value="0x08" />

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        <Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
        <Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
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    <Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="EnableFastVDDPDischarge" Offset="0xC8F" Value="0x00" />
    </Region>

    <Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="RmArcA_106_FDT" Offset="0xC9D" Value="0x812A805080508050C050" />
    </Region>

    <Region RegionName="15693_BR_CFG" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="Tx_Symbol23_Mod_Reg_BR_53" Offset="0xCC5" Value="0x00000005" />
        <Parameter Name="Tx_Data_Mod_Reg_BR_53" Offset="0xCC9" Value="0x00000044" />
        <Parameter Name="Tx_Symbol23_Mod_Reg_BR_106" Offset="0xCCD" Value="0x00000006" />
        <Parameter Name="Tx_Data_Mod_Reg_BR_106" Offset="0xCD1" Value="0x00000045" />
        <Parameter Name="Tx_Symbol23_Mod_Reg_BR_212" Offset="0xCD5" Value="0x00080047" />
        <Parameter Name="Tx_Data_Mod_Reg_BR_212" Offset="0xCD9" Value="0x01080006" />
    </Region>

    <Region RegionName="HIF_DELAY_CFG" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="HiFDelay" Offset="0xCDD" Value="0x32" />
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    <Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
    </Region>

    <Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
    </Region>

    <Region RegionName="LPCD_EXT_DCDC_GPIO_CTRL" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="IpcdExtDcdcEnable" Offset="0xCE0" Value="0x00" />
        <Parameter Name="IpcdExtDcdcDelayToOn" Offset="0xCE1" Value="0x64" />
        <Parameter Name="IpcdExtDcdcDelayToOff" Offset="0xCE2" Value="0x64" />
    </Region>

    <Region RegionName="IRQ_PAD_CFG" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="IrqPad_Polarity" Offset="0xCE3" Value="0x00" />
    </Region>

    <Region RegionName="RX_MULTIPLE_CLIF_RX_FRAMELEN_CFG" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="ClifRXFrameLen" Offset="0xCE4" Value="0x00EF0003" />
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    <Region RegionName="CONFIG_RX_GUARD_TO" RegionAccess="RW" RegionType="DATA">
        <Parameter Name="RxGuardTO_Multiple" Offset="0xCE8" Value="0x01" />
    </Region>

    <Region RegionName="RegisterValuePair" RegionOffset="0x74" RegionType="PROTOCOL" RegionAccess="INDIRECT">
        <Protocol ProtocolName="TX_ISO14443A_106" ProtocolIndex="0x00" ProtocolOffset="0x74">
            <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000F00FF"></Register>
            <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00003D41"></Register>
            <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00220104"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00220104"></Register>
        </Protocol>
        <Protocol ProtocolName="TX_ISO14443A_212" ProtocolIndex="0x01" ProtocolOffset="0xA1">
            <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
            <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00110105"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00110105"></Register>
        </Protocol>
        <Protocol ProtocolName="TX_ISO14443A_424" ProtocolIndex="0x02" ProtocolOffset="0xCE">
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            <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
            <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00060106"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00060106"></Register>
        </Protocol>
        <Protocol ProtocolName="TX_ISO14443A_848" ProtocolIndex="0x03" ProtocolOffset="0xFB">
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            <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
            <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00020107"></Register>
            <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00020107"></Register>
        </Protocol>
        <Protocol ProtocolName="TX_ISO14443B_106" ProtocolIndex="0x04" ProtocolOffset="0x128">
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            <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
            <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
            <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    
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## 21 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.05

### Firmware 2.5

```

-<EEPROM>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="USER_PMU">
<Parameter Value="0xB4" Offset="0x00" Name="PwrConfig"/>
<Parameter Value="0x31" Offset="0x01" Name="DcdcConfig"/>
<Parameter Value="0xFFFFAEB7" Offset="0x02" Name="TxLdoConfig"/>
<Parameter Value="0x00" Offset="0x06" Name="TxLdoVddpaHigh"/>
<Parameter Value="0x00" Offset="0x07" Name="TxLdoVddpaLow"/>
<Parameter Value="0x2A" Offset="0x08" Name="TxLdoVddpaMaxRdr"/>
<Parameter Value="0x2A" Offset="0x09" Name="TxLdoVddpaMaxCard"/>
<Parameter Value="0x1D" Offset="0x0A" Name="BoostDefaultVoltage"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="CLKGEN">
<Parameter Value="0x00" Offset="0x10" Name="XtalConfig"/>
<Parameter Value="0xFF" Offset="0x11" Name="XtalTimeOut"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="RF_CLOCK_CFG">
<Parameter Value="0x08" Offset="0x12" Name="PLLClkInputFrq"/>
<Parameter Value="0xF6" Offset="0x13" Name="XtalCheckDelay"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="USER_SMU">
<Parameter Value="0x99" Offset="0x14" Name="TempWarning"/>
<Parameter Value="0x01" Offset="0x16" Name="EnableGpio0OnOverTemp"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="RM_TECHNO_TX_SHAPING">
<Parameter Value="0x00" Offset="0x22" Name="ResidualAmplitudeLevel_A106"/>
<Parameter Value="0x33" Offset="0x23" Name="EdgeType_A106"/>
<Parameter Value="0x64" Offset="0x24" Name="EdgeStyleConfiguration_A106"/>
<Parameter Value="0x10" Offset="0x25" Name="EdgeLength_A106"/>
<Parameter Value="0x00" Offset="0x26" Name="ResidualAmplitudeLevel_A212"/>
<Parameter Value="0x33" Offset="0x27" Name="EdgeType_A212"/>
<Parameter Value="0x44" Offset="0x28" Name="EdgeStyleConfiguration_A212"/>
<Parameter Value="0x10" Offset="0x29" Name="EdgeLength_A212"/>
<Parameter Value="0x00" Offset="0x2A" Name="ResidualAmplitudeLevel_A424"/>
<Parameter Value="0x33" Offset="0x2B" Name="EdgeType_A424"/>
<Parameter Value="0x24" Offset="0x2C" Name="EdgeStyleConfiguration_A424"/>
<Parameter Value="0x10" Offset="0x2D" Name="EdgeLength_A424"/>
<Parameter Value="0x00" Offset="0x2E" Name="ResidualAmplitudeLevel_A848"/>
<Parameter Value="0x11" Offset="0x2F" Name="EdgeType_A848"/>
<Parameter Value="0x18" Offset="0x30" Name="EdgeStyleConfiguration_A848"/>
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<Parameter Value="0xCA" Offset="0x32" Name="ResidualAmplitudeLevel_B106"/>
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<Parameter Value="0x10" Offset="0x35" Name="EdgeLength_B106"/>
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<Parameter Value="0x22" Offset="0x37" Name="EdgeType_B212"/>
<Parameter Value="0x66" Offset="0x38" Name="EdgeStyleConfiguration_B212"/>
<Parameter Value="0x10" Offset="0x39" Name="EdgeLength_B212"/>
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<Parameter Value="0x22" Offset="0x3B" Name="EdgeType_B424"/>
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<Parameter Value="0x22" Offset="0x47" Name="EdgeType_F424"/>
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<Parameter Value="0x10" Offset="0x49" Name="EdgeLength_F424"/>
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<Parameter Value="0x22" Offset="0x58" Name="EdgeStyleConfiguration_V100_212"/>
<Parameter Value="0x10" Offset="0x59" Name="EdgeLength_V100_212"/>
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<Parameter Value="0x22" Offset="0x5B" Name="EdgeType_V10_26"/>
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<Parameter Value="0x23" Offset="0x60" Name="EdgeStyleConfiguration_V10_53"/>
<Parameter Value="0x10" Offset="0x61" Name="EdgeLength_V10_53"/>
<Parameter Value="0xC0" Offset="0x62" Name="ResidualAmplitudeLevel_V10_106"/>
<Parameter Value="0x22" Offset="0x63" Name="EdgeType_V10_106"/>
<Parameter Value="0x23" Offset="0x64" Name="EdgeStyleConfiguration_V10_106"/>
<Parameter Value="0x10" Offset="0x65" Name="EdgeLength_V10_106"/>
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<Parameter Value="0x23" Offset="0x68" Name="EdgeStyleConfiguration_V10_212"/>
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<Parameter Value="0x22" Offset="0x6B" Name="EdgeType_180003m3_tari18p88"/>
<Parameter Value="0x66" Offset="0x6C" Name="EdgeStyleConfiguration_180003m3_tari18p88"/>
<Parameter Value="0x10" Offset="0x6D" Name="EdgeLength_180003m3_tari18p88"/>
<Parameter Value="0xC0" Offset="0x6E" Name="ResidualAmplitudeLevel_180003m3_tari9p44"/>
<Parameter Value="0x22" Offset="0x6F" Name="EdgeType_180003m3_tari9p44"/>
<Parameter Value="0x66" Offset="0x70" Name="EdgeStyleConfiguration_180003m3_tari9p44"/>
<Parameter Value="0x10" Offset="0x71" Name="EdgeLength_180003m3_tari9p44"/>
<Parameter Value="0xCF" Offset="0x72" Name="ResidualAmplitudeLevel_B_prime106"/>
<Parameter Value="0x22" Offset="0x73" Name="EdgeType_B_prime106"/>
<Parameter Value="0x67" Offset="0x74" Name="EdgeStyleConfiguration_B_prime106"/>
<Parameter Value="0x10" Offset="0x75" Name="EdgeLength_B_prime106"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="DPC_SETTINGS">
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<Parameter Value="0x0132" Offset="0x77" Name="DPC_TARGET_CURRENT"/>
<Parameter Value="0x14" Offset="0x79" Name="DPC_HYSTERESIS_LOADING"/>
<Parameter Value="0x0A" Offset="0x7C" Name="DPC_HYSTERESIS_UNLOADING"/>
<Parameter Value="0x07" Offset="0x7D" Name="DPC_TXLDOVDDPALow"/>
<Parameter Value="0x03" Offset="0x7E" Name="DPC_TXGSN"/>
<Parameter Value="0x01" Offset="0x7F" Name="DPC_RDON_Control"/>
<Parameter Value="0x03" Offset="0x80" Name="DPC_InitialRDON_RFOon"/>
<Parameter Value="0xFF" Offset="0x87" Name="DPC_GAURD_TIME"/>
<Parameter Value="0x01" Offset="0x88" Name="DPC_ENABLE_DURING_FDT"/>
<Parameter Value="0x01" Offset="0x89" Name="DPC_GAURD_TIME_AFTER_RX"/>
<Parameter Value="0x0000137F" Offset="0x8B" Name="Entry_00"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="ARC_SETTINGS">
<Parameter Value="0x00E4" Offset="0x137" Name="ArcConfig"/>
<Parameter Value="0x2A24130E07" Offset="0x139" Name="ArcVddpa"/>
<Parameter Value="0x81348015802A8220C250" Offset="0x13E" Name="RmArcA_106"/>
<Parameter Value="0x001A00200030007F407F" Offset="0x148" Name="RmArcA_212"/>
<Parameter Value="0x001A00200040007F407F" Offset="0x152" Name="RmArcA_424"/>
<Parameter Value="0x001A00200040007F407F" Offset="0x15C" Name="RmArcA_848"/>
<Parameter Value="0x001A0020003000404050" Offset="0x166" Name="RmArcB_106"/>
<Parameter Value="0x001A002000400050407F" Offset="0x170" Name="RmArcB_212"/>
<Parameter Value="0x001A002000400050407F" Offset="0x17A" Name="RmArcB_424"/>
<Parameter Value="0x001A002000400050407F" Offset="0x184" Name="RmArcB_848"/>
<Parameter Value="0x001A00200040007F407F" Offset="0x18E" Name="RmArcF_212"/>
<Parameter Value="0x001A00200040007F407F" Offset="0x198" Name="RmArcF_424"/>
<Parameter Value="0x000A000A000A000A400A" Offset="0x1A2" Name="RmArcV_6p6"/>
<Parameter Value="0x000A000A002F002F402F" Offset="0x1AC" Name="RmArcV_26"/>
<Parameter Value="0x010A010A011F011F411F" Offset="0x1B6" Name="RmArcV_53"/>
<Parameter Value="0x000A000A002F002F402F" Offset="0x1C0" Name="RmArcV_106"/>
<Parameter Value="0x000A000A002F002F402F" Offset="0x1CA" Name="RmArcV_212"/>
<Parameter Value="0x0114011F011F001F401F" Offset="0x1D4" Name="RmArc180003m3_SC424_4Man"/>
<Parameter Value="0x0014001F003F004F404F" Offset="0x1DE" Name="RmArc180003m3_SC424_2Man"/>
<Parameter Value="0x0114011F011F001F401F" Offset="0x1E8" Name="RmArc180003m3_SC848_4Man"/>
<Parameter Value="0x0014001F003F004F404F" Offset="0x1F2" Name="RmArc180003m3_SC848_2Man"/>
<Parameter Value="0x000A000A000A000A400A" Offset="0x1FC" Name="RmArc_AI_106"/>
<Parameter Value="0x000A000A000A000A400A" Offset="0x206" Name="RmArc_AI_212"/>
<Parameter Value="0x000A000A000A000A400A" Offset="0x210" Name="RmArc_AI_424"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="RF_CLOCK_DPLL_COM">
<Parameter Value="0x002D1327" Offset="0x2A6" Name="DPLL_INIT_Default"/>

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<Parameter Value="0x04C1FEFE" Offset="0x2AA" Name="DPLL_GEAR_Default"/>
<Parameter Value="0x00000C03" Offset="0x2AE" Name="DPLL_CONTROL"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="AUTOCOLL_CFG">
<Parameter Value="0x10" Offset="0x2B2" Name="RfDebounceTimeout"/>
<Parameter Value="0x0042" Offset="0x2B3" Name="SensRes"/>
<Parameter Value="0xCCBAA" Offset="0x2B5" Name="NfcID1"/>
<Parameter Value="0x60" Offset="0x2B8" Name="SelRes"/>
<Parameter Value="0xFFD08584424B0B100814119814011401FE01" Offset="0x2B9" Name="PollRes"/>
<Parameter Value="0x00" Offset="0x2CB" Name="RandomUIDEnable"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="MFC_CFG">
<Parameter Value="0x0500" Offset="0x2CC" Name="MfcAuthTimeout"/>
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-<Region RegionType="DATA" RegionAccess="RW" RegionName="APC_RSSI">
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<Parameter Value="0x013D" Offset="0x2DC" Name="RssiTimerFirstPeriod"/>
<Parameter Value="0x09" Offset="0x2DE" Name="RssiCtrl_00_AB"/>
<Parameter Value="0x16" Offset="0x2DF" Name="RssiNbEntriesAB"/>
<Parameter Value="0x2816" Offset="0x2E0" Name="RssiThresholdAB_01"/>
<Parameter Value="0x0000" Offset="0x2E2" Name="ArbPhaseAB_01"/>
<Parameter Value="0x3215" Offset="0x2E4" Name="RssiThresholdAB_02"/>
<Parameter Value="0x0000" Offset="0x2E6" Name="ArbPhaseAB_02"/>
<Parameter Value="0x3B6E" Offset="0x2E8" Name="RssiThresholdAB_03"/>
<Parameter Value="0x0000" Offset="0x2EA" Name="ArbPhaseAB_03"/>
<Parameter Value="0x456A" Offset="0x2EC" Name="RssiThresholdAB_04"/>
<Parameter Value="0x0000" Offset="0x2EE" Name="ArbPhaseAB_04"/>
<Parameter Value="0x4FDC" Offset="0x2F0" Name="RssiThresholdAB_05"/>
<Parameter Value="0x0000" Offset="0x2F2" Name="ArbPhaseAB_05"/>
<Parameter Value="0x5983" Offset="0x2F4" Name="RssiThresholdAB_06"/>
<Parameter Value="0x0000" Offset="0x2F6" Name="ArbPhaseAB_06"/>
<Parameter Value="0x96F9" Offset="0x2F8" Name="RssiThresholdAB_07"/>
<Parameter Value="0x0000" Offset="0x2FA" Name="ArbPhaseAB_07"/>
<Parameter Value="0x96F9" Offset="0x2FC" Name="RssiThresholdAB_08"/>
<Parameter Value="0x0000" Offset="0x2FE" Name="ArbPhaseAB_08"/>
<Parameter Value="0x96F9" Offset="0x300" Name="RssiThresholdAB_09"/>
<Parameter Value="0x0000" Offset="0x302" Name="ArbPhaseAB_09"/>
<Parameter Value="0x96F9" Offset="0x304" Name="RssiThresholdAB_0A"/>
<Parameter Value="0x0000" Offset="0x306" Name="ArbPhaseAB_0A"/>
<Parameter Value="0x96F9" Offset="0x308" Name="RssiThresholdAB_0B"/>
<Parameter Value="0x0000" Offset="0x30A" Name="ArbPhaseAB_0B"/>
<Parameter Value="0x96F9" Offset="0x30C" Name="RssiThresholdAB_0C"/>
<Parameter Value="0x0000" Offset="0x30E" Name="ArbPhaseAB_0C"/>
<Parameter Value="0x96F9" Offset="0x310" Name="RssiThresholdAB_0D"/>
<Parameter Value="0x0000" Offset="0x312" Name="ArbPhaseAB_0D"/>
<Parameter Value="0x96F9" Offset="0x314" Name="RssiThresholdAB_0E"/>
<Parameter Value="0x0000" Offset="0x316" Name="ArbPhaseAB_0E"/>
<Parameter Value="0x96F9" Offset="0x318" Name="RssiThresholdAB_0F"/>
<Parameter Value="0x0000" Offset="0x31A" Name="ArbPhaseAB_0F"/>

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<Parameter Value="0x96F9" Offset="0x31C" Name="RssiThresholdAB_10"/>
<Parameter Value="0x0000" Offset="0x31E" Name="ArbPhaseAB_10"/>
<Parameter Value="0x96F9" Offset="0x320" Name="RssiThresholdAB_11"/>
<Parameter Value="0x0000" Offset="0x322" Name="ArbPhaseAB_11"/>
<Parameter Value="0x96F9" Offset="0x324" Name="RssiThresholdAB_12"/>
<Parameter Value="0x0000" Offset="0x326" Name="ArbPhaseAB_12"/>
<Parameter Value="0x96F9" Offset="0x328" Name="RssiThresholdAB_13"/>
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<Parameter Value="0x96F9" Offset="0x330" Name="RssiThresholdAB_15"/>
<Parameter Value="0x0000" Offset="0x332" Name="ArbPhaseAB_15"/>
<Parameter Value="0x96F9" Offset="0x334" Name="RssiThresholdAB_16"/>
<Parameter Value="0x0000" Offset="0x336" Name="ArbPhaseAB_16"/>
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<Parameter Value="0x96F9" Offset="0x33C" Name="RssiThresholdAB_18"/>
<Parameter Value="0x0000" Offset="0x33E" Name="ArbPhaseAB_18"/>
<Parameter Value="0x09" Offset="0x340" Name="RssiCtrl_00_F"/>
<Parameter Value="0x16" Offset="0x341" Name="RssiNbEntriesF"/>
<Parameter Value="0x2816" Offset="0x342" Name="RssiThresholdF_01"/>
<Parameter Value="0x0000" Offset="0x344" Name="ArbPhaseF_01"/>
<Parameter Value="0x3215" Offset="0x346" Name="RssiThresholdF_02"/>
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<Parameter Value="0x3B6E" Offset="0x34A" Name="RssiThresholdF_03"/>
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<Parameter Value="0x4FDC" Offset="0x352" Name="RssiThresholdF_05"/>
<Parameter Value="0x0000" Offset="0x354" Name="ArbPhaseF_05"/>
<Parameter Value="0x5983" Offset="0x356" Name="RssiThresholdF_06"/>
<Parameter Value="0x0000" Offset="0x358" Name="ArbPhaseF_06"/>
<Parameter Value="0x96F9" Offset="0x35A" Name="RssiThresholdF_07"/>
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<Parameter Value="0x96F9" Offset="0x35E" Name="RssiThresholdF_08"/>
<Parameter Value="0x0000" Offset="0x360" Name="ArbPhaseF_08"/>
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<Parameter Value="0x96F9" Offset="0x366" Name="RssiThresholdF_0A"/>
<Parameter Value="0x0000" Offset="0x368" Name="ArbPhaseF_0A"/>
<Parameter Value="0x96F9" Offset="0x36A" Name="RssiThresholdF_0B"/>
<Parameter Value="0x0000" Offset="0x36C" Name="ArbPhaseF_0B"/>
<Parameter Value="0x96F9" Offset="0x36E" Name="RssiThresholdF_0C"/>
<Parameter Value="0x0000" Offset="0x370" Name="ArbPhaseF_0C"/>
<Parameter Value="0x96F9" Offset="0x372" Name="RssiThresholdF_0D"/>
<Parameter Value="0x0000" Offset="0x374" Name="ArbPhaseF_0D"/>
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<Parameter Value="0x96F9" Offset="0x37A" Name="RssiThresholdF_0F"/>
<Parameter Value="0x0000" Offset="0x37C" Name="ArbPhaseF_0F"/>
<Parameter Value="0x96F9" Offset="0x37E" Name="RssiThresholdF_10"/>

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<Parameter Value="0x0000" Offset="0x380" Name="ArbPhaseF_10"/>
<Parameter Value="0x96F9" Offset="0x382" Name="RssiThresholdF_11"/>
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<Parameter Value="0x96F9" Offset="0x386" Name="RssiThresholdF_12"/>
<Parameter Value="0x0000" Offset="0x388" Name="ArbPhaseF_12"/>
<Parameter Value="0x96F9" Offset="0x38A" Name="RssiThresholdF_13"/>
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<Parameter Value="0x96F9" Offset="0x392" Name="RssiThresholdF_15"/>
<Parameter Value="0x0000" Offset="0x394" Name="ArbPhaseF_15"/>
<Parameter Value="0x96F9" Offset="0x396" Name="RssiThresholdF_16"/>
<Parameter Value="0x0000" Offset="0x398" Name="ArbPhaseF_16"/>
<Parameter Value="0x96F9" Offset="0x39A" Name="RssiThresholdF_17"/>
<Parameter Value="0x0000" Offset="0x39C" Name="ArbPhaseF_17"/>
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<Parameter Value="0x41" Offset="0x3A5" Name="TxParamEntry_01_ID"/>
<Parameter Value="0x00" Offset="0x3A6" Name="TxParamEntry_01_Tx1"/>
<Parameter Value="0x64" Offset="0x3A7" Name="TxParamEntry_01_Tx2"/>
<Parameter Value="0x42" Offset="0x3A8" Name="TxParamEntry_02_ID"/>
<Parameter Value="0x00" Offset="0x3A9" Name="TxParamEntry_02_Tx1"/>
<Parameter Value="0x64" Offset="0x3AA" Name="TxParamEntry_02_Tx2"/>
<Parameter Value="0x43" Offset="0x3AB" Name="TxParamEntry_03_ID"/>
<Parameter Value="0x00" Offset="0x3AC" Name="TxParamEntry_03_Tx1"/>
<Parameter Value="0x64" Offset="0x3AD" Name="TxParamEntry_03_Tx2"/>
<Parameter Value="0x44" Offset="0x3AE" Name="TxParamEntry_04_ID"/>
<Parameter Value="0x00" Offset="0x3AF" Name="TxParamEntry_04_Tx1"/>
<Parameter Value="0x64" Offset="0x3B0" Name="TxParamEntry_04_Tx2"/>
<Parameter Value="0x45" Offset="0x3B1" Name="TxParamEntry_05_ID"/>
<Parameter Value="0x00" Offset="0x3B2" Name="TxParamEntry_05_Tx1"/>
<Parameter Value="0x64" Offset="0x3B3" Name="TxParamEntry_05_Tx2"/>
<Parameter Value="0x46" Offset="0x3B4" Name="TxParamEntry_06_ID"/>
<Parameter Value="0x00" Offset="0x3B5" Name="TxParamEntry_06_Tx1"/>
<Parameter Value="0x64" Offset="0x3B6" Name="TxParamEntry_06_Tx2"/>
<Parameter Value="0x47" Offset="0x3B7" Name="TxParamEntry_07_ID"/>
<Parameter Value="0x00" Offset="0x3B8" Name="TxParamEntry_07_Tx1"/>
<Parameter Value="0x64" Offset="0x3B9" Name="TxParamEntry_07_Tx2"/>
<Parameter Value="0x48" Offset="0x3BA" Name="TxParamEntry_08_ID"/>
<Parameter Value="0x00" Offset="0x3BB" Name="TxParamEntry_08_Tx1"/>
<Parameter Value="0x64" Offset="0x3BC" Name="TxParamEntry_08_Tx2"/>
<Parameter Value="0x49" Offset="0x3BD" Name="TxParamEntry_09_ID"/>
<Parameter Value="0x00" Offset="0x3BE" Name="TxParamEntry_09_Tx1"/>
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<Parameter Value="0x5D" Offset="0x3C2" Name="TxParamEntry_0A_Tx2"/>
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<Parameter Value="0x00" Offset="0x3C4" Name="TxParamEntry_0B_Tx1"/>
<Parameter Value="0x56" Offset="0x3C5" Name="TxParamEntry_0B_Tx2"/>
<Parameter Value="0x4C" Offset="0x3C6" Name="TxParamEntry_0C_ID"/>
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<Parameter Value="0x4F" Offset="0x3C8" Name="TxParamEntry_00C_Tx2"/>
<Parameter Value="0x4D" Offset="0x3C9" Name="TxParamEntry_0D_ID"/>
<Parameter Value="0x00" Offset="0x3CA" Name="TxParamEntry_0D_Tx1"/>
<Parameter Value="0x47" Offset="0x3CB" Name="TxParamEntry_0D_Tx2"/>
<Parameter Value="0x4E" Offset="0x3CC" Name="TxParamEntry_0E_ID"/>
<Parameter Value="0x00" Offset="0x3CD" Name="TxParamEntry_0E_Tx1"/>
<Parameter Value="0x3F" Offset="0x3CE" Name="TxParamEntry_0E_Tx2"/>
<Parameter Value="0x4F" Offset="0x3CF" Name="TxParamEntry_0F_ID"/>
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<Parameter Value="0x50" Offset="0x3D2" Name="TxParamEntry_10_ID"/>
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<Parameter Value="0x37" Offset="0x3D4" Name="TxParamEntry_10_Tx2"/>
<Parameter Value="0x51" Offset="0x3D5" Name="TxParamEntry_11_ID"/>
<Parameter Value="0x00" Offset="0x3D6" Name="TxParamEntry_11_Tx1"/>
<Parameter Value="0x37" Offset="0x3D7" Name="TxParamEntry_11_Tx2"/>
<Parameter Value="0x52" Offset="0x3D8" Name="TxParamEntry_12_ID"/>
<Parameter Value="0x00" Offset="0x3D9" Name="TxParamEntry_12_Tx1"/>
<Parameter Value="0x37" Offset="0x3DA" Name="TxParamEntry_12_Tx2"/>
<Parameter Value="0x53" Offset="0x3DB" Name="TxParamEntry_13_ID"/>
<Parameter Value="0x00" Offset="0x3DC" Name="TxParamEntry_13_Tx1"/>
<Parameter Value="0x37" Offset="0x3DD" Name="TxParamEntry_13_Tx2"/>
<Parameter Value="0x54" Offset="0x3DE" Name="TxParamEntry_14_ID"/>
<Parameter Value="0x00" Offset="0x3DF" Name="TxParamEntry_14_Tx1"/>
<Parameter Value="0x37" Offset="0x3E0" Name="TxParamEntry_14_Tx2"/>
<Parameter Value="0x55" Offset="0x3E1" Name="TxParamEntry_15_ID"/>
<Parameter Value="0x00" Offset="0x3E2" Name="TxParamEntry_15_Tx1"/>
<Parameter Value="0x37" Offset="0x3E3" Name="TxParamEntry_15_Tx2"/>
<Parameter Value="0x56" Offset="0x3E4" Name="TxParamEntry_16_ID"/>
<Parameter Value="0x00" Offset="0x3E5" Name="TxParamEntry_16_Tx1"/>
<Parameter Value="0x37" Offset="0x3E6" Name="TxParamEntry_16_Tx2"/>
<Parameter Value="0x57" Offset="0x3E7" Name="TxParamEntry_17_ID"/>
<Parameter Value="0x00" Offset="0x3E8" Name="TxParamEntry_17_Tx1"/>
<Parameter Value="0x37" Offset="0x3E9" Name="TxParamEntry_17_Tx2"/>
<Parameter Value="0x58" Offset="0x3EA" Name="TxParamEntry_18_ID"/>
<Parameter Value="0x00" Offset="0x3EB" Name="TxParamEntry_18_Tx1"/>
<Parameter Value="0x37" Offset="0x3EC" Name="TxParamEntry_18_Tx2"/>
<Parameter Value="0x59" Offset="0x3ED" Name="TxParamEntry_19_ID"/>
<Parameter Value="0x00" Offset="0x3EE" Name="TxParamEntry_19_Tx1"/>
<Parameter Value="0x37" Offset="0x3EF" Name="TxParamEntry_19_Tx2"/>
<Parameter Value="0x5A" Offset="0x3F0" Name="TxParamEntry_1A_ID"/>
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<Parameter Value="0x5B" Offset="0x3F3" Name="TxParamEntry_1B_ID"/>
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<Parameter Value="0x00" Offset="0x3F7" Name="TxParamEntry_1C_Tx1"/>
<Parameter Value="0x37" Offset="0x3F8" Name="TxParamEntry_1C_Tx2"/>
<Parameter Value="0x5D" Offset="0x3F9" Name="TxParamEntry_1D_ID"/>
<Parameter Value="0x00" Offset="0x3FA" Name="TxParamEntry_1D_Tx1"/>
<Parameter Value="0x37" Offset="0x3FB" Name="TxParamEntry_1D_Tx2"/>
<Parameter Value="0x5E" Offset="0x3FC" Name="TxParamEntry_1E_ID"/>
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<Parameter Value="0x37" Offset="0x3FE" Name="TxParamEntry_1E_Tx2"/>
<Parameter Value="0x5F" Offset="0x3FF" Name="TxParamEntry_1F_ID"/>
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<Parameter Value="0x00" Offset="0x403" Name="TxParamEntry_20_Tx1"/>
<Parameter Value="0x37" Offset="0x404" Name="TxParamEntry_20_Tx2"/>
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<Parameter Value="0x00" Offset="0x406" Name="TxParamEntry_21_Tx1"/>
<Parameter Value="0x37" Offset="0x407" Name="TxParamEntry_21_Tx2"/>
<Parameter Value="0x62" Offset="0x408" Name="TxParamEntry_22_ID"/>
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<Parameter Value="0x37" Offset="0x40A" Name="TxParamEntry_22_Tx2"/>
<Parameter Value="0x63" Offset="0x40B" Name="TxParamEntry_23_ID"/>
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<Parameter Value="0x64" Offset="0x40E" Name="TxParamEntry_24_ID"/>
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<Parameter Value="0x37" Offset="0x410" Name="TxParamEntry_24_Tx2"/>
<Parameter Value="0x65" Offset="0x411" Name="TxParamEntry_25_ID"/>
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<Parameter Value="0x00" Offset="0x415" Name="TxParamEntry_26_Tx1"/>
<Parameter Value="0x37" Offset="0x416" Name="TxParamEntry_26_Tx2"/>
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<Parameter Value="0x37" Offset="0x41C" Name="TxParamEntry_28_Tx2"/>
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<Parameter Value="0x37" Offset="0x41F" Name="TxParamEntry_29_Tx2"/>
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<Parameter Value="0x37" Offset="0x428" Name="TxParamEntry_2C_Tx2"/>
<Parameter Value="0x6D" Offset="0x429" Name="TxParamEntry_2D_ID"/>
<Parameter Value="0x00" Offset="0x42A" Name="TxParamEntry_2D_Tx1"/>
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<Parameter Value="0x6E" Offset="0x42C" Name="TxParamEntry_2E_ID"/>
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<Parameter Value="0x37" Offset="0x431" Name="TxParamEntry_2F_Tx2"/>
<Parameter Value="0x70" Offset="0x432" Name="TxParamEntry_30_ID"/>
<Parameter Value="0x00" Offset="0x433" Name="TxParamEntry_30_Tx1"/>
<Parameter Value="0x37" Offset="0x434" Name="TxParamEntry_30_Tx2"/>
<Parameter Value="0x71" Offset="0x435" Name="TxParamEntry_31_ID"/>
<Parameter Value="0x00" Offset="0x436" Name="TxParamEntry_31_Tx1"/>
<Parameter Value="0x37" Offset="0x437" Name="TxParamEntry_31_Tx2"/>
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<Parameter Value="0x73" Offset="0x43B" Name="TxParamEntry_33_ID"/>
<Parameter Value="0x00" Offset="0x43C" Name="TxParamEntry_33_Tx1"/>
<Parameter Value="0x37" Offset="0x43D" Name="TxParamEntry_33_Tx2"/>
<Parameter Value="0x74" Offset="0x43E" Name="TxParamEntry_34_ID"/>
<Parameter Value="0x00" Offset="0x43F" Name="TxParamEntry_34_Tx1"/>
<Parameter Value="0x37" Offset="0x440" Name="TxParamEntry_34_Tx2"/>
<Parameter Value="0x75" Offset="0x441" Name="TxParamEntry_35_ID"/>
<Parameter Value="0x00" Offset="0x442" Name="TxParamEntry_35_Tx1"/>
<Parameter Value="0x37" Offset="0x443" Name="TxParamEntry_35_Tx2"/>
<Parameter Value="0x76" Offset="0x444" Name="TxParamEntry_36_ID"/>
<Parameter Value="0x00" Offset="0x445" Name="TxParamEntry_36_Tx1"/>
<Parameter Value="0x37" Offset="0x446" Name="TxParamEntry_36_Tx2"/>
<Parameter Value="0x77" Offset="0x447" Name="TxParamEntry_37_ID"/>
<Parameter Value="0x00" Offset="0x448" Name="TxParamEntry_37_Tx1"/>
<Parameter Value="0x37" Offset="0x449" Name="TxParamEntry_37_Tx2"/>
<Parameter Value="0x78" Offset="0x44A" Name="TxParamEntry_38_ID"/>
<Parameter Value="0x00" Offset="0x44B" Name="TxParamEntry_38_Tx1"/>
<Parameter Value="0x37" Offset="0x44C" Name="TxParamEntry_38_Tx2"/>
<Parameter Value="0x79" Offset="0x44D" Name="TxParamEntry_39_ID"/>
<Parameter Value="0x00" Offset="0x44E" Name="TxParamEntry_39_Tx1"/>
<Parameter Value="0x37" Offset="0x44F" Name="TxParamEntry_39_Tx2"/>
<Parameter Value="0x7A" Offset="0x450" Name="TxParamEntry_3A_ID"/>
<Parameter Value="0x00" Offset="0x451" Name="TxParamEntry_3A_Tx1"/>
<Parameter Value="0x37" Offset="0x452" Name="TxParamEntry_3A_Tx2"/>
<Parameter Value="0x7B" Offset="0x453" Name="TxParamEntry_3B_ID"/>
<Parameter Value="0x00" Offset="0x454" Name="TxParamEntry_3B_Tx1"/>
<Parameter Value="0x37" Offset="0x455" Name="TxParamEntry_3B_Tx2"/>
<Parameter Value="0x7C" Offset="0x456" Name="TxParamEntry_3C_ID"/>
<Parameter Value="0x00" Offset="0x457" Name="TxParamEntry_3C_Tx1"/>

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<Parameter Value="0x37" Offset="0x458" Name="TxParamEntry_3C_Tx2"/>
<Parameter Value="0x7D" Offset="0x459" Name="TxParamEntry_3D_ID"/>
<Parameter Value="0x00" Offset="0x45A" Name="TxParamEntry_3D_Tx1"/>
<Parameter Value="0x37" Offset="0x45B" Name="TxParamEntry_3D_Tx2"/>
<Parameter Value="0x7E" Offset="0x45C" Name="TxParamEntry_3E_ID"/>
<Parameter Value="0x00" Offset="0x45D" Name="TxParamEntry_3E_Tx1"/>
<Parameter Value="0x37" Offset="0x45E" Name="TxParamEntry_3E_Tx2"/>
<Parameter Value="0x7F" Offset="0x45F" Name="TxParamEntry_3F_ID"/>
<Parameter Value="0x00" Offset="0x460" Name="TxParamEntry_3F_Tx1"/>
<Parameter Value="0x37" Offset="0x461" Name="TxParamEntry_3F_Tx2"/>
<Parameter Value="0x7F" Offset="0x462" Name="TxParamEntry_40_ID"/>
<Parameter Value="0x00" Offset="0x463" Name="TxParamEntry_40_Tx1"/>
<Parameter Value="0x37" Offset="0x464" Name="TxParamEntry_40_Tx2"/>
<Parameter Value="0x7F" Offset="0x465" Name="TxParamEntry_41_ID"/>
<Parameter Value="0x00" Offset="0x466" Name="TxParamEntry_41_Tx1"/>
<Parameter Value="0x37" Offset="0x467" Name="TxParamEntry_41_Tx2"/>
<Parameter Value="0x7F" Offset="0x468" Name="TxParamEntry_42_ID"/>
<Parameter Value="0x00" Offset="0x469" Name="TxParamEntry_42_Tx1"/>
<Parameter Value="0x37" Offset="0x46A" Name="TxParamEntry_42_Tx2"/>
<Parameter Value="0x7F" Offset="0x46B" Name="TxParamEntry_43_ID"/>
<Parameter Value="0x00" Offset="0x46C" Name="TxParamEntry_43_Tx1"/>
<Parameter Value="0x37" Offset="0x46D" Name="TxParamEntry_43_Tx2"/>
<Parameter Value="0x7F" Offset="0x46E" Name="TxParamEntry_44_ID"/>
<Parameter Value="0x00" Offset="0x46F" Name="TxParamEntry_44_Tx1"/>
<Parameter Value="0x37" Offset="0x470" Name="TxParamEntry_44_Tx2"/>
<Parameter Value="0x7F" Offset="0x471" Name="TxParamEntry_45_ID"/>
<Parameter Value="0x00" Offset="0x472" Name="TxParamEntry_45_Tx1"/>
<Parameter Value="0x37" Offset="0x473" Name="TxParamEntry_45_Tx2"/>
<Parameter Value="0x7F" Offset="0x474" Name="TxParamEntry_46_ID"/>
<Parameter Value="0x00" Offset="0x475" Name="TxParamEntry_46_Tx1"/>
<Parameter Value="0x37" Offset="0x476" Name="TxParamEntry_46_Tx2"/>
<Parameter Value="0x7F" Offset="0x477" Name="TxParamEntry_47_ID"/>
<Parameter Value="0x00" Offset="0x478" Name="TxParamEntry_47_Tx1"/>
<Parameter Value="0x37" Offset="0x479" Name="TxParamEntry_47_Tx2"/>
<Parameter Value="0x7F" Offset="0x47A" Name="TxParamEntry_48_ID"/>
<Parameter Value="0x00" Offset="0x47B" Name="TxParamEntry_48_Tx1"/>
<Parameter Value="0x37" Offset="0x47C" Name="TxParamEntry_48_Tx2"/>
<Parameter Value="0x7F" Offset="0x47D" Name="TxParamEntry_49_ID"/>
<Parameter Value="0x00" Offset="0x47E" Name="TxParamEntry_49_Tx1"/>
<Parameter Value="0x37" Offset="0x47F" Name="TxParamEntry_49_Tx2"/>
<Parameter Value="0x7F" Offset="0x480" Name="TxParamEntry_4A_ID"/>
<Parameter Value="0x00" Offset="0x481" Name="TxParamEntry_4A_Tx1"/>
<Parameter Value="0x37" Offset="0x482" Name="TxParamEntry_4A_Tx2"/>
<Parameter Value="0x7F" Offset="0x483" Name="TxParamEntry_4B_ID"/>
<Parameter Value="0x00" Offset="0x484" Name="TxParamEntry_4B_Tx1"/>
<Parameter Value="0x37" Offset="0x485" Name="TxParamEntry_4B_Tx2"/>
<Parameter Value="0x7F" Offset="0x486" Name="TxParamEntry_4C_ID"/>
<Parameter Value="0x00" Offset="0x487" Name="TxParamEntry_4C_Tx1"/>
<Parameter Value="0x37" Offset="0x488" Name="TxParamEntry_4C_Tx2"/>
<Parameter Value="0x7F" Offset="0x489" Name="TxParamEntry_4D_ID"/>
<Parameter Value="0x00" Offset="0x48A" Name="TxParamEntry_4D_Tx1"/>

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<Parameter Value="0x37" Offset="0x48B" Name="TxParamEntry_4D_Tx2"/>
<Parameter Value="0x7F" Offset="0x48C" Name="TxParamEntry_4E_ID"/>
<Parameter Value="0x00" Offset="0x48D" Name="TxParamEntry_4E_Tx1"/>
<Parameter Value="0x37" Offset="0x48E" Name="TxParamEntry_4E_Tx2"/>
<Parameter Value="0x000000" Offset="0x48F" Name="dummy"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="LPCD_SETTINGS">
<Parameter Value="0x06" Offset="0x492" Name="avg_samples"/>
<Parameter Value="0x02A3" Offset="0x494" Name="lpcd_rssi_target"/>
<Parameter Value="0x1F" Offset="0x496" Name="lpcd_rssi_hyst"/>
<Parameter Value="0x003B" Offset="0x497" Name="Config"/>
<Parameter Value="0x00500050" Offset="0x49A" Name="lpcd_threshold_coarse"/>
<Parameter Value="0x7FFF7FFF" Offset="0x49E" Name="lpcd_threshold_fine"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="ULPCD_CONFIG">
<Parameter Value="0x0206" Offset="0x4BF" Name="Vddpa_Ctrl"/>
<Parameter Value="0x3D" Offset="0x4C2" Name="Timing_Ctrl"/>
<Parameter Value="0x6A" Offset="0x4C6" Name="Voltage_Ctrl"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="ULPCD_SETTINGS">
<Parameter Value="0x10" Offset="0x4C9" Name="rssi_nsp"/>
<Parameter Value="0x00" Offset="0x4CA" Name="rssi_no_samples"/>
<Parameter Value="0x0C" Offset="0x4CB" Name="thresh_lvl"/>
<Parameter Value="0x01" Offset="0x4CC" Name="polarity"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TXIRQ_GUARD">
<Parameter Value="0x000FFFFF" Offset="0x559" Name="TXIRQ_GuardTime"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="FDT_DEFAULT">
<Parameter Value="0x000472AC" Offset="0x55D" Name="FDT_DefaultVal"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="RXIRQ_GUARD">
<Parameter Value="0x000F4240" Offset="0x561" Name="RXIRQ_GuardTime"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_SHAPING_PROPRIETARY_CORR">
<Parameter Value="0x0000" Offset="0xBAD" Name="Correction_Entry0"/>
<Parameter Value="0x0000" Offset="0xBAF" Name="Correction_Entry1"/>
<Parameter Value="0x0000" Offset="0xBB1" Name="Correction_Entry2"/>
<Parameter Value="0x0000" Offset="0xBB3" Name="Correction_Entry3"/>
<Parameter Value="0x0000" Offset="0xBB5" Name="Correction_Entry4"/>
<Parameter Value="0x0000" Offset="0xBB7" Name="Correction_Entry5"/>
<Parameter Value="0x0000" Offset="0xBB9" Name="Correction_Entry6"/>
<Parameter Value="0x0000" Offset="0xBBB" Name="Correction_Entry7"/>
<Parameter Value="0x0000" Offset="0xBBD" Name="Correction_Entry8"/>
<Parameter Value="0x0000" Offset="0xBBF" Name="Correction_Entry9"/>
<Parameter Value="0x0000" Offset="0xBC1" Name="Correction_Entry10"/>
<Parameter Value="0x0000" Offset="0xBC3" Name="Correction_Entry11"/>

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<Parameter Value="0x0000" Offset="0xBC5" Name="Correction_Entry12"/>
<Parameter Value="0x0000" Offset="0xBC7" Name="Correction_Entry13"/>
<Parameter Value="0x0000" Offset="0xBC9" Name="Correction_Entry14"/>
<Parameter Value="0x0000" Offset="0xBCB" Name="Correction_Entry15"/>
<Parameter Value="0x0000" Offset="0xBCD" Name="Correction_Entry16"/>
<Parameter Value="0x0000" Offset="0xBCF" Name="Correction_Entry17"/>
<Parameter Value="0x0000" Offset="0xBD1" Name="Correction_Entry18"/>
<Parameter Value="0x0000" Offset="0xBD3" Name="Correction_Entry19"/>
<Parameter Value="0x0000" Offset="0xBD5" Name="Correction_Entry20"/>
<Parameter Value="0x0000" Offset="0xBD7" Name="Correction_Entry21"/>
<Parameter Value="0x0000" Offset="0xBD9" Name="Correction_Entry22"/>
<Parameter Value="0x0000" Offset="0xBDB" Name="Correction_Entry23"/>
<Parameter Value="0x0000" Offset="0xBDD" Name="Correction_Entry24"/>
<Parameter Value="0x0000" Offset="0xBDF" Name="Correction_Entry25"/>
<Parameter Value="0x0000" Offset="0xBE1" Name="Correction_Entry26"/>
<Parameter Value="0x0000" Offset="0xBE3" Name="Correction_Entry27"/>
<Parameter Value="0x0000" Offset="0xBE5" Name="Correction_Entry28"/>
<Parameter Value="0x0000" Offset="0xBE7" Name="Correction_Entry29"/>
<Parameter Value="0x0000" Offset="0xBE9" Name="Correction_Entry30"/>
<Parameter Value="0x0000" Offset="0xBEB" Name="Correction_Entry31"/>
<Parameter Value="0x0000" Offset="0xBED" Name="Correction_Entry32"/>
<Parameter Value="0x0000" Offset="0xBEF" Name="Correction_Entry33"/>
<Parameter Value="0x0000" Offset="0xBF1" Name="Correction_Entry34"/>
<Parameter Value="0x0000" Offset="0xBF3" Name="Correction_Entry35"/>
<Parameter Value="0x0000" Offset="0xBF5" Name="Correction_Entry36"/>
<Parameter Value="0x0000" Offset="0xBF7" Name="Correction_Entry37"/>
<Parameter Value="0x0000" Offset="0xBF9" Name="Correction_Entry38"/>
<Parameter Value="0x0000" Offset="0xBF3" Name="Correction_Entry39"/>
<Parameter Value="0x0000" Offset="0xBF5" Name="Correction_Entry40"/>
<Parameter Value="0x0000" Offset="0xBF7" Name="Correction_Entry41"/>
<Parameter Value="0x0000" Offset="0xBF9" Name="Correction_Entry42"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_SHAPING_PROPRIETARY_1">
<Parameter Value="0xEAE6DCCD" Offset="0xC03" Name="RTRANS0"/>
<Parameter Value="0xFAF6F2EE" Offset="0xC07" Name="RTRANS1"/>
<Parameter Value="0xFFFFFFFF" Offset="0xC0B" Name="RTRANS2"/>
<Parameter Value="0xFFFFFFFF" Offset="0xC0F" Name="RTRANS3"/>
<Parameter Value="0xCACACACA" Offset="0xC13" Name="FTRANS0"/>
<Parameter Value="0xCACACAD8" Offset="0xC17" Name="FTRANS1"/>
<Parameter Value="0xCACACACA" Offset="0xC1B" Name="FTRANS2"/>
<Parameter Value="0xCACACACA" Offset="0xC1F" Name="FTRANS3"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_SHAPING_PROPRIETARY_2">
<Parameter Value="0xF0EAE3DA" Offset="0xC23" Name="RTRANS0"/>
<Parameter Value="0xFAF9F6F4" Offset="0xC27" Name="RTRANS1"/>
<Parameter Value="0xFEFDFFDF" Offset="0xC2B" Name="RTRANS2"/>
<Parameter Value="0xFFFFFFFF" Offset="0xC2F" Name="RTRANS3"/>
<Parameter Value="0xFEFFFFFF" Offset="0xC33" Name="FTRANS0"/>
<Parameter Value="0xFCFDFDFE" Offset="0xC37" Name="FTRANS1"/>

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<Parameter Value="0xF4F6F9FA" Offset="0xC3B" Name="FTRANS2"/>
<Parameter Value="0xDAE3EAF0" Offset="0xC3F" Name="FTRANS3"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_SHAPING_PROPRIETARY_3">
<Parameter Value="0x00000000" Offset="0xC43" Name="RTRANS0"/>
<Parameter Value="0x00000000" Offset="0xC47" Name="RTRANS1"/>
<Parameter Value="0x00000000" Offset="0xC4B" Name="RTRANS2"/>
<Parameter Value="0x00000000" Offset="0xC4F" Name="RTRANS3"/>
<Parameter Value="0x00000000" Offset="0xC53" Name="FTRANS0"/>
<Parameter Value="0x00000000" Offset="0xC57" Name="FTRANS1"/>
<Parameter Value="0x00000000" Offset="0xC5B" Name="FTRANS2"/>
<Parameter Value="0x00000000" Offset="0xC5F" Name="FTRANS3"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_SHAPING_PROPRIETARY_4">
<Parameter Value="0x00000000" Offset="0xC63" Name="RTRANS0"/>
<Parameter Value="0x00000000" Offset="0xC67" Name="RTRANS1"/>
<Parameter Value="0x00000000" Offset="0xC6B" Name="RTRANS2"/>
<Parameter Value="0x00000000" Offset="0xC6F" Name="RTRANS3"/>
<Parameter Value="0x00000000" Offset="0xC73" Name="FTRANS0"/>
<Parameter Value="0x00000000" Offset="0xC77" Name="FTRANS1"/>
<Parameter Value="0x00000000" Offset="0xC7B" Name="FTRANS2"/>
<Parameter Value="0x00000000" Offset="0xC7F" Name="FTRANS3"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="RF_CLOCK_ACTIVE_DPLL_COM">
<Parameter Value="0x20050530" Offset="0xCA8" Name="DPLL_INIT_ActiveInitiator"/>
<Parameter Value="0x0FFDFEFFF" Offset="0xCAC" Name="DPLL_GEAR_ActiveInitiator"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="TX_DRIVER_NOV">
<Parameter Value="0x42" Offset="0xC83" Name="CfgNovCal"/>
<Parameter Value="0x03" Offset="0xC84" Name="VddpaCalVal1"/>
<Parameter Value="0x15" Offset="0xC85" Name="VddpaCalVal2"/>
<Parameter Value="0x08" Offset="0xC86" Name="CfgThreshold"/>
<Parameter Value="0x8A0A0C00" Offset="0xC87" Name="UserOffsets1"/>
<Parameter Value="0x09080D03" Offset="0xC8B" Name="UserOffsets2"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="USER_PMU_INT_1">
<Parameter Value="0x00" Offset="0xC8F" Name="EnableFastVDDPADischarge"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="ARC_SETTINGS_1">
<Parameter Value="0x812A805080508050C050" Offset="0xC9D" Name="RmArcA_106_FDT"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="15693_BR_CFG">
<Parameter Value="0x00000005" Offset="0xCC5" Name="Tx_Symbol23_Mod_Reg_BR_53"/>
<Parameter Value="0x00000044" Offset="0xCC9" Name="Tx_Data_Mod_Reg_BR_53"/>
<Parameter Value="0x00000006" Offset="0xCCD" Name="Tx_Symbol23_Mod_Reg_BR_106"/>
<Parameter Value="0x00000045" Offset="0xCD1" Name="Tx_Data_Mod_Reg_BR_106"/>
<Parameter Value="0x00080047" Offset="0xCD5" Name="Tx_Symbol23_Mod_Reg_BR_212"/>

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<Parameter Value="0x01080006" Offset="0xCD9" Name="Tx_Data_Mod_Reg_BR_212"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="HIF_DELAY_CFG">
<Parameter Value="0x32" Offset="0xCDD" Name="HifDelay"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="AUTOCOLL_CFG_1">
<Parameter Value="0x00" Offset="0xCDF" Name="CardModeUltraLowPowerEnabled"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="AUTOCOLL_CFG_1">
<Parameter Value="0x00" Offset="0xCDF" Name="CardModeUltraLowPowerEnabled"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="LPCD_EXT_DCDC_GPIO_CTRL">
<Parameter Value="0x00" Offset="0xCE0" Name="LpcdExtDcdcEnable"/>
<Parameter Value="0x64" Offset="0xCE1" Name="LpcdExtDcdcDelayToOn"/>
<Parameter Value="0x64" Offset="0xCE2" Name="LpcdExtDcdcDelayToOff"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="IRQ_PAD_CFG">
<Parameter Value="0x00" Offset="0xCE3" Name="IrqPad_Polarity"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="RX_MULTIPLE_CLIF_RX_FRAMELEN_CFG">
<Parameter Value="0x00EF0003" Offset="0xCE4" Name="ClifRXFrameLen"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="CONFIG_RX_GUARD_TO">
<Parameter Value="0x01" Offset="0xCE8" Name="RxGuardTO_Multiple"/>
</Region>

-<Region RegionType="DATA" RegionAccess="RW" RegionName="COMBINED_TB_SETTINGS">
<Parameter Value="0x9B" Offset="0xCE9" Name="DigitalTBSignalIndex"/>
<Parameter Value="0x04" Offset="0xCEA" Name="DigitalTBSignalBit"/>
<Parameter Value="0x78" Offset="0xCEB" Name="AnalogTBSignal"/>
</Region>

-<Region RegionType="PROTOCOL" RegionAccess="INDIRECT" RegionName="RegisterValuePair" RegionOffset="0x74">

-<Protocol ProtocolOffset="0x74" ProtocolIndex="0x00" ProtocolName="TX_ISO14443A_106">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000F00FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00003D41" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00220104" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00220104" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0xA1" ProtocolIndex="0x01" ProtocolName="TX_ISO14443A_212">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>

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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00110105" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00110105" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0xCE" ProtocolIndex="0x02" ProtocolName="TX ISO14443A 424">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00060106" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00060106" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0xFB" ProtocolIndex="0x03" ProtocolName="TX ISO14443A 848">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00020107" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00020107" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x128" ProtocolIndex="0x04" ProtocolName="TX ISO14443B 106">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00030107" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000084" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x155" ProtocolIndex="0x05" ProtocolName="TX ISO14443B 212">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00030107" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>

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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000085" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x182" ProtocolIndex="0x06" ProtocolName="TX ISO14443B 424">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00030107" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000086" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x1AF" ProtocolIndex="0x07" ProtocolName="TX ISO14443B 848">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00030107" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000087" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x1DC" ProtocolIndex="0x08" ProtocolName="TX Felica 212">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000015" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x209" ProtocolIndex="0x09" ProtocolName="TX Felica 424">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000016" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x236" ProtocolIndex="0x0A" ProtocolName="TX ISO15693 ASK100">

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<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000F00FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000004" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00020084" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000043" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x263" ProtocolIndex="0x0B" ProtocolName="TX ISO15693 ASK10">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000004" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00020084" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000043" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x290" ProtocolIndex="0x0F" ProtocolName="TX ISO180003m3 TARI=18.88us">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000F00FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000004" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00020084" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000043" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x2BD" ProtocolIndex="0x10" ProtocolName="TX ISO180003m3 TARI=9.44us">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000004" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00020084" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000043" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x2EA" ProtocolIndex="0x13" ProtocolName="TX ISO14443A-PICC 106">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x001F002E" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>

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<Register RegisterValue="0x00008002" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x0000002C" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x0000002C" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x317" ProtocolIndex="0x14" ProtocolName="TX ISO14443A-PICC 212">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00007402" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x0000003D" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x344" ProtocolIndex="0x15" ProtocolName="TX ISO14443A-PICC 424">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00007402" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x0000002E" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x0000003E" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x371" ProtocolIndex="0x16" ProtocolName="TX ISO14443A-PICC 848">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00007402" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x0000002F" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x0000003F" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x39E" ProtocolIndex="0x17" ProtocolName="TX NFC-PT-212 212">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000015" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>

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</Protocol>

-<Protocol ProtocolOffset="0x3CB" ProtocolIndex="0x18" ProtocolName="TX NFC-PT-424 424">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000016" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x3F8" ProtocolIndex="0x19" ProtocolName="TX NFC-AT-106 106">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000F00FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00003D41" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00220104" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00220104" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x425" ProtocolIndex="0x1A" ProtocolName="TX NFC-AT-212 212">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000015" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x452" ProtocolIndex="0x1B" ProtocolName="TX NFC-AT-424 424">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000016" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x47F" ProtocolIndex="0x1C" ProtocolName="TX GTM All">
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000700FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>

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<Register RegisterValue="0x001F002E" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00008002" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x000002C" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x0000002C" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x4AC" ProtocolIndex="0x1D" ProtocolName="TX B_Prime All">
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3B" RegisterName="CLIF_SS_TX1_CMCFG"/>
<Register RegisterValue="0x000900FF" RegisterLogicalAddress="0x3C" RegisterName="CLIF_SS_TX2_CMCFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x13" RegisterName="CLIF_TX_UNDERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x14" RegisterName="CLIF_TX_OVERSHOOT_CONFIG"/>
<Register RegisterValue="0x00000001" RegisterLogicalAddress="0x08" RegisterName="CLIF_TRANSCEIVE_CONTROL"/>
<Register RegisterValue="0x00002289" RegisterLogicalAddress="0x15" RegisterName="CLIF_SS_TX_CFG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0C" RegisterName="CLIF_TX_SYMBOL23_MOD"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x0D" RegisterName="CLIF_TX_SYMBOL23_DEF"/>
<Register RegisterValue="0x00000084" RegisterLogicalAddress="0x10" RegisterName="CLIF_TX_DATA_MOD"/>
</Protocol>

-<Protocol ProtocolOffset="0x506" ProtocolIndex="0x80" ProtocolName="RX ISO14443A 106">
<Register RegisterValue="0x0000E407" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x000000FC" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00A0202" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x09BD307F" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x500800B0" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x0810203F" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00080808" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889138" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00E63400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xED4D24A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x0C0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x7B75FFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x313F51AA" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x4A8B60A7" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x57E" ProtocolIndex="0x81" ProtocolName="RX ISO14443A 212">
<Register RegisterValue="0x0000E407" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
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<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00003939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x10F8024C" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000055" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400800C0" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x8A866150" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x5F6" ProtocolIndex="0x82" ProtocolName="RX ISO14443A 424">
<Register RegisterValue="0x0000E407" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00003939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x14F80228" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000055" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x401000D0" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x88046548" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x66E" ProtocolIndex="0x83" ProtocolName="RX ISO14443A 848">
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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>  
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>  
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>  
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>  
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>  
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>  
<Register RegisterValue="0x28F80209" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>  
<Register RegisterValue="0x00000055" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>  
<Register RegisterValue="0x401000E0" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>  
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>  
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>  
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>  
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>  
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>  
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>  
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>  
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>  
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>  
<Register RegisterValue="0x2A8FFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>  
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>  
<Register RegisterValue="0x40026508" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>  
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>  
</Protocol>
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-<Protocol ProtocolOffset="0x6E6" ProtocolIndex="0x84" ProtocolName="RX ISO14443B 106">  
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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>  
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>  
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>  
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>  
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>  
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>  
<Register RegisterValue="0x3E380248" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>  
<Register RegisterValue="0x00000045" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>  
<Register RegisterValue="0x400000B6" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>  
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>  
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>  
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>  
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>  
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>  
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>  
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>  
<Register RegisterValue="0xED4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>  
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>  
<Register RegisterValue="0x2A8FFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>  
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>  
<Register RegisterValue="0x95086250" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>  
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
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-<Protocol ProtocolOffset="0x75E" ProtocolIndex="0x85" ProtocolName="RX ISO14443B 212">
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x000000FC" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x10380248" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000045" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400000C6" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x0C0F7C1F" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x94866248" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
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-<Protocol ProtocolOffset="0x7D6" ProtocolIndex="0x86" ProtocolName="RX ISO14443B 424">
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x000000FC" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x20380248" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000045" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400000D6" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x0C0F7C1F" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
</Protocol>
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<Register RegisterValue="0x94046650" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x84E" ProtocolIndex="0x87" ProtocolName="RX ISO14443B 848">
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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x0A380209" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000045" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400000E6" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D23400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x5C026608" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x8C6" ProtocolIndex="0x88" ProtocolName="RX Felica 212">
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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x10780203" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000055" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x110000C4" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x0088D238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D27400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xED4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
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<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x01806100" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x93E" ProtocolIndex="0x89" ProtocolName="RX Felica 424">
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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x10780203" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000055" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x010000D4" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x1F200000" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x01B0618E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x0088D238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00D27400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xED4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x2A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x48826548" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x9B6" ProtocolIndex="0x8A" ProtocolName="RX ISO15693 6P6">
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
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<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815307D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x40080088" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>

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<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0xDB0660FF" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
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</Protocol>

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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
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<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
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<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815307D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x40080098" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
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<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
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<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815307D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400800A8" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>

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<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00E63400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xED4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
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<Register RegisterValue="0x6A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x432B609F" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
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-<Protocol ProtocolOffset="0xB1E" ProtocolIndex="0x8D" ProtocolName="RX ISO15693 Plutus 106">
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
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<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815307D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x401000B8" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
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<Register RegisterValue="0x00E63400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xED4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x42A2689F" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815307D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x401800C8" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x0C082155" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
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<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
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<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00E63400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F518A" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x422C689F" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815077D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x000017FF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
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<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00E63400" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFF" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x393F5194" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x6B3B60AB" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

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<Register RegisterValue="0x000000F4" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x000A0200" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x0815077D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x000017FF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x0D81830E" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00889238" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
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<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFE" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
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<Register RegisterValue="0x23406053" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
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</Protocol>

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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
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<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
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<Register RegisterValue="0x01000008" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
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<Register RegisterValue="0x0815077D" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x400800BA" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x000017FF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
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<Register RegisterValue="0x000A85CC" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
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<Register RegisterValue="0xAD4C64A4" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0xC0F7C1F0" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x6A8FFFFE" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
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<Register RegisterValue="0x6ABB60AB" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
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</Protocol>

-<Protocol ProtocolOffset="0xD76" ProtocolIndex="0x92" ProtocolName="RX ISO180003m3 Manch424_2_212">
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<Register RegisterValue="0x0044893E" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00024820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x00000FC0" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00D03939" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
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<Register RegisterValue="0x401000CC" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
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<Register RegisterValue="0x6A3264AB" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x1FE00001" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0xDEE" ProtocolIndex="0x93" ProtocolName="RX ISO14443A-PICC 106">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x00100032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000B1" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x000037FF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0xB79600A0" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0xE66" ProtocolIndex="0x94" ProtocolName="RX ISO14443A-PICC 212">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x00000032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>

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<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000C1" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0xB9790A0" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0xEDE" ProtocolIndex="0x95" ProtocolName="RX ISO14443A-PICC 424">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x00000032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000D1" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0xB9790A0" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0xF56" ProtocolIndex="0x96" ProtocolName="RX ISO14443A-PICC 848">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
<Register RegisterValue="0x00000032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>

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<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000E1" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0xB79700A0" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0xFCE" ProtocolIndex="0x97" ProtocolName="RX NFC-PT-212 212">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
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<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000C5" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x20100000" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

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-<Protocol ProtocolOffset="0x1046" ProtocolIndex="0x98" ProtocolName="RX NFC-PT-424 424">  
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<Register RegisterValue="0x00100032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>  
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>  
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>  
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>  
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>  
<Register RegisterValue="0x000000D5" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>  
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>  
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>  
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>  
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</Protocol>
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-<Protocol ProtocolOffset="0x10BE" ProtocolIndex="0x99" ProtocolName="RX NFC-AT-106 106">  
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<Register RegisterValue="0x00100032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>  
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>  
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>  
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>  
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>  
<Register RegisterValue="0x000000B1" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>  
<Register RegisterValue="0x000037FF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>  
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>  
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>  
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2F" RegisterName="CLIF_DGRM_HF_ATT"/>  
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>  
<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
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<Register RegisterValue="0xB79600A0" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
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<Register RegisterValue="0x00100032" RegisterLogicalAddress="0x33" RegisterName="CLIF_DCOC_CONFIG"/>
<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
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<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
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<Register RegisterValue="0x000000C5" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
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<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x30" RegisterName="CLIF_DGRM_RSSI"/>
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<Register RegisterValue="0x20100000" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x11AE" ProtocolIndex="0x9B" ProtocolName="RX NFC-AT-424 424">
<Register RegisterValue="0x0700E437" RegisterLogicalAddress="0x43" RegisterName="CLIF_ANA_RX_CTRL"/>
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<Register RegisterValue="0x0004C935" RegisterLogicalAddress="0x35" RegisterName="CLIF_RXM_CTRL"/>
<Register RegisterValue="0x00A24820" RegisterLogicalAddress="0x38" RegisterName="CLIF_GCM_CONFIG2"/>
<Register RegisterValue="0x4000003F" RegisterLogicalAddress="0x39" RegisterName="CLIF_GCM_CONFIG1"/>
<Register RegisterValue="0x00A93979" RegisterLogicalAddress="0x3A" RegisterName="CLIF_GCM_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x36" RegisterName="CLIF_ANA_AGC_DCO_CTRL"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x1F" RegisterName="CLIF_SIGPRO_RM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x21" RegisterName="CLIF_SIGPRO_RM_ENABLES"/>
<Register RegisterValue="0x000000D5" RegisterLogicalAddress="0x1D" RegisterName="CLIF_SIGPRO_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x23" RegisterName="CLIF_SIGPRO_NOISE_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x24" RegisterName="CLIF_SIGPRO_NOISE_CONFIG2"/>
<Register RegisterValue="0x00003FFF" RegisterLogicalAddress="0x27" RegisterName="CLIF_RX_ERROR_CONFIG"/>
<Register RegisterValue="0x00280200" RegisterLogicalAddress="0x48" RegisterName="CLIF_RX_EMD_0_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x29" RegisterName="CLIF_SIGPRO_IIR_CONFIG1"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2A" RegisterName="CLIF_SIGPRO_IIR_CONFIG0"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2B" RegisterName="CLIF_DGRM_DAC_FILTER"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2C" RegisterName="CLIF_DGRM_CONFIG"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2D" RegisterName="CLIF_DGRM_BBA"/>
<Register RegisterValue="0x00000000" RegisterLogicalAddress="0x2E" RegisterName="CLIF_DGRM_DCO"/>
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<Register RegisterValue="0x00000003" RegisterLogicalAddress="0x22" RegisterName="CLIF_SIGPRO_RM_TECH"/>
<Register RegisterValue="0x20060200" RegisterLogicalAddress="0x37" RegisterName="CLIF_SIGPRO_CM_CONFIG"/>
</Protocol>

-<Protocol ProtocolOffset="0x1226" ProtocolIndex="0x9C" ProtocolName="RX GTM All">
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22 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.06

Firmware 2.06

```

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<Parameter Name="ArbPhaseAB_10" Offset="0x31E" Value="0x0000" />
<Parameter Name="RssiThresholdAB_11" Offset="0x320" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_11" Offset="0x322" Value="0x0000" />
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<Parameter Name="ArbPhaseAB_15" Offset="0x332" Value="0x0000" />
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<Parameter Name="ArbPhaseAB_17" Offset="0x33A" Value="0x0000" />
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<Parameter Name="ArbPhaseAB_18" Offset="0x33E" Value="0x0000" />
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<Parameter Name="RssiNbEntriesF" Offset="0x341" Value="0x16" />
<Parameter Name="RssiThresholdF_01" Offset="0x342" Value="0x2816" />
<Parameter Name="ArbPhaseF_01" Offset="0x344" Value="0x0000" />
<Parameter Name="RssiThresholdF_02" Offset="0x346" Value="0x3215" />
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<Parameter Name="ArbPhaseF_05" Offset="0x354" Value="0x0000" />
<Parameter Name="RssiThresholdF_06" Offset="0x356" Value="0x5983" />
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<Parameter Name="ArbPhaseF_09" Offset="0x364" Value="0x0000" />
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<Parameter Name="ArbPhaseF_0B" Offset="0x36C" Value="0x0000" />
<Parameter Name="RssiThresholdF_0C" Offset="0x36E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0C" Offset="0x370" Value="0x0000" />
<Parameter Name="RssiThresholdF_0D" Offset="0x372" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0D" Offset="0x374" Value="0x0000" />
<Parameter Name="RssiThresholdF_0E" Offset="0x376" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0E" Offset="0x378" Value="0x0000" />
<Parameter Name="RssiThresholdF_0F" Offset="0x37A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0F" Offset="0x37C" Value="0x0000" />
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<Parameter Name="RssiThresholdF_11" Offset="0x382" Value="0x96F9" />
<Parameter Name="ArbPhaseF_11" Offset="0x384" Value="0x0000" />
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<Parameter Name="ArbPhaseF_12" Offset="0x388" Value="0x0000" />
<Parameter Name="RssiThresholdF_13" Offset="0x38A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_13" Offset="0x38C" Value="0x0000" />
<Parameter Name="RssiThresholdF_14" Offset="0x38E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
<Parameter Name="RssiThresholdF_15" Offset="0x392" Value="0x96F9" />
<Parameter Name="ArbPhaseF_15" Offset="0x394" Value="0x0000" />
<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
<Parameter Name="ArbPhaseF_16" Offset="0x398" Value="0x0000" />
<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
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<Parameter Name="TxParamEntry_00_Tx1" Offset="0x3A3" Value="0x00" />
<Parameter Name="TxParamEntry_00_Tx2" Offset="0x3A4" Value="0x64" />
<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
<Parameter Name="TxParamEntry_04_ID" Offset="0x3AE" Value="0x44" />
<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
<Parameter Name="TxParamEntry_05_ID" Offset="0x3B1" Value="0x45" />
<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
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<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
<Parameter Name="TxParamEntry_07_ID" Offset="0x3B7" Value="0x47" />
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<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
<Parameter Name="TxParamEntry_08_ID" Offset="0x3BA" Value="0x48" />
<Parameter Name="TxParamEntry_08_Tx1" Offset="0x3BB" Value="0x00" />
<Parameter Name="TxParamEntry_08_Tx2" Offset="0x3BC" Value="0x64" />
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<Parameter Name="TxParamEntry_09_Tx1" Offset="0x3BE" Value="0x00" />
<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
<Parameter Name="TxParamEntry_0A_ID" Offset="0x3C0" Value="0x4A" />
<Parameter Name="TxParamEntry_0A_Tx1" Offset="0x3C1" Value="0x00" />
<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x5D" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
<Parameter Name="TxParamEntry_0B_Tx2" Offset="0x3C5" Value="0x56" />
<Parameter Name="TxParamEntry_0C_ID" Offset="0x3C6" Value="0x4C" />
<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
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<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x47" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x3F" />
<Parameter Name="TxParamEntry_0F_ID" Offset="0x3CF" Value="0x4F" />
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<Parameter Name="TxParamEntry_0F_Tx2" Offset="0x3D1" Value="0x37" />
<Parameter Name="TxParamEntry_10_ID" Offset="0x3D2" Value="0x50" />
<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
<Parameter Name="TxParamEntry_10_Tx2" Offset="0x3D4" Value="0x37" />
<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
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<Parameter Name="TxParamEntry_11_Tx2" Offset="0x3D7" Value="0x37" />
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<Parameter Name="TxParamEntry_12_Tx1" Offset="0x3D9" Value="0x00" />
<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x37" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
<Parameter Name="TxParamEntry_13_Tx1" Offset="0x3DC" Value="0x00" />
<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x37" />
<Parameter Name="TxParamEntry_14_ID" Offset="0x3DE" Value="0x54" />
<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
<Parameter Name="TxParamEntry_14_Tx2" Offset="0x3E0" Value="0x37" />
<Parameter Name="TxParamEntry_15_ID" Offset="0x3E1" Value="0x55" />
<Parameter Name="TxParamEntry_15_Tx1" Offset="0x3E2" Value="0x00" />
<Parameter Name="TxParamEntry_15_Tx2" Offset="0x3E3" Value="0x37" />
<Parameter Name="TxParamEntry_16_ID" Offset="0x3E4" Value="0x56" />
<Parameter Name="TxParamEntry_16_Tx1" Offset="0x3E5" Value="0x00" />
<Parameter Name="TxParamEntry_16_Tx2" Offset="0x3E6" Value="0x37" />
<Parameter Name="TxParamEntry_17_ID" Offset="0x3E7" Value="0x57" />
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<Parameter Name="TxParamEntry_39_ID" Offset="0x44D" Value="0x79" />
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<Parameter Name="TxParamEntry_39_Tx2" Offset="0x44F" Value="0x37" />
<Parameter Name="TxParamEntry_3A_ID" Offset="0x450" Value="0x7A" />
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<Parameter Name="TxParamEntry_3A_Tx2" Offset="0x452" Value="0x37" />
<Parameter Name="TxParamEntry_3B_ID" Offset="0x453" Value="0x7B" />
<Parameter Name="TxParamEntry_3B_Tx1" Offset="0x454" Value="0x00" />
<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
<Parameter Name="TxParamEntry_3C_ID" Offset="0x456" Value="0x7C" />
<Parameter Name="TxParamEntry_3C_Tx1" Offset="0x457" Value="0x00" />
<Parameter Name="TxParamEntry_3C_Tx2" Offset="0x458" Value="0x37" />
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<Parameter Name="TxParamEntry_3D_Tx1" Offset="0x45A" Value="0x00" />
<Parameter Name="TxParamEntry_3D_Tx2" Offset="0x45B" Value="0x37" />
<Parameter Name="TxParamEntry_3E_ID" Offset="0x45C" Value="0x7E" />
<Parameter Name="TxParamEntry_3E_Tx1" Offset="0x45D" Value="0x00" />
<Parameter Name="TxParamEntry_3E_Tx2" Offset="0x45E" Value="0x37" />
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<Parameter Name="TxParamEntry_3F_Tx2" Offset="0x461" Value="0x37" />
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<Parameter Name="TxParamEntry_41_Tx1" Offset="0x466" Value="0x00" />
<Parameter Name="TxParamEntry_41_Tx2" Offset="0x467" Value="0x37" />
<Parameter Name="TxParamEntry_42_ID" Offset="0x468" Value="0x7F" />
<Parameter Name="TxParamEntry_42_Tx1" Offset="0x469" Value="0x00" />
<Parameter Name="TxParamEntry_42_Tx2" Offset="0x46A" Value="0x37" />
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<Parameter Name="TxParamEntry_43_Tx1" Offset="0x46C" Value="0x00" />
<Parameter Name="TxParamEntry_43_Tx2" Offset="0x46D" Value="0x37" />
<Parameter Name="TxParamEntry_44_ID" Offset="0x46E" Value="0x7F" />
<Parameter Name="TxParamEntry_44_Tx1" Offset="0x46F" Value="0x00" />
<Parameter Name="TxParamEntry_44_Tx2" Offset="0x470" Value="0x37" />
<Parameter Name="TxParamEntry_45_ID" Offset="0x471" Value="0x7F" />
<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
<Parameter Name="TxParamEntry_45_Tx2" Offset="0x473" Value="0x37" />
<Parameter Name="TxParamEntry_46_ID" Offset="0x474" Value="0x7F" />
<Parameter Name="TxParamEntry_46_Tx1" Offset="0x475" Value="0x00" />
<Parameter Name="TxParamEntry_46_Tx2" Offset="0x476" Value="0x37" />
<Parameter Name="TxParamEntry_47_ID" Offset="0x477" Value="0x7F" />
<Parameter Name="TxParamEntry_47_Tx1" Offset="0x478" Value="0x00" />
<Parameter Name="TxParamEntry_47_Tx2" Offset="0x479" Value="0x37" />
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<Parameter Name="TxParamEntry_48_Tx1" Offset="0x47B" Value="0x00" />
<Parameter Name="TxParamEntry_48_Tx2" Offset="0x47C" Value="0x37" />
<Parameter Name="TxParamEntry_49_ID" Offset="0x47D" Value="0x7F" />
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<Parameter Name="TxParamEntry_49_Tx2" Offset="0x47F" Value="0x37" />
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<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
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<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
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<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7F" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
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<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
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<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
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<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
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<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x00FFFFFF" />
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<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
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<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
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<Region RegionName="TX_SHAPING_PROPRIETARY_CORR" RegionAccess="RW" RegionType="DATA">
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  <Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
  <Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />
  <Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
  <Parameter Name="Correction_Entry4" Offset="0xBB5" Value="0x0000" />
  <Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
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  <Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
  <Parameter Name="Correction_Entry8" Offset="0xBBD" Value="0x0000" />
  <Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
  <Parameter Name="Correction_Entry10" Offset="0xBC1" Value="0x0000" />
  <Parameter Name="Correction_Entry11" Offset="0xBC3" Value="0x0000" />
  <Parameter Name="Correction_Entry12" Offset="0xBC5" Value="0x0000" />
  <Parameter Name="Correction_Entry13" Offset="0xBC7" Value="0x0000" />
  <Parameter Name="Correction_Entry14" Offset="0xBC9" Value="0x0000" />
  <Parameter Name="Correction_Entry15" Offset="0xBCB" Value="0x0000" />
  <Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
  <Parameter Name="Correction_Entry17" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry18" Offset="0xBD1" Value="0x0000" />
  <Parameter Name="Correction_Entry19" Offset="0xBD3" Value="0x0000" />
  <Parameter Name="Correction_Entry20" Offset="0xBD5" Value="0x0000" />
  <Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
  <Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
  <Parameter Name="Correction_Entry23" Offset="0xBDB" Value="0x0000" />
  <Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
  <Parameter Name="Correction_Entry25" Offset="0xBDE" Value="0x0000" />
  <Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
  <Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
  <Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
  <Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
  <Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
  <Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
  <Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
  <Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
  <Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
  <Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
  <Parameter Name="Correction_Entry36" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry39" Offset="0xBF" Value="0x0000" />
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  <Parameter Name="Correction_Entry41" Offset="0xBF" Value="0x0000" />
  <Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
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<Region RegionName="TX_SHAPING_PROPRIETARY_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xEAE6DCCD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xFAF6F2EE" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFFFFFFFF" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xCACACACA" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xCACACAD8" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xCACACACA" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xCACACACA" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xFAF9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFDFDFC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFEFDFDFE" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>

<Region RegionName="RF_CLOCK_ACTIVE_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_ActiveInitiator" Offset="0xCA8" Value="0x20050530" />
  <Parameter Name="DPLL_GEAR_ActiveInitiator" Offset="0xCAC" Value="0x0FFDFEFF" />
</Region>

<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfNovCal" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
</Region>
```

```

<Parameter Name="CfgThreshold" Offset="0xC86" Value="0x08" />
<Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
<Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
</Region>

<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="EnableFastVDDPADischarge" Offset="0xC8F" Value="0x00" />
</Region>

<Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RmArcA_106_FDT" Offset="0xC9D" Value="0x812A805080508050C050" />
</Region>

<Region RegionName="15693_BR_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_53" Offset="0xCC5" Value="0x00000005" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_53" Offset="0xCC9" Value="0x00000044" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_106" Offset="0xCCD" Value="0x00000006" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_106" Offset="0xCD1" Value="0x00000045" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_212" Offset="0xCD5" Value="0x00008047" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_212" Offset="0xCD9" Value="0x01080006" />
</Region>

<Region RegionName="HIF_DELAY_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="HiFDelay" Offset="0xCDD" Value="0x32" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDE" Value="0x00" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
</Region>

<Region RegionName="LPCD_EXT_DCDC_GPIO_CTRL" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="IpcdExtDcdcEnable" Offset="0xCE0" Value="0x00" />
  <Parameter Name="IpcdExtDcdcDelayToOn" Offset="0xCE1" Value="0x64" />
  <Parameter Name="IpcdExtDcdcDelayToOff" Offset="0xCE2" Value="0x64" />
</Region>

<Region RegionName="IRQ_PAD_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="IrpPad_Polarity" Offset="0xCE3" Value="0x00" />
</Region>

<Region RegionName="RX_MULTIPLE_CLIF_RX_FRAMELEN_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="ClifRXFrameLen" Offset="0xCE4" Value="0x00EF0003" />
</Region>

<Region RegionName="CONFIG_RX_GUARD_TO" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RxGuardTO_Multiple" Offset="0xCE8" Value="0x01" />
</Region>

<Region RegionName="COMBINED_TB_SETTINGS" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DigitalTBSignalIndex" Offset="0xCE9" Value="0x9B" />
  <Parameter Name="DigitalTBSignalBit" Offset="0xCEA" Value="0x04" />
  <Parameter Name="AnalogTBSignal" Offset="0xCEB" Value="0x78" />
</Region>

<Region RegionName="RegisterValuePair" RegionOffset="0x74" RegionType="PROTOCOL" RegionAccess="INDIRECT">
  <Protocol ProtocolName="TX_ISO14443A_106" ProtocolIndex="0x00" ProtocolOffset="0x74">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00003D41"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00220104"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00220104"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_212" ProtocolIndex="0x01" ProtocolOffset="0xA1">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00110105"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00110105"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_424" ProtocolIndex="0x02" ProtocolOffset="0xCE">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00060106"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00060106"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_848" ProtocolIndex="0x03" ProtocolOffset="0xFB">
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    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x0020107"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
  </Protocol>

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```
<Register RegisterName="CLIF_DGRM_RSSI" RegisterLogicalAddress="0x30" RegisterValue="0x393F518A"></Register>
<Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x95086250"></Register>
<Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x1FE00001"></Register>
</Protocol>
</Region>
</EEPROM>
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## 23 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.06 - EMVC<sub>0</sub> optimized

**Firmware 2.06**

```
<?xml version="1.0" encoding="utf-8"?>
<EEPROM>
  <Region RegionName="USER_PMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PwrConfig" Offset="0x00" Value="0xE4" />
    <Parameter Name="DcdcConfig" Offset="0x01" Value="0x31" />
    <Parameter Name="TxLdoConfig" Offset="0x02" Value="0xFFFFAEA7" />
    <Parameter Name="TxLdoVddpaHigh" Offset="0x06" Value="0x00" />
    <Parameter Name="TxLdoVddpaLow" Offset="0x07" Value="0x00" />
    <Parameter Name="TxLdoVddpaMaxRdr" Offset="0x08" Value="0x2A" />
    <Parameter Name="TxLdoVddpaMaxCard" Offset="0x09" Value="0x2A" />
    <Parameter Name="BoostDefaultVoltage" Offset="0x0A" Value="0x1D" />
  </Region>

  <Region RegionName="CLKGEN" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="XtalConfig" Offset="0x10" Value="0x00" />
    <Parameter Name="XtalTimeOut" Offset="0x11" Value="0xFF" />
  </Region>

  <Region RegionName="RF_CLOCK_CFG" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PLLClkInputFrq" Offset="0x12" Value="0x08" />
    <Parameter Name="XtalCheckDelay" Offset="0x13" Value="0xF6" />
  </Region>

  <Region RegionName="USER_SMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="TempWarning" Offset="0x14" Value="0x99" />
    <Parameter Name="EnableGpio0OnOverTemp" Offset="0x16" Value="0x01" />
  </Region>

  <Region RegionName="RM_TECHNO_TX_SHAPING" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="ResidualAmplitudeLevel_A106" Offset="0x22" Value="0x00" />
    <Parameter Name="EdgeType_A106" Offset="0x23" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A106" Offset="0x24" Value="0x64" />
    <Parameter Name="EdgeLength_A106" Offset="0x25" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A212" Offset="0x26" Value="0x00" />
    <Parameter Name="EdgeType_A212" Offset="0x27" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A212" Offset="0x28" Value="0x44" />
    <Parameter Name="EdgeLength_A212" Offset="0x29" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A424" Offset="0x2A" Value="0x00" />
    <Parameter Name="EdgeType_A424" Offset="0x2B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A424" Offset="0x2C" Value="0x24" />
    <Parameter Name="EdgeLength_A424" Offset="0x2D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A848" Offset="0x2E" Value="0x00" />
    <Parameter Name="EdgeType_A848" Offset="0x2F" Value="0x11" />
    <Parameter Name="EdgeStyleConfiguration_A848" Offset="0x30" Value="0x18" />
    <Parameter Name="EdgeLength_A848" Offset="0x31" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B106" Offset="0x32" Value="0xC8" />
    <Parameter Name="EdgeType_B106" Offset="0x33" Value="0x44" />
    <Parameter Name="EdgeStyleConfiguration_B106" Offset="0x34" Value="0x00" />
    <Parameter Name="EdgeLength_B106" Offset="0x35" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B212" Offset="0x36" Value="0xCF" />
    <Parameter Name="EdgeType_B212" Offset="0x37" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B212" Offset="0x38" Value="0x66" />
    <Parameter Name="EdgeLength_B212" Offset="0x39" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B424" Offset="0x3A" Value="0xCF" />
    <Parameter Name="EdgeType_B424" Offset="0x3B" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B424" Offset="0x3C" Value="0x55" />
    <Parameter Name="EdgeLength_B424" Offset="0x3D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B848" Offset="0x3E" Value="0xCE" />
    <Parameter Name="EdgeType_B848" Offset="0x3F" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B848" Offset="0x40" Value="0x34" />
    <Parameter Name="EdgeLength_B848" Offset="0x41" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_F212" Offset="0x42" Value="0xCF" />
    <Parameter Name="EdgeType_F212" Offset="0x43" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_F212" Offset="0x44" Value="0x65" />
    <Parameter Name="EdgeLength_F212" Offset="0x45" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_F424" Offset="0x46" Value="0xCE" />
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    <Parameter Name="EdgeStyleConfiguration_F424" Offset="0x48" Value="0x55" />
    <Parameter Name="EdgeLength_F424" Offset="0x49" Value="0x10" />
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    <Parameter Name="EdgeType_V100_26" Offset="0x4B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_26" Offset="0x4C" Value="0x66" />
    <Parameter Name="EdgeLength_V100_26" Offset="0x4D" Value="0x10" />
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    <Parameter Name="EdgeStyleConfiguration_V100_53" Offset="0x50" Value="0x66" />
    <Parameter Name="EdgeLength_V100_53" Offset="0x51" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_106" Offset="0x52" Value="0x00" />
    <Parameter Name="EdgeType_V100_106" Offset="0x53" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_106" Offset="0x54" Value="0x66" />
    <Parameter Name="EdgeLength_V100_106" Offset="0x55" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_212" Offset="0x56" Value="0x00" />
    <Parameter Name="EdgeType_V100_212" Offset="0x57" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_212" Offset="0x58" Value="0x22" />
    <Parameter Name="EdgeLength_V100_212" Offset="0x59" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V10_26" Offset="0x5A" Value="0xC0" />
    <Parameter Name="EdgeType_V10_26" Offset="0x5B" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_V10_26" Offset="0x5C" Value="0x66" />
    <Parameter Name="EdgeLength_V10_26" Offset="0x5D" Value="0x10" />
  </Region>
</EEPROM>
```

```

<Parameter Name="ResidualAmplitudeLevel_V10_53" Offset="0x5E" Value="0xC0" />
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<Parameter Name="EdgeStyleConfiguration_V10_53" Offset="0x60" Value="0x23" />
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<Parameter Name="ResidualAmplitudeLevel_V10_106" Offset="0x62" Value="0xC0" />
<Parameter Name="EdgeType_V10_106" Offset="0x63" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_106" Offset="0x64" Value="0x23" />
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<Parameter Name="EdgeType_V10_212" Offset="0x67" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_212" Offset="0x68" Value="0x23" />
<Parameter Name="EdgeLength_V10_212" Offset="0x69" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_180003m3_tari18p88" Offset="0x6A" Value="0xC0" />
<Parameter Name="EdgeType_180003m3_tari18p88" Offset="0x6B" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_180003m3_tari18p88" Offset="0x6C" Value="0x66" />
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<Parameter Name="ResidualAmplitudeLevel_B_prime106" Offset="0x72" Value="0xCF" />
<Parameter Name="EdgeType_B_prime106" Offset="0x73" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_B_prime106" Offset="0x74" Value="0x67" />
<Parameter Name="EdgeLength_B_prime106" Offset="0x75" Value="0x10" />
</Region>

<Region RegionName="DPC SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="DPC_CONFIG" Offset="0x76" Value="0x77" />
<Parameter Name="DPC_TARGET_CURRENT" Offset="0x77" Value="0x0132" />
<Parameter Name="DPC_HYSTERESIS_LOADING" Offset="0x79" Value="0x14" />
<Parameter Name="DPC_HYSTERESIS_UNLOADING" Offset="0x7C" Value="0x0A" />
<Parameter Name="DPC_TXLDOVDDPAw" Offset="0x7D" Value="0x07" />
<Parameter Name="DPC_TXGSN" Offset="0x7E" Value="0x03" />
<Parameter Name="DPC_RDON_Control" Offset="0x7F" Value="0x01" />
<Parameter Name="DPC_InitialRDON_RFOw" Offset="0x80" Value="0x03" />
<Parameter Name="DPC_GAURD_TIME" Offset="0x87" Value="0xFF" />
<Parameter Name="DPC_ENABLE_DURING_FDT" Offset="0x88" Value="0x01" />
<Parameter Name="DPC_GAURD_TIME_AFTER_RX" Offset="0x89" Value="0x01" />
<Parameter Name="Entry_00" Offset="0x8B" Value="0x0000137F" />
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<Parameter Name="Entry_33" Offset="0x10F" Value="0x0000006A" />
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<Parameter Name="Entry_35" Offset="0x117" Value="0x00000066" />
<Parameter Name="Entry_36" Offset="0x11B" Value="0x00000057" />
<Parameter Name="Entry_37" Offset="0x11F" Value="0x0000004B" />
<Parameter Name="Entry_38" Offset="0x123" Value="0x0000003F" />
<Parameter Name="Entry_39" Offset="0x127" Value="0x0000002D" />
<Parameter Name="Entry_40" Offset="0x12B" Value="0x00000000" />
<Parameter Name="Entry_41" Offset="0x12E" Value="0x00000000" />
<Parameter Name="Entry_42" Offset="0x133" Value="0x00000000" />
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<Region RegionName="ARC SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="ArcConfig" Offset="0x137" Value="0x0064" />
<Parameter Name="ArcVddpa" Offset="0x139" Value="0x2A24130E07" />
<Parameter Name="RmArcA_106" Offset="0x13E" Value="0x81348015802A8220C250" />
<Parameter Name="RmArcA_212" Offset="0x148" Value="0x001A00200030007F407E" />
<Parameter Name="RmArcA_424" Offset="0x152" Value="0x001A00200040007F407E" />
<Parameter Name="RmArcA_848" Offset="0x15C" Value="0x001A00200040007F407E" />
<Parameter Name="RmArcB_106" Offset="0x166" Value="0x001A0020003000404050" />
<Parameter Name="RmArcB_212" Offset="0x170" Value="0x001A002000400050407E" />
<Parameter Name="RmArcB_424" Offset="0x17A" Value="0x001A002000400050407E" />
<Parameter Name="RmArcB_848" Offset="0x184" Value="0x001A002000400050407E" />
<Parameter Name="RmArcF_212" Offset="0x18E" Value="0x001A00200040007F407E" />
<Parameter Name="RmArcF_424" Offset="0x198" Value="0x001A00200040007F407E" />
<Parameter Name="RmArcV_6p6" Offset="0x1A2" Value="0x000A000A000A00A00A" />
<Parameter Name="RmArcV_26" Offset="0x1AC" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_53" Offset="0x1B6" Value="0x010A010A011F011F411F" />
<Parameter Name="RmArcV_106" Offset="0x1C0" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_212" Offset="0x1CA" Value="0x000A000A002F002F402F" />

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<Parameter Name="RmArc180003m3_SC424_4Man" Offset="0x1D4" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC424_2Man" Offset="0x1DE" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc180003m3_SC848_4Man" Offset="0x1E8" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC848_2Man" Offset="0x1F2" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc_AI_106" Offset="0x1FC" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_212" Offset="0x206" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_424" Offset="0x210" Value="0x000A000A000A000A400A" />
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<Region RegionName="RF_CLOCK_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_Default" Offset="0x2A6" Value="0x002D1327" />
  <Parameter Name="DPLL_GEAR_Default" Offset="0x2AA" Value="0x004C1FEFE" />
  <Parameter Name="DPLL_CONTROL" Offset="0x2AE" Value="0x00000C03" />
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<Region RegionName="AUTOCOLL_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RfDebounceTimeout" Offset="0x2B2" Value="0x10" />
  <Parameter Name="SensRes" Offset="0x2B3" Value="0x0042" />
  <Parameter Name="NfcID1" Offset="0x2B5" Value="0xCCBBAA" />
  <Parameter Name="SelRes" Offset="0x2B8" Value="0x60" />
  <Parameter Name="PollRes" Offset="0x2B9" Value="0xFFD08584424B0B100814119814011401FE01" />
  <Parameter Name="RandomUIDEnable" Offset="0x2CB" Value="0x00" />
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<Region RegionName="MFC_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="MfcAuthTimeout" Offset="0x2CC" Value="0x0500" />
</Region>

<Region RegionName="APC_RSSI" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RssiTimer" Offset="0x2DA" Value="0x0423" />
  <Parameter Name="RssiTimerFirstPeriod" Offset="0x2DC" Value="0x013D" />
  <Parameter Name="RssiCtrl_00_AB" Offset="0x2DE" Value="0x09" />
  <Parameter Name="RssiNbEntriesAB" Offset="0x2DF" Value="0x16" />
  <Parameter Name="RssiThresholdAB_01" Offset="0x2E0" Value="0x2816" />
  <Parameter Name="ArbPhaseAB_01" Offset="0x2E2" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_02" Offset="0x2E4" Value="0x3215" />
  <Parameter Name="ArbPhaseAB_02" Offset="0x2E6" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_03" Offset="0x2E8" Value="0x3B6E" />
  <Parameter Name="ArbPhaseAB_03" Offset="0x2EA" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_04" Offset="0x2EC" Value="0x456A" />
  <Parameter Name="ArbPhaseAB_04" Offset="0x2EE" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_05" Offset="0x2F0" Value="0x4FDC" />
  <Parameter Name="ArbPhaseAB_05" Offset="0x2F2" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_06" Offset="0x2F4" Value="0x5983" />
  <Parameter Name="ArbPhaseAB_06" Offset="0x2F6" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_07" Offset="0x2F8" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_07" Offset="0x2FA" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_08" Offset="0x2FC" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_08" Offset="0x2FE" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_09" Offset="0x300" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_09" Offset="0x302" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0A" Offset="0x304" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0A" Offset="0x306" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0B" Offset="0x308" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0B" Offset="0x30A" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0C" Offset="0x30C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0C" Offset="0x30E" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0D" Offset="0x310" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0D" Offset="0x312" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0E" Offset="0x314" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_0E" Offset="0x316" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_0F" Offset="0x318" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_14" Offset="0x32C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_14" Offset="0x32E" Value="0x0000" />
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  <Parameter Name="RssiThresholdAB_16" Offset="0x334" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_17" Offset="0x338" Value="0x96F9" />
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  <Parameter Name="RssiThresholdAB_18" Offset="0x33C" Value="0x96F9" />
  <Parameter Name="ArbPhaseAB_18" Offset="0x33E" Value="0x0000" />
  <Parameter Name="RssiCtrl_00_F" Offset="0x340" Value="0x09" />
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  <Parameter Name="RssiThresholdF_01" Offset="0x342" Value="0x2816" />
  <Parameter Name="ArbPhaseF_01" Offset="0x344" Value="0x0000" />
  <Parameter Name="RssiThresholdF_02" Offset="0x346" Value="0x3215" />
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  <Parameter Name="RssiThresholdF_03" Offset="0x34A" Value="0x3B6E" />
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  <Parameter Name="RssiThresholdF_04" Offset="0x34E" Value="0x456A" />
  <Parameter Name="ArbPhaseF_04" Offset="0x350" Value="0x0000" />
  <Parameter Name="RssiThresholdF_05" Offset="0x352" Value="0x4FDC" />
  <Parameter Name="ArbPhaseF_05" Offset="0x354" Value="0x0000" />
  <Parameter Name="RssiThresholdF_06" Offset="0x356" Value="0x5983" />
  <Parameter Name="ArbPhaseF_06" Offset="0x358" Value="0x0000" />
  <Parameter Name="RssiThresholdF_07" Offset="0x35A" Value="0x96F9" />
  <Parameter Name="ArbPhaseF_07" Offset="0x35C" Value="0x0000" />
  <Parameter Name="RssiThresholdF_08" Offset="0x35E" Value="0x96F9" />
  <Parameter Name="ArbPhaseF_08" Offset="0x360" Value="0x0000" />
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<Parameter Name="ArbPhaseF_0F" Offset="0x37C" Value="0x0000" />
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<Parameter Name="RssiThresholdF_11" Offset="0x382" Value="0x96F9" />
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<Parameter Name="ArbPhaseF_13" Offset="0x38C" Value="0x0000" />
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<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
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<Parameter Name="ArbPhaseF_15" Offset="0x394" Value="0x0000" />
<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
<Parameter Name="ArbPhaseF_16" Offset="0x398" Value="0x0000" />
<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
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<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
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<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
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<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
<Parameter Name="TxParamEntry_06_Tx1" Offset="0x3B5" Value="0x00" />
<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
<Parameter Name="TxParamEntry_07_ID" Offset="0x3B7" Value="0x47" />
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<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
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<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
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<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x5D" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
<Parameter Name="TxParamEntry_0B_Tx2" Offset="0x3C5" Value="0x56" />
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<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
<Parameter Name="TxParamEntry_00C_Tx2" Offset="0x3C8" Value="0x4F" />
<Parameter Name="TxParamEntry_0D_ID" Offset="0x3C9" Value="0x4D" />
<Parameter Name="TxParamEntry_0D_Tx1" Offset="0x3CA" Value="0x00" />
<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x47" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
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<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x37" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
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<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x37" />
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<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
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<Parameter Name="TxParamEntry_15_Tx2" Offset="0x3E3" Value="0x37" />
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<Parameter Name="TxParamEntry_39_Tx2" Offset="0x44F" Value="0x37" />
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<Parameter Name="TxParamEntry_3A_Tx1" Offset="0x451" Value="0x00" />
<Parameter Name="TxParamEntry_3A_Tx2" Offset="0x452" Value="0x37" />
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<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
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<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
<Parameter Name="TxParamEntry_4B_ID" Offset="0x483" Value="0x7F" />
<Parameter Name="TxParamEntry_4B_Tx1" Offset="0x484" Value="0x00" />
<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7F" />
<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7F" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
<Parameter Name="dummy" Offset="0x48F" Value="0x000000" />
</Region>

<Region RegionName="LPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
</Region>

<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
</Region>

<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
</Region>

<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x00FFFFFF" />
</Region>

<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
</Region>

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<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RXIRQ_GuardTime" Offset="0x561" Value="0x000F4240" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_CORR" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Correction_Entry0" Offset="0xBAD" Value="0x0000" />
  <Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
  <Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />
  <Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
  <Parameter Name="Correction_Entry4" Offset="0xBB5" Value="0x0000" />
  <Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
  <Parameter Name="Correction_Entry6" Offset="0xBB9" Value="0x0000" />
  <Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
  <Parameter Name="Correction_Entry8" Offset="0xBBD" Value="0x0000" />
  <Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
  <Parameter Name="Correction_Entry10" Offset="0xBC1" Value="0x0000" />
  <Parameter Name="Correction_Entry11" Offset="0xBC3" Value="0x0000" />
  <Parameter Name="Correction_Entry12" Offset="0xBC5" Value="0x0000" />
  <Parameter Name="Correction_Entry13" Offset="0xBC7" Value="0x0000" />
  <Parameter Name="Correction_Entry14" Offset="0xBC9" Value="0x0000" />
  <Parameter Name="Correction_Entry15" Offset="0xBCB" Value="0x0000" />
  <Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
  <Parameter Name="Correction_Entry17" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry18" Offset="0xBD1" Value="0x0000" />
  <Parameter Name="Correction_Entry19" Offset="0xBD3" Value="0x0000" />
  <Parameter Name="Correction_Entry20" Offset="0xBD5" Value="0x0000" />
  <Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
  <Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
  <Parameter Name="Correction_Entry23" Offset="0xBDB" Value="0x0000" />
  <Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
  <Parameter Name="Correction_Entry25" Offset="0xBDF" Value="0x0000" />
  <Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
  <Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
  <Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
  <Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
  <Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
  <Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
  <Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
  <Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
  <Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
  <Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
  <Parameter Name="Correction_Entry36" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry39" Offset="0xBFB" Value="0x0000" />
  <Parameter Name="Correction_Entry40" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry41" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xD9D9D3CD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xF1EEEE55" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFDFAF7F4" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xE7EDF3F9" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xD4D8DBE1" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xC8CACDD1" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xC7C7C7C7" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xFAP9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFD9DFC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFEFFFFFF" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY_4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>

<Region RegionName="RF_CLOCK_ACTIVE_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_ActiveInitiator" Offset="0xCA8" Value="0x20050530" />
  <Parameter Name="DPLL_GEAR_ActiveInitiator" Offset="0xCAC" Value="0x0FFDFEFF" />
</Region>

<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfNovCal" Offset="0xC83" Value="0x42" />

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<Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
<Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
<Parameter Name="CfgThreshold" Offset="0xC86" Value="0x08" />
<Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
<Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
</Region>

<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="EnableFastVDDPADischarge" Offset="0xC8F" Value="0x00" />
</Region>

<Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RmArcA_106_FDT" Offset="0xC9D" Value="0x8040804080608060C060" />
</Region>

<Region RegionName="15693_BR_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_53" Offset="0xCC5" Value="0x00000005" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_53" Offset="0xCC9" Value="0x00000044" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_106" Offset="0xCCE" Value="0x00000006" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_106" Offset="0xCD1" Value="0x00000045" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_212" Offset="0xCD5" Value="0x00008047" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_212" Offset="0xCD9" Value="0x01080006" />
</Region>

<Region RegionName="HIF_DELAY_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="HiFDelay" Offset="0xCDD" Value="0x32" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CardModeUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CardModeUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
</Region>

<Region RegionName="LPCD_EXT_DCDC_GPIO_CTRL" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="LpcdExtDcdcEnable" Offset="0xCE0" Value="0x00" />
  <Parameter Name="LpcdExtDcdcDelayToOn" Offset="0xCE1" Value="0x64" />
  <Parameter Name="LpcdExtDcdcDelayToOff" Offset="0xCE2" Value="0x64" />
</Region>

<Region RegionName="IRQ_PAD_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="IrqPad_Polarity" Offset="0xCE3" Value="0x00" />
</Region>

<Region RegionName="RX_MULTIPLE_CLIF_RX_FRAMELEN_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="ClifRxFramLen" Offset="0xCE4" Value="0x00EF0003" />
</Region>

<Region RegionName="CONFIG_RX_GUARD_TO" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RxGuardTO_Multiple" Offset="0xCE8" Value="0x01" />
</Region>

<Region RegionName="COMBINED_TB_SETTINGS" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DigitalTBSignalIndex" Offset="0xCE9" Value="0x9B" />
  <Parameter Name="DigitalTBSignalBit" Offset="0xCEA" Value="0x04" />
  <Parameter Name="AnalogTBSignal" Offset="0xCEB" Value="0x78" />
</Region>

<Region RegionName="RegisterValuePair" RegionOffset="0x74" RegionType="PROTOCOL" RegionAccess="INDIRECT">
  <Protocol ProtocolName="TX_ISO14443A_106" ProtocolIndex="0x00" ProtocolOffset="0x74">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000F00FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00003D41"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00220104"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00220104"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_212" ProtocolIndex="0x01" ProtocolOffset="0xA1">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00110105"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00110105"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_424" ProtocolIndex="0x02" ProtocolOffset="0xCE">
    <Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00060106"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00060106"></Register>
  </Protocol>
  <Protocol ProtocolName="TX_ISO14443A_848" ProtocolIndex="0x03" ProtocolOffset="0xFB">
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    <Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
    <Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
  </Protocol>

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<Register RegisterName="CLIF_DGRM_DCO" RegisterLogicalAddress="0x2E" RegisterValue="0xC0F7C1F0"></Register>
<Register RegisterName="CLIF_DGRM_HF_ATT" RegisterLogicalAddress="0x2F" RegisterValue="0x2A8FFFFFF"></Register>
<Register RegisterName="CLIF_DGRM_RSSI" RegisterLogicalAddress="0x30" RegisterValue="0x393F518A"></Register>
<Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x95086250"></Register>
<Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x1FE00001"></Register>
  </Protocol>
</Region>
</EEPROM>
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24 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.07

Firmware 2.07

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<?xml version="1.0" encoding="utf-8"?>
<EEPROM>
  <Region RegionName="USER_PMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PwrConfig" Offset="0x00" Value="0xE4" />
    <Parameter Name="DcdcConfig" Offset="0x01" Value="0x31" />
    <Parameter Name="TxLdoConfig" Offset="0x02" Value="0xFFFFAE7" />
    <Parameter Name="TxLdoVddpaHigh" Offset="0x06" Value="0x00" />
    <Parameter Name="TxLdoVddpaLow" Offset="0x07" Value="0x00" />
    <Parameter Name="TxLdoVddpaMaxRdx" Offset="0x08" Value="0x2A" />
    <Parameter Name="TxLdoVddpaMaxCard" Offset="0x09" Value="0x2A" />
    <Parameter Name="BoostDefaultVoltage" Offset="0x0A" Value="0x1D" />
  </Region>
  <Region RegionName="CLKGEN" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="XtalConfig" Offset="0x10" Value="0x00" />
    <Parameter Name="XtalTimeOut" Offset="0x11" Value="0xFF" />
  </Region>
  <Region RegionName="RF_CLOCK_CFG" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PLLClkInputFrq" Offset="0x12" Value="0x08" />
    <Parameter Name="XtalCheckDelay" Offset="0x13" Value="0xF6" />
  </Region>
  <Region RegionName="USER_SMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="TempWarning" Offset="0x14" Value="0x99" />
    <Parameter Name="EnableGpio0OnOverTemp" Offset="0x16" Value="0x01" />
  </Region>
  <Region RegionName="RM_TECHNO_TX_SHAPING" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="ResidualAmplitudeLevel_A106" Offset="0x22" Value="0x00" />
    <Parameter Name="EdgeType_A106" Offset="0x23" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A106" Offset="0x24" Value="0x64" />
    <Parameter Name="EdgeLength_A106" Offset="0x25" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A212" Offset="0x26" Value="0x00" />
    <Parameter Name="EdgeType_A212" Offset="0x27" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A212" Offset="0x28" Value="0x44" />
    <Parameter Name="EdgeLength_A212" Offset="0x29" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A424" Offset="0x2A" Value="0x00" />
    <Parameter Name="EdgeType_A424" Offset="0x2B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A424" Offset="0x2C" Value="0x24" />
    <Parameter Name="EdgeLength_A424" Offset="0x2D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A848" Offset="0x2E" Value="0x00" />
    <Parameter Name="EdgeType_A848" Offset="0x2F" Value="0x11" />
    <Parameter Name="EdgeStyleConfiguration_A848" Offset="0x30" Value="0x18" />
    <Parameter Name="EdgeLength_A848" Offset="0x31" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B106" Offset="0x32" Value="0xC8" />
    <Parameter Name="EdgeType_B106" Offset="0x33" Value="0x44" />
    <Parameter Name="EdgeStyleConfiguration_B106" Offset="0x34" Value="0x00" />
    <Parameter Name="EdgeLength_B106" Offset="0x35" Value="0x10" />
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    <Parameter Name="EdgeStyleConfiguration_B424" Offset="0x3C" Value="0x55" />
    <Parameter Name="EdgeLength_B424" Offset="0x3D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B848" Offset="0x3E" Value="0xCE" />
    <Parameter Name="EdgeType_B848" Offset="0x3F" Value="0x22" />
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    <Parameter Name="EdgeLength_B848" Offset="0x41" Value="0x10" />
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    <Parameter Name="EdgeType_F212" Offset="0x43" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_F212" Offset="0x44" Value="0x65" />
    <Parameter Name="EdgeLength_F212" Offset="0x45" Value="0x10" />
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    <Parameter Name="EdgeStyleConfiguration_F424" Offset="0x48" Value="0x55" />
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    <Parameter Name="EdgeType_V100_26" Offset="0x4B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_26" Offset="0x4C" Value="0x66" />
    <Parameter Name="EdgeLength_V100_26" Offset="0x4D" Value="0x10" />
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    <Parameter Name="EdgeStyleConfiguration_V100_53" Offset="0x50" Value="0x66" />
    <Parameter Name="EdgeLength_V100_53" Offset="0x51" Value="0x10" />
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    <Parameter Name="EdgeStyleConfiguration_V10_26" Offset="0x5C" Value="0x66" />
    <Parameter Name="EdgeLength_V10_26" Offset="0x5D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V10_53" Offset="0x5E" Value="0xC0" />
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<Parameter Name="DPC_HYSTERESIS_UNLOADING" Offset="0x7C" Value="0x0A" />
<Parameter Name="DPC_TXLDOVDDPAlow" Offset="0x7D" Value="0x07" />
<Parameter Name="DPC_TXGSM" Offset="0x7E" Value="0x03" />
<Parameter Name="DPC_RDON_Control" Offset="0x7F" Value="0x01" />
<Parameter Name="DPC_InitialRDON_RfOn" Offset="0x80" Value="0x03" />
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<Parameter Name="DPC_ENABLE_DURING_FDT" Offset="0x88" Value="0x01" />
<Parameter Name="DPC_GAURD_TIME_AFTER_RX" Offset="0x89" Value="0x01" />
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<Parameter Name="RmArcA_106" Offset="0x13E" Value="0x81348015802A8220C250" />
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<Parameter Name="RmArcB_424" Offset="0x17A" Value="0x001A002000400050407F" />
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<Parameter Name="RmArcF_424" Offset="0x198" Value="0x001A00200040007F407F" />
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<Parameter Name="RmArcV_26" Offset="0x1AC" Value="0x000A000A002F002F402F" />
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<Parameter Name="RmArcV_106" Offset="0x1C0" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_212" Offset="0x1CA" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArc180003m3_SC424_4Man" Offset="0x1D4" Value="0x0114011F011F001F401F" />
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  <Parameter Name="SensRes" Offset="0x2B3" Value="0x0042" />
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  <Parameter Name="SelRes" Offset="0x2B8" Value="0x60" />
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  <Parameter Name="RandomUIDEnable" Offset="0x2CB" Value="0x00" />
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<Region RegionName="MFC_CFG" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="MfcAuthTimeout" Offset="0x2CC" Value="0x0500" />
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<Region RegionName="APC_RSSI" RegionAccess="RW" RegionType="DATA">
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  <Parameter Name="RssiTimerFirstPeriod" Offset="0x2DC" Value="0x013D" />
  <Parameter Name="RssiCtrl_00_AB" Offset="0x2DE" Value="0x0C" />
  <Parameter Name="RssiNbEntriesAB" Offset="0x2DF" Value="0x16" />
  <Parameter Name="RssiThresholdAB_01" Offset="0x2E0" Value="0x2816" />
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  <Parameter Name="ArbPhaseAB_02" Offset="0x2E6" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_03" Offset="0x2E8" Value="0x3B6E" />
  <Parameter Name="ArbPhaseAB_03" Offset="0x2EA" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_04" Offset="0x2EC" Value="0x456A" />
  <Parameter Name="ArbPhaseAB_04" Offset="0x2EE" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_05" Offset="0x2F0" Value="0x4FDC" />
  <Parameter Name="ArbPhaseAB_05" Offset="0x2F2" Value="0x0000" />
  <Parameter Name="RssiThresholdAB_06" Offset="0x2F4" Value="0x5983" />
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<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
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<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
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<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x3F" />
<Parameter Name="TxParamEntry_0F_ID" Offset="0x3CF" Value="0x4F" />
<Parameter Name="TxParamEntry_0F_Tx1" Offset="0x3D0" Value="0x00" />
<Parameter Name="TxParamEntry_0F_Tx2" Offset="0x3D1" Value="0x37" />
<Parameter Name="TxParamEntry_10_ID" Offset="0x3D2" Value="0x50" />
<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
<Parameter Name="TxParamEntry_10_Tx2" Offset="0x3D4" Value="0x37" />
<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
<Parameter Name="TxParamEntry_11_Tx1" Offset="0x3D6" Value="0x00" />
<Parameter Name="TxParamEntry_11_Tx2" Offset="0x3D7" Value="0x37" />
<Parameter Name="TxParamEntry_12_ID" Offset="0x3D8" Value="0x52" />
<Parameter Name="TxParamEntry_12_Tx1" Offset="0x3D9" Value="0x00" />
<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x37" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
<Parameter Name="TxParamEntry_13_Tx1" Offset="0x3DC" Value="0x00" />
<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x37" />
<Parameter Name="TxParamEntry_14_ID" Offset="0x3DE" Value="0x54" />
<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
<Parameter Name="TxParamEntry_14_Tx2" Offset="0x3E0" Value="0x37" />
<Parameter Name="TxParamEntry_15_ID" Offset="0x3E1" Value="0x55" />
<Parameter Name="TxParamEntry_15_Tx1" Offset="0x3E2" Value="0x00" />
<Parameter Name="TxParamEntry_15_Tx2" Offset="0x3E3" Value="0x37" />
<Parameter Name="TxParamEntry_16_ID" Offset="0x3E4" Value="0x56" />
<Parameter Name="TxParamEntry_16_Tx1" Offset="0x3E5" Value="0x00" />
<Parameter Name="TxParamEntry_16_Tx2" Offset="0x3E6" Value="0x37" />
<Parameter Name="TxParamEntry_17_ID" Offset="0x3E7" Value="0x57" />
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<Parameter Name="TxParamEntry_39_ID" Offset="0x44D" Value="0x79" />
<Parameter Name="TxParamEntry_39_Tx1" Offset="0x44E" Value="0x00" />
<Parameter Name="TxParamEntry_39_Tx2" Offset="0x44F" Value="0x37" />
<Parameter Name="TxParamEntry_3A_ID" Offset="0x450" Value="0x7A" />
<Parameter Name="TxParamEntry_3A_Tx1" Offset="0x451" Value="0x00" />
<Parameter Name="TxParamEntry_3A_Tx2" Offset="0x452" Value="0x37" />
<Parameter Name="TxParamEntry_3B_ID" Offset="0x453" Value="0x7B" />
<Parameter Name="TxParamEntry_3B_Tx1" Offset="0x454" Value="0x00" />
<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
<Parameter Name="TxParamEntry_3C_ID" Offset="0x456" Value="0x7C" />
<Parameter Name="TxParamEntry_3C_Tx1" Offset="0x457" Value="0x00" />
<Parameter Name="TxParamEntry_3C_Tx2" Offset="0x458" Value="0x37" />
<Parameter Name="TxParamEntry_3D_ID" Offset="0x459" Value="0x7D" />
<Parameter Name="TxParamEntry_3D_Tx1" Offset="0x45A" Value="0x00" />
<Parameter Name="TxParamEntry_3D_Tx2" Offset="0x45B" Value="0x37" />
<Parameter Name="TxParamEntry_3E_ID" Offset="0x45C" Value="0x7E" />
<Parameter Name="TxParamEntry_3E_Tx1" Offset="0x45D" Value="0x00" />
<Parameter Name="TxParamEntry_3E_Tx2" Offset="0x45E" Value="0x37" />
<Parameter Name="TxParamEntry_3F_ID" Offset="0x45F" Value="0x7F" />
<Parameter Name="TxParamEntry_3F_Tx1" Offset="0x460" Value="0x00" />
<Parameter Name="TxParamEntry_3F_Tx2" Offset="0x461" Value="0x37" />
<Parameter Name="TxParamEntry_40_ID" Offset="0x462" Value="0x7F" />
<Parameter Name="TxParamEntry_40_Tx1" Offset="0x463" Value="0x00" />
<Parameter Name="TxParamEntry_40_Tx2" Offset="0x464" Value="0x37" />
<Parameter Name="TxParamEntry_41_ID" Offset="0x465" Value="0x7F" />
<Parameter Name="TxParamEntry_41_Tx1" Offset="0x466" Value="0x00" />
<Parameter Name="TxParamEntry_41_Tx2" Offset="0x467" Value="0x37" />
<Parameter Name="TxParamEntry_42_ID" Offset="0x468" Value="0x7F" />
<Parameter Name="TxParamEntry_42_Tx1" Offset="0x469" Value="0x00" />
<Parameter Name="TxParamEntry_42_Tx2" Offset="0x46A" Value="0x37" />
<Parameter Name="TxParamEntry_43_ID" Offset="0x46B" Value="0x7F" />
<Parameter Name="TxParamEntry_43_Tx1" Offset="0x46C" Value="0x00" />
<Parameter Name="TxParamEntry_43_Tx2" Offset="0x46D" Value="0x37" />
<Parameter Name="TxParamEntry_44_ID" Offset="0x46E" Value="0x7F" />
<Parameter Name="TxParamEntry_44_Tx1" Offset="0x46F" Value="0x00" />
<Parameter Name="TxParamEntry_44_Tx2" Offset="0x470" Value="0x37" />
<Parameter Name="TxParamEntry_45_ID" Offset="0x471" Value="0x7F" />
<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
<Parameter Name="TxParamEntry_45_Tx2" Offset="0x473" Value="0x37" />
<Parameter Name="TxParamEntry_46_ID" Offset="0x474" Value="0x7F" />
<Parameter Name="TxParamEntry_46_Tx1" Offset="0x475" Value="0x00" />
<Parameter Name="TxParamEntry_46_Tx2" Offset="0x476" Value="0x37" />
<Parameter Name="TxParamEntry_47_ID" Offset="0x477" Value="0x7F" />
<Parameter Name="TxParamEntry_47_Tx1" Offset="0x478" Value="0x00" />
<Parameter Name="TxParamEntry_47_Tx2" Offset="0x479" Value="0x37" />
<Parameter Name="TxParamEntry_48_ID" Offset="0x47A" Value="0x7F" />
<Parameter Name="TxParamEntry_48_Tx1" Offset="0x47B" Value="0x00" />
<Parameter Name="TxParamEntry_48_Tx2" Offset="0x47C" Value="0x37" />
<Parameter Name="TxParamEntry_49_ID" Offset="0x47D" Value="0x7F" />
<Parameter Name="TxParamEntry_49_Tx1" Offset="0x47E" Value="0x00" />
<Parameter Name="TxParamEntry_49_Tx2" Offset="0x47F" Value="0x37" />
<Parameter Name="TxParamEntry_4A_ID" Offset="0x480" Value="0x7F" />
<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
<Parameter Name="TxParamEntry_4B_ID" Offset="0x483" Value="0x7F" />
<Parameter Name="TxParamEntry_4B_Tx1" Offset="0x484" Value="0x00" />
<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7F" />
<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7F" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
<Parameter Name="dummy" Offset="0x48F" Value="0x000000" />
</Region>

<Region RegionName="LPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
</Region>

<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
</Region>

<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
</Region>

<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x00FFFFFF" />
</Region>

<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
<Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
</Region>

<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RXIRQ_GuardTime" Offset="0x561" Value="0x000F4240" />

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</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_CORR" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Correction_Entry0" Offset="0xBAD" Value="0x0000" />
  <Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
  <Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />
  <Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
  <Parameter Name="Correction_Entry4" Offset="0xBB5" Value="0x0000" />
  <Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
  <Parameter Name="Correction_Entry6" Offset="0xBB9" Value="0x0000" />
  <Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
  <Parameter Name="Correction_Entry8" Offset="0xBBD" Value="0x0000" />
  <Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
  <Parameter Name="Correction_Entry10" Offset="0xBC1" Value="0x0000" />
  <Parameter Name="Correction_Entry11" Offset="0xBC3" Value="0x0000" />
  <Parameter Name="Correction_Entry12" Offset="0xBC5" Value="0x0000" />
  <Parameter Name="Correction_Entry13" Offset="0xBC7" Value="0x0000" />
  <Parameter Name="Correction_Entry14" Offset="0xBC9" Value="0x0000" />
  <Parameter Name="Correction_Entry15" Offset="0xBCB" Value="0x0000" />
  <Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
  <Parameter Name="Correction_Entry17" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry18" Offset="0xBD1" Value="0x0000" />
  <Parameter Name="Correction_Entry19" Offset="0xBD3" Value="0x0000" />
  <Parameter Name="Correction_Entry20" Offset="0xBD5" Value="0x0000" />
  <Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
  <Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
  <Parameter Name="Correction_Entry23" Offset="0xBDB" Value="0x0000" />
  <Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
  <Parameter Name="Correction_Entry25" Offset="0xBDE" Value="0x0000" />
  <Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
  <Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
  <Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
  <Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
  <Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
  <Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
  <Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
  <Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
  <Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
  <Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
  <Parameter Name="Correction_Entry36" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry39" Offset="0xBF8" Value="0x0000" />
  <Parameter Name="Correction_Entry40" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry41" Offset="0xBF8" Value="0x0000" />
  <Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xD9D3CD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xF1EEBE5" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFDFAF7F4" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xE7EDF3F9" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xD4D8DBE1" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xC8CACDD1" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xC7C7C7C7" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xF9F9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFDFDFC" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFEFDFDFC" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>
<Region RegionName="TX_SHAPING_PROPRIETARY_4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>
<Region RegionName="RF_CLOCK_ACTIVE_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_ActiveInitiator" Offset="0xCA8" Value="0x20050530" />
  <Parameter Name="DPLL_GEAR_ActiveInitiator" Offset="0xCAC" Value="0x0FFDFEFF" />
</Region>
<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Cf9NovCal" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
</Region>
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<Parameter Name="CfgThreshold" Offset="0xC86" Value="0x08" />
<Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
<Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
</Region>

<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
<Parameter Name="EnableFastVDDPADischarge" Offset="0xC8F" Value="0x00" />
</Region>

<Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RmArcA_106_FDT" Offset="0xC9D" Value="0x8040804080608060C060" />
</Region>

<Region RegionName="15693_BR_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Tx_Symbol23_Mod_Reg_BR_53" Offset="0xCC5" Value="0x00000005" />
<Parameter Name="Tx_Data_Mod_Reg_BR_53" Offset="0xCC9" Value="0x00000044" />
<Parameter Name="Tx_Symbol23_Mod_Reg_BR_106" Offset="0xCCD" Value="0x00000006" />
<Parameter Name="Tx_Data_Mod_Reg_BR_106" Offset="0xCD1" Value="0x00000045" />
<Parameter Name="Tx_Symbol23_Mod_Reg_BR_212" Offset="0xCD5" Value="0x00008047" />
<Parameter Name="Tx_Data_Mod_Reg_BR_212" Offset="0xCD9" Value="0x01080006" />
</Region>

<Region RegionName="HIF_DELAY_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="HiFDelay" Offset="0xCDD" Value="0x32" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
<Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDE" Value="0x00" />
</Region>

<Region RegionName="AUTOCOLL_CFG_1" RegionAccess="RW" RegionType="DATA">
<Parameter Name="CardModUltraLowPowerEnabled" Offset="0xCDF" Value="0x00" />
</Region>

<Region RegionName="LPCD_EXT_DCDC_GPIO_CTRL" RegionAccess="RW" RegionType="DATA">
<Parameter Name="IpcdExtDcdcEnable" Offset="0xCE0" Value="0x00" />
<Parameter Name="IpcdExtDcdcDelayToOn" Offset="0xCE1" Value="0x64" />
<Parameter Name="IpcdExtDcdcDelayToOff" Offset="0xCE2" Value="0x64" />
</Region>

<Region RegionName="IRQ_PAD_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="IrpPadPolarity" Offset="0xCE3" Value="0x00" />
</Region>

<Region RegionName="RX_MULTIPLE_CLIF_RX_FRAMELEN_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="ClifRXFrameLen" Offset="0xCE4" Value="0x00EF0003" />
</Region>

<Region RegionName="CONFIG_RX_GUARD_TO" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RxGuardTO_Multiple" Offset="0xCE8" Value="0x01" />
</Region>

<Region RegionName="COMBINED_TB_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="DigitalTBSignalIndex" Offset="0xCE9" Value="0x9B" />
<Parameter Name="DigitalTBSignalBit" Offset="0xCEA" Value="0x04" />
<Parameter Name="AnalogTBSignal" Offset="0xCEB" Value="0x78" />
</Region>

<Region RegionName="ULPCD_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
<Parameter Name="UlfoTrimCalibrationCounter" Offset="0xCEC" Value="0x00" />
</Region>

<Region RegionName="RegisterValuePair" RegionOffset="0x74" RegionType="PROTOCOL" RegionAccess="INDIRECT">
<Protocol ProtocolName="TX_ISO14443A_106" ProtocolIndex="0x00" ProtocolOffset="0x74">
<Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000F00FF"></Register>
<Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00003D41"></Register>
<Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00220104"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00220104"></Register>
</Protocol>
<Protocol ProtocolName="TX_ISO14443A_212" ProtocolIndex="0x01" ProtocolOffset="0xA1">
<Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
<Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00110105"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00110105"></Register>
</Protocol>
<Protocol ProtocolName="TX_ISO14443A_424" ProtocolIndex="0x02" ProtocolOffset="0xCE">
<Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00000001"></Register>
<Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00060106"></Register>
<Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_DATA_MOD" RegisterLogicalAddress="0x10" RegisterValue="0x00060106"></Register>
</Protocol>
<Protocol ProtocolName="TX_ISO14443A_848" ProtocolIndex="0x03" ProtocolOffset="0xFB">
<Register RegisterName="CLIF_SS_TX1_CMCFG" RegisterLogicalAddress="0x3B" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_SS_TX2_CMCFG" RegisterLogicalAddress="0x3C" RegisterValue="0x000900FF"></Register>
<Register RegisterName="CLIF_TX_UNDERSHOOT_CONFIG" RegisterLogicalAddress="0x13" RegisterValue="0x00000000"></Register>
<Register RegisterName="CLIF_TX_OVERSHOOT_CONFIG" RegisterLogicalAddress="0x14" RegisterValue="0x00000000"></Register>

```























```
<Register RegisterName="CLIF_DGRM_BBA" RegisterLogicalAddress="0x2D" RegisterValue="0xED4C64A4"></Register>
<Register RegisterName="CLIF_DGRM_DCO" RegisterLogicalAddress="0x2E" RegisterValue="0xC0F7C1F0"></Register>
<Register RegisterName="CLIF_DGRM_HF_ATT" RegisterLogicalAddress="0x2F" RegisterValue="0x2A8FFFFFF"></Register>
<Register RegisterName="CLIF_DGRM_RSSI" RegisterLogicalAddress="0x30" RegisterValue="0x393F518A"></Register>
<Register RegisterName="CLIF_SIGPRO_RM_TECH" RegisterLogicalAddress="0x22" RegisterValue="0x95086250"></Register>
<Register RegisterName="CLIF_SIGPRO_CM_CONFIG" RegisterLogicalAddress="0x37" RegisterValue="0x1FE00001"></Register>
</Protocol>
</Region>
</EEPROM>
```

## 25 Appendix: EEPROM\_LOAD\_RF\_CONFIGURATION FW2.07 - EMVCo optimized

These settings are not programmed during production. They are used for the best EMVCo compliancy of the NXP customer development board.

**Firmware 2.07 EMVCo optimized**

```
<?xml version="1.0" encoding="utf-8"?>
<EEPROM>
  <Region RegionName="USER_PMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PwrConfig" Offset="0x00" Value="0xE4" />
    <Parameter Name="DcdcConfig" Offset="0x01" Value="0x31" />
    <Parameter Name="TxLdoConfig" Offset="0x02" Value="0xFFFFAEA7" />
    <Parameter Name="TxLdoVddpaHigh" Offset="0x06" Value="0x00" />
    <Parameter Name="TxLdoVddpaLow" Offset="0x07" Value="0x00" />
    <Parameter Name="TxLdoVddpaMaxRdr" Offset="0x08" Value="0x2A" />
    <Parameter Name="TxLdoVddpaMaxCard" Offset="0x09" Value="0x2A" />
    <Parameter Name="BoostDefaultVoltage" Offset="0x0A" Value="0x1D" />
  </Region>

  <Region RegionName="CLKGEN" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="XtalConfig" Offset="0x10" Value="0x00" />
    <Parameter Name="XtalTimeOut" Offset="0x11" Value="0xFF" />
  </Region>

  <Region RegionName="RF_CLOCK_CFG" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="PLLClkInputFrq" Offset="0x12" Value="0x08" />
    <Parameter Name="XtalCheckDelay" Offset="0x13" Value="0xF6" />
  </Region>

  <Region RegionName="USER_SMU" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="TempWarning" Offset="0x14" Value="0x99" />
    <Parameter Name="EnableGpio0OnOverTemp" Offset="0x16" Value="0x01" />
  </Region>

  <Region RegionName="RM_TECHNO_TX_SHAPING" RegionAccess="RW" RegionType="DATA">
    <Parameter Name="ResidualAmplitudeLevel_A106" Offset="0x22" Value="0x00" />
    <Parameter Name="EdgeType_A106" Offset="0x23" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A106" Offset="0x24" Value="0x64" />
    <Parameter Name="EdgeLength_A106" Offset="0x25" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A212" Offset="0x26" Value="0x00" />
    <Parameter Name="EdgeType_A212" Offset="0x27" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A212" Offset="0x28" Value="0x44" />
    <Parameter Name="EdgeLength_A212" Offset="0x29" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A424" Offset="0x2A" Value="0x00" />
    <Parameter Name="EdgeType_A424" Offset="0x2B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_A424" Offset="0x2C" Value="0x24" />
    <Parameter Name="EdgeLength_A424" Offset="0x2D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_A848" Offset="0x2E" Value="0x00" />
    <Parameter Name="EdgeType_A848" Offset="0x2F" Value="0x11" />
    <Parameter Name="EdgeStyleConfiguration_A848" Offset="0x30" Value="0x18" />
    <Parameter Name="EdgeLength_A848" Offset="0x31" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B106" Offset="0x32" Value="0xC8" />
    <Parameter Name="EdgeType_B106" Offset="0x33" Value="0x44" />
    <Parameter Name="EdgeStyleConfiguration_B106" Offset="0x34" Value="0x00" />
    <Parameter Name="EdgeLength_B106" Offset="0x35" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B212" Offset="0x36" Value="0xCF" />
    <Parameter Name="EdgeType_B212" Offset="0x37" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B212" Offset="0x38" Value="0x66" />
    <Parameter Name="EdgeLength_B212" Offset="0x39" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B424" Offset="0x3A" Value="0xCF" />
    <Parameter Name="EdgeType_B424" Offset="0x3B" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B424" Offset="0x3C" Value="0x55" />
    <Parameter Name="EdgeLength_B424" Offset="0x3D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_B848" Offset="0x3E" Value="0xCE" />
    <Parameter Name="EdgeType_B848" Offset="0x3F" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_B848" Offset="0x40" Value="0x34" />
    <Parameter Name="EdgeLength_B848" Offset="0x41" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_F212" Offset="0x42" Value="0xCF" />
    <Parameter Name="EdgeType_F212" Offset="0x43" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_F212" Offset="0x44" Value="0x65" />
    <Parameter Name="EdgeLength_F212" Offset="0x45" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_F424" Offset="0x46" Value="0xCE" />
    <Parameter Name="EdgeType_F424" Offset="0x47" Value="0x22" />
    <Parameter Name="EdgeStyleConfiguration_F424" Offset="0x48" Value="0x55" />
    <Parameter Name="EdgeLength_F424" Offset="0x49" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_26" Offset="0x4A" Value="0x00" />
    <Parameter Name="EdgeType_V100_26" Offset="0x4B" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_26" Offset="0x4C" Value="0x66" />
    <Parameter Name="EdgeLength_V100_26" Offset="0x4D" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_53" Offset="0x4E" Value="0x00" />
    <Parameter Name="EdgeType_V100_53" Offset="0x4F" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_53" Offset="0x50" Value="0x66" />
    <Parameter Name="EdgeLength_V100_53" Offset="0x51" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_106" Offset="0x52" Value="0x00" />
    <Parameter Name="EdgeType_V100_106" Offset="0x53" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_106" Offset="0x54" Value="0x66" />
    <Parameter Name="EdgeLength_V100_106" Offset="0x55" Value="0x10" />
    <Parameter Name="ResidualAmplitudeLevel_V100_212" Offset="0x56" Value="0x00" />
    <Parameter Name="EdgeType_V100_212" Offset="0x57" Value="0x33" />
    <Parameter Name="EdgeStyleConfiguration_V100_212" Offset="0x58" Value="0x22" />
    <Parameter Name="EdgeLength_V100_212" Offset="0x59" Value="0x10" />
  </Region>
</EEPROM>
```

```

<Parameter Name="ResidualAmplitudeLevel_V10_26" Offset="0x5A" Value="0xC0" />
<Parameter Name="EdgeType_V10_26" Offset="0x5B" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_26" Offset="0x5C" Value="0x66" />
<Parameter Name="EdgeLength_V10_26" Offset="0x5D" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_V10_53" Offset="0x5E" Value="0xC0" />
<Parameter Name="EdgeType_V10_53" Offset="0x5F" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_53" Offset="0x60" Value="0x23" />
<Parameter Name="EdgeLength_V10_53" Offset="0x61" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_V10_106" Offset="0x62" Value="0xC0" />
<Parameter Name="EdgeType_V10_106" Offset="0x63" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_106" Offset="0x64" Value="0x23" />
<Parameter Name="EdgeLength_V10_106" Offset="0x65" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_V10_212" Offset="0x66" Value="0xC0" />
<Parameter Name="EdgeType_V10_212" Offset="0x67" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_V10_212" Offset="0x68" Value="0x23" />
<Parameter Name="EdgeLength_V10_212" Offset="0x69" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_180003m3_tari18p88" Offset="0x6A" Value="0xC0" />
<Parameter Name="EdgeType_180003m3_tari18p88" Offset="0x6B" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_180003m3_tari18p88" Offset="0x6C" Value="0x66" />
<Parameter Name="EdgeLength_180003m3_tari18p88" Offset="0x6D" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_180003m3_tari9p44" Offset="0x6E" Value="0xC0" />
<Parameter Name="EdgeType_180003m3_tari9p44" Offset="0x6F" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_180003m3_tari9p44" Offset="0x70" Value="0x66" />
<Parameter Name="EdgeLength_180003m3_tari9p44" Offset="0x71" Value="0x10" />
<Parameter Name="ResidualAmplitudeLevel_B_prime106" Offset="0x72" Value="0xCF" />
<Parameter Name="EdgeType_B_prime106" Offset="0x73" Value="0x22" />
<Parameter Name="EdgeStyleConfiguration_B_prime106" Offset="0x74" Value="0x67" />
<Parameter Name="EdgeLength_B_prime106" Offset="0x75" Value="0x10" />
</Region>

<Region RegionName="DPC_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="DPC_CONFIG" Offset="0x76" Value="0x77" />
<Parameter Name="DPC_TARGET_CURRENT" Offset="0x77" Value="0x0132" />
<Parameter Name="DPC_HYSTERESIS_LOADING" Offset="0x79" Value="0x14" />
<Parameter Name="DPC_HYSTERESIS_UNLOADING" Offset="0x7C" Value="0x0A" />
<Parameter Name="DPC_TXLDOVDDPALow" Offset="0x7D" Value="0x07" />
<Parameter Name="DPC_TXGSN" Offset="0x7E" Value="0x03" />
<Parameter Name="DPC_RDON_Control" Offset="0x7F" Value="0x01" />
<Parameter Name="DPC_InitialRDON_RFOn" Offset="0x80" Value="0x03" />
<Parameter Name="DPC_GAURD_TIME" Offset="0x87" Value="0xFF" />
<Parameter Name="DPC_ENABLE_DURING_FDT" Offset="0x88" Value="0x01" />
<Parameter Name="DPC_GAURD_TIME_AFTER_RX" Offset="0x89" Value="0x01" />
<Parameter Name="Entry_00" Offset="0x8B" Value="0x0000137F" />
<Parameter Name="Entry_01" Offset="0x8F" Value="0x0000137F" />
<Parameter Name="Entry_02" Offset="0x93" Value="0x0000137F" />
<Parameter Name="Entry_03" Offset="0x97" Value="0x0000137F" />
<Parameter Name="Entry_04" Offset="0x9B" Value="0x0000137F" />
<Parameter Name="Entry_05" Offset="0x9F" Value="0x0000137F" />
<Parameter Name="Entry_06" Offset="0xA3" Value="0x0000007F" />
<Parameter Name="Entry_07" Offset="0xA7" Value="0x0000007F" />
<Parameter Name="Entry_08" Offset="0xAB" Value="0x0000007F" />
<Parameter Name="Entry_09" Offset="0xAF" Value="0x0000007F" />
<Parameter Name="Entry_10" Offset="0xB3" Value="0x0000007F" />
<Parameter Name="Entry_11" Offset="0xB7" Value="0x0000007F" />
<Parameter Name="Entry_12" Offset="0xBB" Value="0x0000007F" />
<Parameter Name="Entry_13" Offset="0xBF" Value="0x0000007F" />
<Parameter Name="Entry_14" Offset="0xC3" Value="0x0000007F" />
<Parameter Name="Entry_15" Offset="0xC7" Value="0x0000007F" />
<Parameter Name="Entry_16" Offset="0xCB" Value="0x0000007F" />
<Parameter Name="Entry_17" Offset="0xCF" Value="0x0000007F" />
<Parameter Name="Entry_18" Offset="0xD3" Value="0x0000007F" />
<Parameter Name="Entry_19" Offset="0xD7" Value="0x0000007F" />
<Parameter Name="Entry_20" Offset="0xDB" Value="0x0000007F" />
<Parameter Name="Entry_21" Offset="0xDF" Value="0x0000007F" />
<Parameter Name="Entry_22" Offset="0xE3" Value="0x0000007F" />
<Parameter Name="Entry_23" Offset="0xE7" Value="0x0000007F" />
<Parameter Name="Entry_24" Offset="0xEB" Value="0x0000007F" />
<Parameter Name="Entry_25" Offset="0xEF" Value="0x00000079" />
<Parameter Name="Entry_26" Offset="0xF3" Value="0x00000077" />
<Parameter Name="Entry_27" Offset="0xF7" Value="0x00000075" />
<Parameter Name="Entry_28" Offset="0xFB" Value="0x00000073" />
<Parameter Name="Entry_29" Offset="0xFF" Value="0x00000071" />
<Parameter Name="Entry_30" Offset="0x103" Value="0x0000006F" />
<Parameter Name="Entry_31" Offset="0x107" Value="0x0000006E" />
<Parameter Name="Entry_32" Offset="0x10B" Value="0x0000006C" />
<Parameter Name="Entry_33" Offset="0x10F" Value="0x0000006A" />
<Parameter Name="Entry_34" Offset="0x113" Value="0x00000068" />
<Parameter Name="Entry_35" Offset="0x117" Value="0x00000066" />
<Parameter Name="Entry_36" Offset="0x11B" Value="0x00000057" />
<Parameter Name="Entry_37" Offset="0x11F" Value="0x0000004B" />
<Parameter Name="Entry_38" Offset="0x123" Value="0x0000003F" />
<Parameter Name="Entry_39" Offset="0x127" Value="0x0000002D" />
<Parameter Name="Entry_40" Offset="0x12B" Value="0x00000000" />
<Parameter Name="Entry_41" Offset="0x12F" Value="0x00000000" />
<Parameter Name="Entry_42" Offset="0x133" Value="0x00000000" />
</Region>

<Region RegionName="ARC_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="ArcConfig" Offset="0x137" Value="0x0064" />
<Parameter Name="ArcVddpa" Offset="0x139" Value="0x2A24130E07" />
<Parameter Name="RmArcA_106" Offset="0x13E" Value="0x81348015802A8220C250" />
<Parameter Name="RmArcA_212" Offset="0x148" Value="0x001A00200030007F407F" />
<Parameter Name="RmArcA_424" Offset="0x152" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcA_848" Offset="0x15C" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcB_106" Offset="0x166" Value="0x001A00200030004050" />
<Parameter Name="RmArcB_212" Offset="0x170" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_424" Offset="0x17A" Value="0x001A002000400050407F" />
<Parameter Name="RmArcB_848" Offset="0x184" Value="0x001A002000400050407F" />
<Parameter Name="RmArcF_212" Offset="0x18E" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcF_424" Offset="0x198" Value="0x001A00200040007F407F" />
<Parameter Name="RmArcV_6p6" Offset="0x1A2" Value="0x000A000A000A00A400A" />

```

```

<Parameter Name="RmArcV_26" Offset="0x1AC" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_53" Offset="0x1B6" Value="0x010A010A011F011F411F" />
<Parameter Name="RmArcV_106" Offset="0x1C0" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArcV_212" Offset="0x1CA" Value="0x000A000A002F002F402F" />
<Parameter Name="RmArc180003m3_SC424_4Man" Offset="0x1D4" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC424_2Man" Offset="0x1DE" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc180003m3_SC848_4Man" Offset="0x1E8" Value="0x0114011F011F001F401F" />
<Parameter Name="RmArc180003m3_SC848_2Man" Offset="0x1F2" Value="0x0014001F003F004F404F" />
<Parameter Name="RmArc_AI_106" Offset="0x1FC" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_212" Offset="0x206" Value="0x000A000A000A000A400A" />
<Parameter Name="RmArc_AI_424" Offset="0x210" Value="0x000A000A000A000A400A" />
</Region>

<Region RegionName="RF_CLOCK_DPLL_COM" RegionAccess="RW" RegionType="DATA">
<Parameter Name="DPLL_INIT_Default" Offset="0x2A6" Value="0x002D1327" />
<Parameter Name="DPLL_GEAR_Default" Offset="0x2AA" Value="0x04C1FEFE" />
<Parameter Name="DPLL_CONTROL" Offset="0x2AE" Value="0x00000C63" />
</Region>

<Region RegionName="AUTOCOLL_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RfDebounceTimeout" Offset="0x2B2" Value="0x10" />
<Parameter Name="SensRes" Offset="0x2B3" Value="0x0042" />
<Parameter Name="NfcID1" Offset="0x2B5" Value="0xCCBBAA" />
<Parameter Name="SelRes" Offset="0x2B8" Value="0x60" />
<Parameter Name="PollRes" Offset="0x2B9" Value="0xFFD08584424B0B100814119814011401FE01" />
<Parameter Name="RandomUIDEnable" Offset="0x2CB" Value="0x00" />
</Region>

<Region RegionName="MFC_CFG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="MfcAuthTimeout" Offset="0x2CC" Value="0x0500" />
</Region>

<Region RegionName="APC_RSSI" RegionAccess="RW" RegionType="DATA">
<Parameter Name="RssiTimer" Offset="0x2DA" Value="0x0423" />
<Parameter Name="RssiTimerFirstPeriod" Offset="0x2DC" Value="0x013D" />
<Parameter Name="RssiCtrl_00_AB" Offset="0x2DE" Value="0x0C" />
<Parameter Name="RssiNbEntriesAB" Offset="0x2DF" Value="0x16" />
<Parameter Name="RssiThresholdAB_01" Offset="0x2E0" Value="0x2816" />
<Parameter Name="ArbPhaseAB_01" Offset="0x2E2" Value="0x0000" />
<Parameter Name="RssiThresholdAB_02" Offset="0x2E4" Value="0x3215" />
<Parameter Name="ArbPhaseAB_02" Offset="0x2E6" Value="0x0000" />
<Parameter Name="RssiThresholdAB_03" Offset="0x2E8" Value="0x3B6E" />
<Parameter Name="ArbPhaseAB_03" Offset="0x2EA" Value="0x0000" />
<Parameter Name="RssiThresholdAB_04" Offset="0x2EC" Value="0x456A" />
<Parameter Name="ArbPhaseAB_04" Offset="0x2EE" Value="0x0000" />
<Parameter Name="RssiThresholdAB_05" Offset="0x2F0" Value="0x4FDC" />
<Parameter Name="ArbPhaseAB_05" Offset="0x2F2" Value="0x0000" />
<Parameter Name="RssiThresholdAB_06" Offset="0x2F4" Value="0x5983" />
<Parameter Name="ArbPhaseAB_06" Offset="0x2F6" Value="0x0000" />
<Parameter Name="RssiThresholdAB_07" Offset="0x2F8" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_07" Offset="0x2FA" Value="0x0000" />
<Parameter Name="RssiThresholdAB_08" Offset="0x2FC" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_08" Offset="0x2FE" Value="0x0000" />
<Parameter Name="RssiThresholdAB_09" Offset="0x300" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_09" Offset="0x302" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0A" Offset="0x304" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0A" Offset="0x306" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0B" Offset="0x308" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0B" Offset="0x30A" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0C" Offset="0x30C" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0C" Offset="0x30E" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0D" Offset="0x310" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0D" Offset="0x312" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0E" Offset="0x314" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0E" Offset="0x316" Value="0x0000" />
<Parameter Name="RssiThresholdAB_0F" Offset="0x318" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_0F" Offset="0x31A" Value="0x0000" />
<Parameter Name="RssiThresholdAB_10" Offset="0x31C" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_10" Offset="0x31E" Value="0x0000" />
<Parameter Name="RssiThresholdAB_11" Offset="0x320" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_11" Offset="0x322" Value="0x0000" />
<Parameter Name="RssiThresholdAB_12" Offset="0x324" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_12" Offset="0x326" Value="0x0000" />
<Parameter Name="RssiThresholdAB_13" Offset="0x328" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_13" Offset="0x32A" Value="0x0000" />
<Parameter Name="RssiThresholdAB_14" Offset="0x32C" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_14" Offset="0x32E" Value="0x0000" />
<Parameter Name="RssiThresholdAB_15" Offset="0x330" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_15" Offset="0x332" Value="0x0000" />
<Parameter Name="RssiThresholdAB_16" Offset="0x334" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_16" Offset="0x336" Value="0x0000" />
<Parameter Name="RssiThresholdAB_17" Offset="0x338" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_17" Offset="0x33A" Value="0x0000" />
<Parameter Name="RssiThresholdAB_18" Offset="0x33C" Value="0x96F9" />
<Parameter Name="ArbPhaseAB_18" Offset="0x33E" Value="0x0000" />
<Parameter Name="RssiCtrl_00_F" Offset="0x340" Value="0x09" />
<Parameter Name="RssiNbEntriesF" Offset="0x341" Value="0x16" />
<Parameter Name="RssiThresholdF_01" Offset="0x342" Value="0x2816" />
<Parameter Name="ArbPhaseF_01" Offset="0x344" Value="0x0000" />
<Parameter Name="RssiThresholdF_02" Offset="0x346" Value="0x3215" />
<Parameter Name="ArbPhaseF_02" Offset="0x348" Value="0x0000" />
<Parameter Name="RssiThresholdF_03" Offset="0x34A" Value="0x3B6E" />
<Parameter Name="ArbPhaseF_03" Offset="0x34C" Value="0x0000" />
<Parameter Name="RssiThresholdF_04" Offset="0x34E" Value="0x456A" />
<Parameter Name="ArbPhaseF_04" Offset="0x350" Value="0x0000" />
<Parameter Name="RssiThresholdF_05" Offset="0x352" Value="0x4FDC" />
<Parameter Name="ArbPhaseF_05" Offset="0x354" Value="0x0000" />
<Parameter Name="RssiThresholdF_06" Offset="0x356" Value="0x5983" />
<Parameter Name="ArbPhaseF_06" Offset="0x358" Value="0x0000" />
<Parameter Name="RssiThresholdF_07" Offset="0x35A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_07" Offset="0x35C" Value="0x0000" />

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<Parameter Name="RssiThresholdF_08" Offset="0x35E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_08" Offset="0x360" Value="0x0000" />
<Parameter Name="RssiThresholdF_09" Offset="0x362" Value="0x96F9" />
<Parameter Name="ArbPhaseF_09" Offset="0x364" Value="0x0000" />
<Parameter Name="RssiThresholdF_0A" Offset="0x366" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0A" Offset="0x368" Value="0x0000" />
<Parameter Name="RssiThresholdF_0B" Offset="0x36A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0B" Offset="0x36C" Value="0x0000" />
<Parameter Name="RssiThresholdF_0C" Offset="0x36E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0C" Offset="0x370" Value="0x0000" />
<Parameter Name="RssiThresholdF_0D" Offset="0x372" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0D" Offset="0x374" Value="0x0000" />
<Parameter Name="RssiThresholdF_0E" Offset="0x376" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0E" Offset="0x378" Value="0x0000" />
<Parameter Name="RssiThresholdF_0F" Offset="0x37A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_0F" Offset="0x37C" Value="0x0000" />
<Parameter Name="RssiThresholdF_10" Offset="0x37E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_10" Offset="0x380" Value="0x0000" />
<Parameter Name="RssiThresholdF_11" Offset="0x382" Value="0x96F9" />
<Parameter Name="ArbPhaseF_11" Offset="0x384" Value="0x0000" />
<Parameter Name="RssiThresholdF_12" Offset="0x386" Value="0x96F9" />
<Parameter Name="ArbPhaseF_12" Offset="0x388" Value="0x0000" />
<Parameter Name="RssiThresholdF_13" Offset="0x38A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_13" Offset="0x38C" Value="0x0000" />
<Parameter Name="RssiThresholdF_14" Offset="0x38E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_14" Offset="0x390" Value="0x0000" />
<Parameter Name="RssiThresholdF_15" Offset="0x392" Value="0x96F9" />
<Parameter Name="ArbPhaseF_15" Offset="0x394" Value="0x0000" />
<Parameter Name="RssiThresholdF_16" Offset="0x396" Value="0x96F9" />
<Parameter Name="ArbPhaseF_16" Offset="0x398" Value="0x0000" />
<Parameter Name="RssiThresholdF_17" Offset="0x39A" Value="0x96F9" />
<Parameter Name="ArbPhaseF_17" Offset="0x39C" Value="0x0000" />
<Parameter Name="RssiThresholdF_18" Offset="0x39E" Value="0x96F9" />
<Parameter Name="ArbPhaseF_18" Offset="0x3A0" Value="0x0000" />
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<Region RegionName="APC_TX" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TxParamEntry_00_ID" Offset="0x3A2" Value="0x40" />
<Parameter Name="TxParamEntry_00_Tx1" Offset="0x3A3" Value="0x00" />
<Parameter Name="TxParamEntry_00_Tx2" Offset="0x3A4" Value="0x64" />
<Parameter Name="TxParamEntry_01_ID" Offset="0x3A5" Value="0x41" />
<Parameter Name="TxParamEntry_01_Tx1" Offset="0x3A6" Value="0x00" />
<Parameter Name="TxParamEntry_01_Tx2" Offset="0x3A7" Value="0x64" />
<Parameter Name="TxParamEntry_02_ID" Offset="0x3A8" Value="0x42" />
<Parameter Name="TxParamEntry_02_Tx1" Offset="0x3A9" Value="0x00" />
<Parameter Name="TxParamEntry_02_Tx2" Offset="0x3AA" Value="0x64" />
<Parameter Name="TxParamEntry_03_ID" Offset="0x3AB" Value="0x43" />
<Parameter Name="TxParamEntry_03_Tx1" Offset="0x3AC" Value="0x00" />
<Parameter Name="TxParamEntry_03_Tx2" Offset="0x3AD" Value="0x64" />
<Parameter Name="TxParamEntry_04_ID" Offset="0x3AE" Value="0x44" />
<Parameter Name="TxParamEntry_04_Tx1" Offset="0x3AF" Value="0x00" />
<Parameter Name="TxParamEntry_04_Tx2" Offset="0x3B0" Value="0x64" />
<Parameter Name="TxParamEntry_05_ID" Offset="0x3B1" Value="0x45" />
<Parameter Name="TxParamEntry_05_Tx1" Offset="0x3B2" Value="0x00" />
<Parameter Name="TxParamEntry_05_Tx2" Offset="0x3B3" Value="0x64" />
<Parameter Name="TxParamEntry_06_ID" Offset="0x3B4" Value="0x46" />
<Parameter Name="TxParamEntry_06_Tx1" Offset="0x3B5" Value="0x00" />
<Parameter Name="TxParamEntry_06_Tx2" Offset="0x3B6" Value="0x64" />
<Parameter Name="TxParamEntry_07_ID" Offset="0x3B7" Value="0x47" />
<Parameter Name="TxParamEntry_07_Tx1" Offset="0x3B8" Value="0x00" />
<Parameter Name="TxParamEntry_07_Tx2" Offset="0x3B9" Value="0x64" />
<Parameter Name="TxParamEntry_08_ID" Offset="0x3BA" Value="0x48" />
<Parameter Name="TxParamEntry_08_Tx1" Offset="0x3BB" Value="0x00" />
<Parameter Name="TxParamEntry_08_Tx2" Offset="0x3BC" Value="0x64" />
<Parameter Name="TxParamEntry_09_ID" Offset="0x3BD" Value="0x49" />
<Parameter Name="TxParamEntry_09_Tx1" Offset="0x3BE" Value="0x00" />
<Parameter Name="TxParamEntry_09_Tx2" Offset="0x3BF" Value="0x64" />
<Parameter Name="TxParamEntry_0A_ID" Offset="0x3C0" Value="0x4A" />
<Parameter Name="TxParamEntry_0A_Tx1" Offset="0x3C1" Value="0x00" />
<Parameter Name="TxParamEntry_0A_Tx2" Offset="0x3C2" Value="0x5D" />
<Parameter Name="TxParamEntry_0B_ID" Offset="0x3C3" Value="0x4B" />
<Parameter Name="TxParamEntry_0B_Tx1" Offset="0x3C4" Value="0x00" />
<Parameter Name="TxParamEntry_0B_Tx2" Offset="0x3C5" Value="0x56" />
<Parameter Name="TxParamEntry_0C_ID" Offset="0x3C6" Value="0x4C" />
<Parameter Name="TxParamEntry_00C_Tx1" Offset="0x3C7" Value="0x00" />
<Parameter Name="TxParamEntry_00C_Tx2" Offset="0x3C8" Value="0x4E" />
<Parameter Name="TxParamEntry_0D_ID" Offset="0x3C9" Value="0x4D" />
<Parameter Name="TxParamEntry_0D_Tx1" Offset="0x3CA" Value="0x00" />
<Parameter Name="TxParamEntry_0D_Tx2" Offset="0x3CB" Value="0x47" />
<Parameter Name="TxParamEntry_0E_ID" Offset="0x3CC" Value="0x4E" />
<Parameter Name="TxParamEntry_0E_Tx1" Offset="0x3CD" Value="0x00" />
<Parameter Name="TxParamEntry_0E_Tx2" Offset="0x3CE" Value="0x3F" />
<Parameter Name="TxParamEntry_0F_ID" Offset="0x3CF" Value="0x4F" />
<Parameter Name="TxParamEntry_0F_Tx1" Offset="0x3D0" Value="0x00" />
<Parameter Name="TxParamEntry_0F_Tx2" Offset="0x3D1" Value="0x37" />
<Parameter Name="TxParamEntry_10_ID" Offset="0x3D2" Value="0x50" />
<Parameter Name="TxParamEntry_10_Tx1" Offset="0x3D3" Value="0x00" />
<Parameter Name="TxParamEntry_10_Tx2" Offset="0x3D4" Value="0x37" />
<Parameter Name="TxParamEntry_11_ID" Offset="0x3D5" Value="0x51" />
<Parameter Name="TxParamEntry_11_Tx1" Offset="0x3D6" Value="0x00" />
<Parameter Name="TxParamEntry_11_Tx2" Offset="0x3D7" Value="0x37" />
<Parameter Name="TxParamEntry_12_ID" Offset="0x3D8" Value="0x52" />
<Parameter Name="TxParamEntry_12_Tx1" Offset="0x3D9" Value="0x00" />
<Parameter Name="TxParamEntry_12_Tx2" Offset="0x3DA" Value="0x37" />
<Parameter Name="TxParamEntry_13_ID" Offset="0x3DB" Value="0x53" />
<Parameter Name="TxParamEntry_13_Tx1" Offset="0x3DC" Value="0x00" />
<Parameter Name="TxParamEntry_13_Tx2" Offset="0x3DD" Value="0x37" />
<Parameter Name="TxParamEntry_14_ID" Offset="0x3DE" Value="0x54" />
<Parameter Name="TxParamEntry_14_Tx1" Offset="0x3DF" Value="0x00" />
<Parameter Name="TxParamEntry_14_Tx2" Offset="0x3E0" Value="0x37" />
<Parameter Name="TxParamEntry_15_ID" Offset="0x3E1" Value="0x55" />
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<Parameter Name="TxParamEntry_37_ID" Offset="0x447" Value="0x77" />
<Parameter Name="TxParamEntry_37_Tx1" Offset="0x448" Value="0x00" />
<Parameter Name="TxParamEntry_37_Tx2" Offset="0x449" Value="0x37" />
<Parameter Name="TxParamEntry_38_ID" Offset="0x44A" Value="0x78" />
<Parameter Name="TxParamEntry_38_Tx1" Offset="0x44B" Value="0x00" />
<Parameter Name="TxParamEntry_38_Tx2" Offset="0x44C" Value="0x37" />
<Parameter Name="TxParamEntry_39_ID" Offset="0x44D" Value="0x79" />
<Parameter Name="TxParamEntry_39_Tx1" Offset="0x44E" Value="0x00" />
<Parameter Name="TxParamEntry_39_Tx2" Offset="0x44F" Value="0x37" />
<Parameter Name="TxParamEntry_3A_ID" Offset="0x450" Value="0x7A" />
<Parameter Name="TxParamEntry_3A_Tx1" Offset="0x451" Value="0x00" />
<Parameter Name="TxParamEntry_3A_Tx2" Offset="0x452" Value="0x37" />
<Parameter Name="TxParamEntry_3B_ID" Offset="0x453" Value="0x7B" />
<Parameter Name="TxParamEntry_3B_Tx1" Offset="0x454" Value="0x00" />
<Parameter Name="TxParamEntry_3B_Tx2" Offset="0x455" Value="0x37" />
<Parameter Name="TxParamEntry_3C_ID" Offset="0x456" Value="0x7C" />
<Parameter Name="TxParamEntry_3C_Tx1" Offset="0x457" Value="0x00" />
<Parameter Name="TxParamEntry_3C_Tx2" Offset="0x458" Value="0x37" />
<Parameter Name="TxParamEntry_3D_ID" Offset="0x459" Value="0x7D" />
<Parameter Name="TxParamEntry_3D_Tx1" Offset="0x45A" Value="0x00" />
<Parameter Name="TxParamEntry_3D_Tx2" Offset="0x45B" Value="0x37" />
<Parameter Name="TxParamEntry_3E_ID" Offset="0x45C" Value="0x7E" />
<Parameter Name="TxParamEntry_3E_Tx1" Offset="0x45D" Value="0x00" />
<Parameter Name="TxParamEntry_3E_Tx2" Offset="0x45E" Value="0x37" />
<Parameter Name="TxParamEntry_3F_ID" Offset="0x45F" Value="0x7F" />
<Parameter Name="TxParamEntry_3F_Tx1" Offset="0x460" Value="0x00" />
<Parameter Name="TxParamEntry_3F_Tx2" Offset="0x461" Value="0x37" />
<Parameter Name="TxParamEntry_40_ID" Offset="0x462" Value="0x7F" />
<Parameter Name="TxParamEntry_40_Tx1" Offset="0x463" Value="0x00" />
<Parameter Name="TxParamEntry_40_Tx2" Offset="0x464" Value="0x37" />
<Parameter Name="TxParamEntry_41_ID" Offset="0x465" Value="0x7F" />
<Parameter Name="TxParamEntry_41_Tx1" Offset="0x466" Value="0x00" />
<Parameter Name="TxParamEntry_41_Tx2" Offset="0x467" Value="0x37" />
<Parameter Name="TxParamEntry_42_ID" Offset="0x468" Value="0x7F" />
<Parameter Name="TxParamEntry_42_Tx1" Offset="0x469" Value="0x00" />
<Parameter Name="TxParamEntry_42_Tx2" Offset="0x46A" Value="0x37" />
<Parameter Name="TxParamEntry_43_ID" Offset="0x46B" Value="0x7F" />
<Parameter Name="TxParamEntry_43_Tx1" Offset="0x46C" Value="0x00" />
<Parameter Name="TxParamEntry_43_Tx2" Offset="0x46D" Value="0x37" />
<Parameter Name="TxParamEntry_44_ID" Offset="0x46E" Value="0x7F" />
<Parameter Name="TxParamEntry_44_Tx1" Offset="0x46F" Value="0x00" />
<Parameter Name="TxParamEntry_44_Tx2" Offset="0x470" Value="0x37" />
<Parameter Name="TxParamEntry_45_ID" Offset="0x471" Value="0x7F" />
<Parameter Name="TxParamEntry_45_Tx1" Offset="0x472" Value="0x00" />
<Parameter Name="TxParamEntry_45_Tx2" Offset="0x473" Value="0x37" />
<Parameter Name="TxParamEntry_46_ID" Offset="0x474" Value="0x7F" />
<Parameter Name="TxParamEntry_46_Tx1" Offset="0x475" Value="0x00" />
<Parameter Name="TxParamEntry_46_Tx2" Offset="0x476" Value="0x37" />
<Parameter Name="TxParamEntry_47_ID" Offset="0x477" Value="0x7F" />
<Parameter Name="TxParamEntry_47_Tx1" Offset="0x478" Value="0x00" />
<Parameter Name="TxParamEntry_47_Tx2" Offset="0x479" Value="0x37" />
<Parameter Name="TxParamEntry_48_ID" Offset="0x47A" Value="0x7F" />
<Parameter Name="TxParamEntry_48_Tx1" Offset="0x47B" Value="0x00" />
<Parameter Name="TxParamEntry_48_Tx2" Offset="0x47C" Value="0x37" />
<Parameter Name="TxParamEntry_49_ID" Offset="0x47D" Value="0x7F" />
<Parameter Name="TxParamEntry_49_Tx1" Offset="0x47E" Value="0x00" />
<Parameter Name="TxParamEntry_49_Tx2" Offset="0x47F" Value="0x37" />
<Parameter Name="TxParamEntry_4A_ID" Offset="0x480" Value="0x7F" />
<Parameter Name="TxParamEntry_4A_Tx1" Offset="0x481" Value="0x00" />
<Parameter Name="TxParamEntry_4A_Tx2" Offset="0x482" Value="0x37" />
<Parameter Name="TxParamEntry_4B_ID" Offset="0x483" Value="0x7F" />
<Parameter Name="TxParamEntry_4B_Tx1" Offset="0x484" Value="0x00" />
<Parameter Name="TxParamEntry_4B_Tx2" Offset="0x485" Value="0x37" />
<Parameter Name="TxParamEntry_4C_ID" Offset="0x486" Value="0x7F" />
<Parameter Name="TxParamEntry_4C_Tx1" Offset="0x487" Value="0x00" />
<Parameter Name="TxParamEntry_4C_Tx2" Offset="0x488" Value="0x37" />
<Parameter Name="TxParamEntry_4D_ID" Offset="0x489" Value="0x7F" />
<Parameter Name="TxParamEntry_4D_Tx1" Offset="0x48A" Value="0x00" />
<Parameter Name="TxParamEntry_4D_Tx2" Offset="0x48B" Value="0x37" />
<Parameter Name="TxParamEntry_4E_ID" Offset="0x48C" Value="0x7F" />
<Parameter Name="TxParamEntry_4E_Tx1" Offset="0x48D" Value="0x00" />
<Parameter Name="TxParamEntry_4E_Tx2" Offset="0x48E" Value="0x37" />
<Parameter Name="dummy" Offset="0x48F" Value="0x000000" />
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<Region RegionName="LPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="avg_samples" Offset="0x492" Value="0x06" />
<Parameter Name="lpcd_rssi_target" Offset="0x494" Value="0x02A3" />
<Parameter Name="lpcd_rssi_hyst" Offset="0x496" Value="0x1F" />
<Parameter Name="Config" Offset="0x497" Value="0x003B" />
<Parameter Name="lpcd_threshold_coarse" Offset="0x49A" Value="0x00500050" />
<Parameter Name="lpcd_threshold_fine" Offset="0x49E" Value="0x7FFF7FFF" />
</Region>

<Region RegionName="ULPCD_CONFIG" RegionAccess="RW" RegionType="DATA">
<Parameter Name="Vddpa_Ctrl" Offset="0x4BF" Value="0x0206" />
<Parameter Name="Timing_Ctrl" Offset="0x4C2" Value="0x3D" />
<Parameter Name="Voltage_Ctrl" Offset="0x4C6" Value="0x6A" />
</Region>

<Region RegionName="ULPCD_SETTINGS" RegionAccess="RW" RegionType="DATA">
<Parameter Name="rssi_nsp" Offset="0x4C9" Value="0x10" />
<Parameter Name="rssi_no_samples" Offset="0x4CA" Value="0x00" />
<Parameter Name="thresh_lvl" Offset="0x4CB" Value="0x0C" />
<Parameter Name="polarity" Offset="0x4CC" Value="0x01" />
</Region>

<Region RegionName="TXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
<Parameter Name="TXIRQ_GuardTime" Offset="0x559" Value="0x0000FFFF" />
</Region>

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<Region RegionName="FDT_DEFAULT" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="FDT_DefaultVal" Offset="0x55D" Value="0x000472AC" />
</Region>

<Region RegionName="RXIRQ_GUARD" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RXIRQ_GuardTime" Offset="0x561" Value="0x000F4240" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY CORR" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="Correction_Entry0" Offset="0xBAD" Value="0x0000" />
  <Parameter Name="Correction_Entry1" Offset="0xBAF" Value="0x0000" />
  <Parameter Name="Correction_Entry2" Offset="0xBB1" Value="0x0000" />
  <Parameter Name="Correction_Entry3" Offset="0xBB3" Value="0x0000" />
  <Parameter Name="Correction_Entry4" Offset="0xBB5" Value="0x0000" />
  <Parameter Name="Correction_Entry5" Offset="0xBB7" Value="0x0000" />
  <Parameter Name="Correction_Entry6" Offset="0xBB9" Value="0x0000" />
  <Parameter Name="Correction_Entry7" Offset="0xBBB" Value="0x0000" />
  <Parameter Name="Correction_Entry8" Offset="0xBBD" Value="0x0000" />
  <Parameter Name="Correction_Entry9" Offset="0xBBF" Value="0x0000" />
  <Parameter Name="Correction_Entry10" Offset="0xBC1" Value="0x0000" />
  <Parameter Name="Correction_Entry11" Offset="0xBC3" Value="0x0000" />
  <Parameter Name="Correction_Entry12" Offset="0xBC5" Value="0x0000" />
  <Parameter Name="Correction_Entry13" Offset="0xBC7" Value="0x0000" />
  <Parameter Name="Correction_Entry14" Offset="0xBC9" Value="0x0000" />
  <Parameter Name="Correction_Entry15" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry16" Offset="0xBCD" Value="0x0000" />
  <Parameter Name="Correction_Entry17" Offset="0xBCE" Value="0x0000" />
  <Parameter Name="Correction_Entry18" Offset="0xBD1" Value="0x0000" />
  <Parameter Name="Correction_Entry19" Offset="0xBD3" Value="0x0000" />
  <Parameter Name="Correction_Entry20" Offset="0xBD5" Value="0x0000" />
  <Parameter Name="Correction_Entry21" Offset="0xBD7" Value="0x0000" />
  <Parameter Name="Correction_Entry22" Offset="0xBD9" Value="0x0000" />
  <Parameter Name="Correction_Entry23" Offset="0xBDB" Value="0x0000" />
  <Parameter Name="Correction_Entry24" Offset="0xBDD" Value="0x0000" />
  <Parameter Name="Correction_Entry25" Offset="0xBDF" Value="0x0000" />
  <Parameter Name="Correction_Entry26" Offset="0xBE1" Value="0x0000" />
  <Parameter Name="Correction_Entry27" Offset="0xBE3" Value="0x0000" />
  <Parameter Name="Correction_Entry28" Offset="0xBE5" Value="0x0000" />
  <Parameter Name="Correction_Entry29" Offset="0xBE7" Value="0x0000" />
  <Parameter Name="Correction_Entry30" Offset="0xBE9" Value="0x0000" />
  <Parameter Name="Correction_Entry31" Offset="0xBEB" Value="0x0000" />
  <Parameter Name="Correction_Entry32" Offset="0xBED" Value="0x0000" />
  <Parameter Name="Correction_Entry33" Offset="0xBEF" Value="0x0000" />
  <Parameter Name="Correction_Entry34" Offset="0xBF1" Value="0x0000" />
  <Parameter Name="Correction_Entry35" Offset="0xBF3" Value="0x0000" />
  <Parameter Name="Correction_Entry36" Offset="0xBF5" Value="0x0000" />
  <Parameter Name="Correction_Entry37" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry38" Offset="0xBF9" Value="0x0000" />
  <Parameter Name="Correction_Entry39" Offset="0xBFB" Value="0x0000" />
  <Parameter Name="Correction_Entry40" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry41" Offset="0xBF7" Value="0x0000" />
  <Parameter Name="Correction_Entry42" Offset="0xC01" Value="0x0000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY 1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC03" Value="0xD9D9D3CD" />
  <Parameter Name="RTRANS1" Offset="0xC07" Value="0xF1EEEBE5" />
  <Parameter Name="RTRANS2" Offset="0xC0B" Value="0xFDFAF7F4" />
  <Parameter Name="RTRANS3" Offset="0xC0F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC13" Value="0xE7EDF3F9" />
  <Parameter Name="FTRANS1" Offset="0xC17" Value="0xD4D8DBE1" />
  <Parameter Name="FTRANS2" Offset="0xC1B" Value="0xC8CACDD1" />
  <Parameter Name="FTRANS3" Offset="0xC1F" Value="0xC7C7C7C7" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY 2" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC23" Value="0xF0EAE3DA" />
  <Parameter Name="RTRANS1" Offset="0xC27" Value="0xFAF9F6F4" />
  <Parameter Name="RTRANS2" Offset="0xC2B" Value="0xFEFFDFDF" />
  <Parameter Name="RTRANS3" Offset="0xC2F" Value="0xFFFFFFFF" />
  <Parameter Name="FTRANS0" Offset="0xC33" Value="0xFEFFDFDF" />
  <Parameter Name="FTRANS1" Offset="0xC37" Value="0xFCFDFDFE" />
  <Parameter Name="FTRANS2" Offset="0xC3B" Value="0xF4F6F9FA" />
  <Parameter Name="FTRANS3" Offset="0xC3F" Value="0xDAE3EAF0" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY 3" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC43" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC47" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC4B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC4F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC53" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC57" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC5B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC5F" Value="0x00000000" />
</Region>

<Region RegionName="TX_SHAPING_PROPRIETARY 4" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RTRANS0" Offset="0xC63" Value="0x00000000" />
  <Parameter Name="RTRANS1" Offset="0xC67" Value="0x00000000" />
  <Parameter Name="RTRANS2" Offset="0xC6B" Value="0x00000000" />
  <Parameter Name="RTRANS3" Offset="0xC6F" Value="0x00000000" />
  <Parameter Name="FTRANS0" Offset="0xC73" Value="0x00000000" />
  <Parameter Name="FTRANS1" Offset="0xC77" Value="0x00000000" />
  <Parameter Name="FTRANS2" Offset="0xC7B" Value="0x00000000" />
  <Parameter Name="FTRANS3" Offset="0xC7F" Value="0x00000000" />
</Region>

<Region RegionName="RF_CLOCK_ACTIVE_DPLL_COM" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="DPLL_INIT_ActiveInitiator" Offset="0xCA8" Value="0x20050530" />
  <Parameter Name="DPLL_GEAR_ActiveInitiator" Offset="0xCAC" Value="0x0FFDFEFF" />

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</Region>

<Region RegionName="TX_DRIVER_NOV" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="CfignovCal" Offset="0xC83" Value="0x42" />
  <Parameter Name="VddpaCalVal1" Offset="0xC84" Value="0x03" />
  <Parameter Name="VddpaCalVal2" Offset="0xC85" Value="0x15" />
  <Parameter Name="CfignThreshold" Offset="0xC86" Value="0x08" />
  <Parameter Name="UserOffsets1" Offset="0xC87" Value="0x8A0A0C00" />
  <Parameter Name="UserOffsets2" Offset="0xC8B" Value="0x09080D03" />
</Region>

<Region RegionName="USER_PMU_INT_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="EnableFastVDDPDischarge" Offset="0xC8F" Value="0x00" />
</Region>

<Region RegionName="ARC_SETTINGS_1" RegionAccess="RW" RegionType="DATA">
  <Parameter Name="RmArcA_106_FDT" Offset="0xC9D" Value="0x8040804080608060C060" />
</Region>

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  <Parameter Name="Tx_Data_Mod_Reg_BR_53" Offset="0xCC9" Value="0x00000044" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_106" Offset="0xCCD" Value="0x00000006" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_106" Offset="0xCD1" Value="0x00000045" />
  <Parameter Name="Tx_Symbol23_Mod_Reg_BR_212" Offset="0xCD5" Value="0x000080047" />
  <Parameter Name="Tx_Data_Mod_Reg_BR_212" Offset="0xCD9" Value="0x01080006" />
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  <Parameter Name="RxGuardTO_Multiple" Offset="0xCE8" Value="0x01" />
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<Region RegionName="COMBINED_TB_SETTINGS" RegionAccess="RW" RegionType="DATA">
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  <Parameter Name="DigitalTBSignalBit" Offset="0xCEA" Value="0x04" />
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    <Register RegisterName="CLIF_TRANSCEIVE_CONTROL" RegisterLogicalAddress="0x08" RegisterValue="0x00003D41"></Register>
    <Register RegisterName="CLIF_SS_TX_CFG" RegisterLogicalAddress="0x15" RegisterValue="0x00002289"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_MOD" RegisterLogicalAddress="0x0C" RegisterValue="0x00220104"></Register>
    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
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    <Register RegisterName="CLIF_TX_SYMBOL23_DEF" RegisterLogicalAddress="0x0D" RegisterValue="0x00000000"></Register>
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</Protocol>
</Region>
</EEPROM>
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## 26 Abbreviations

Table 330. Abbreviations

| Acronym  | Description  |
|----------|--|
| AA       | audio accelerator  |
| ADC      | analog-to-digital converter  |
| AGC      | automatic gain control   |
| AHB      | advanced high-performance bus  |
| AHB-Lite | advanced high-performance bus (single-controller implementation)   |
| AHB bus  | advanced high-performance bus  |
| APB      | advanced peripheral bus  |
| API      | application programming interface  |
| ARC      | adaptive receiver control  |
| Arm      | Advanced RISC Machine  |
| AWC      | adaptive waveshape control   |
| BBA      | baseband amplifier   |
| BOD      | brownout detection   |
| CITO     | controller input target output (previously master input slave output)  |
| CLIF     | contactless interface  |
| COTI     | controller output target input (previously master output slave input)  |
| CPU      | central processing unit  |
| CRC      | cyclic redundancy check  |
| CTR      | current transfer ratio   |
| CTS      | clear to send  |
| DAC      | digital-to-analog converter  |
| DC-DC    | switch-mode voltage regulator which uses an inductor to store and transfer energy to the output, used for a power supply voltage conversion. PN5190B1 integrates a step-up/boost converter |
| DDR      | double data rate   |
| DMA      | direct memory access   |
| DPC      | dynamic power control  |
| ECC      | elliptic curve cryptography  |
| EEPROM   | electrically erasable programmable read-only memory  |
| EMC      | electromagnetic compatibility  |
| EMD      | electromagnetic disturbance  |
| ETB      | Embedded Trace Buffer  |
| ETM      | Embedded Trace Macro   |
| EOF      | end-of-frame   |
| Fm+      | Fast-mode Plus   |
| FSM      | finite state machine   |



Table 330. Abbreviations...continued

| Acronym | Description   |
|---------|---|
| GND     | Ground  |
| GPIO    | general-purpose input output                            |
| HID     | human interface device                                  |
| HPD     | hard power down   |
| HW      | hardware  |
| IC      | Integrated Circuit                                      |
| IIR     | infinite impulse response                               |
| IrDA    | Infrared Data Association                               |
| IAP     | In-Application Programming                              |
| ISP     | In-System Programming                                   |
| I/O     | input/output  |
| I/Q     | in-phase/quadrature-phase                               |
| JEDEC   | Joint Electron Device Engineering Council               |
| LDO     | low dropout regulator                                   |
| LPCD    | low-power card detection                                |
| LPUART  | Low-Power Universal Asynchronous Receiver / Transmitter |
| LSB     | least significant bit                                   |
| LSByte  | least significant byte                                  |
| MISO    | SPI interface controller in target out                  |
| MSL     | moisture sensitivity level                              |
| MOSI    | SPI interface controller out target In                  |
| NFC     | near-field communication                                |
| NRZ     | non-return-to-zero                                      |
| NSS     | SPI interface active-low target-select signal           |
| NTS     | not target select (previously not slave select)         |
| NVIC    | nested vectored interrupt controller                    |
| OS      | operating system  |
| OTP     | one time programmable                                   |
| PCB     | printed-circuit board                                   |
| PC      | personal computer                                       |
| PCD     | power card detection                                    |
| PICC    | proximity inductive coupling card                       |
| PLL     | phase-locked loop                                       |
| PMU     | power management unit                                   |
| PWM     | pulse width modulation                                  |
| RAM     | random-access memory                                    |

Table 330. Abbreviations...continued

| Acronym | Description   |
|---------|---|
| RF      | radio frequency   |
| RNG     | random number generator   |
| ROM     | read-only memory  |
| RSA     | Rivest, Shamir, and Adleman public key cryptosystem   |
| RSSI    | receiver signal strength indicator  |
| RTOS    | real-time operating system  |
| RTS     | request to send   |
| SCK     | SPI interface serial clock  |
| SCL     | I <sup>2</sup> C interface serial clock   |
| SDA     | serial data   |
| SMPS    | switch mode power supply  |
| SPI     | serial peripheral interface   |
| SRAM    | static random-access memory   |
| SWD     | serial wire debug   |
| TFT     | display technology: thin-film transistor-display  |
| TX      | transmit  |
| UART    | universal asynchronous receiver transmitter   |
| UID     | Unique identifier of a card, used during anti-collision sequence to select one out of multiple cards. |
| ULPCD   | ultra low-power card detection  |
| USB     | universal serial bus  |
| VREF    | voltage reference   |

## 27 References

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- [1] Application note - AN12551 PN5190 design-in recommendations, <https://www.nxp.com/doc/AN12551>
- [2] Application note - AN12549 PN5190 Antenna design guide, <https://www.nxp.com/doc/AN12549>
- [3] User manual - UM11942 PN5190 instruction layer, <https://www.nxp.com/doc/UM11942>

## 28 Note about the source code in the document

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## 29 Revision history

Table 331. Revision history

| Document ID     | Release date   | Data sheet status  | Supersedes      |
|-----------------|--|--------------------|-----------------|
| PN5190B1 v. 3.8 | 20231120   | Product data sheet | PN5190B1 v. 3.7 |
| Modifications:  | <ul style="list-style-type: none"> <li>Register description for PMU_ANA_SMPS_CTRL_REG (00058h) removed</li> <li><a href="#">Section 9.25.3</a>, <a href="#">Section 9.25.59</a> and <a href="#">Section 9.25.61</a>: some bit fields updated</li> </ul>  |                    |                 |
| PN5190B1 v. 3.7 | 20231106   | Product data sheet | PN5190B1 v. 3.6 |
| Modifications:  | <ul style="list-style-type: none"> <li><a href="#">Section 27 "References"</a>: PN5190 instruction layer [3]: Document type changed from product data sheet addendum to user manual</li> <li>New register added: <a href="#">Section 9.26.195 "ENABLE_ULFO_TRIM_CALIBRATION (0CECh)"</a></li> <li><a href="#">Section 6 "Ordering information"</a>: updated</li> <li><a href="#">Section 4 "Firmware versions"</a> updated</li> <li>New appendixes added</li> <li><a href="#">Section 28</a>: added</li> </ul>   |                    |                 |
| PN5190B1 v. 3.6 | 20230515   | Product data sheet | PN5190B1 v. 3.5 |
| Modifications:  | <ul style="list-style-type: none"> <li>New firmware versions 2.6 added, new registers and description added</li> <li>Register description for SIGPRO_CONFIG (001Dh) added</li> <li>Host interface command list updated with command 0x29</li> <li>CLK_INPUT_FREQ (0012h): Table for frequencies updated</li> <li>V<sub>DD(VUP_TX)</sub> Absolute Limiting Value increased to 6.3 V</li> <li>Package marking drawing VFBGA64 updated with new FW version information</li> <li>Package marking drawing VFLGA40 updated with new FW version information</li> <li>Initial calibration: Value to write for calibration updated</li> <li>Supply voltage range for transmitter supply configuration examples: updated</li> <li>DWL_REQ pin description: Recommendation added</li> <li><a href="#">Table 318 "AUX1, AUX2, AUX3 pins (Debug output)"</a>: V<sub>AUX_OL</sub> mV corrected to V</li> <li>Various typos corrected and descriptions improved</li> </ul>  |                    |                 |
| PN5190B1 v. 3.5 | 20221019   | Product data sheet | PN5190B1 v. 3.4 |
| Modifications:  | <ul style="list-style-type: none"> <li>Package type HVQFN40 updated to official naming VFLGA40</li> <li><a href="#">Section 6 "Ordering information"</a>: updated</li> <li>The replacement of "master/slave" by "controller/target" in this document follows the recommendation of the NXP - I<sup>2</sup>C and JEDEC SPI standards organizations.</li> <li>Pin description in static characteristics corrected. CLK → XTAL <a href="#">Table 312</a></li> <li>Pin name in <a href="#">Table 3</a> and <a href="#">Table 4</a> corrected. VBATPWR → VBAT_PWR</li> <li>Pin name in <a href="#">Table 319</a> corrected. DAC → VTUNE</li> <li>Register RX_STATUS_ERROR: Bit description corrected</li> <li>RX_ERROR_CONFIG register (address 0027h) description updated</li> <li>Pin description VFLGA40: ATX Input / output corrected.</li> <li>Chapter antenna connection: added remark: Stored as part of the RF protocol configuration, added RM_GLOBAL_TX_SHAPING. bTX_INV_RM (0x18)</li> <li>Register description for RX_ERROR_CONFIG removed, there is nothing to be configured/modified - default values work under all conditions.</li> <li>EEPROM description DPC_TXLDO_MAX_DROP (0081h) added</li> <li>TXLDO_CONFIG (0002h) description updated</li> <li>TXLDO_VDDPA_HIGH (0006h) description updated</li> <li>TxLdoVddpaLow (adr 0x07) description removed and changed to RFU- no useful function linked to this address.</li> <li>TX_SHAPING_CONFIG (address 0017h): description updated</li> </ul> |                    |                 |

Table 331. Revision history...continued

| Document ID     | Release date | Data sheet status   | Supersedes      |
|-----------------|--------------|---|-----------------|
|                 |              | <ul style="list-style-type: none"> <li>Small editorial changes</li> </ul>   |                 |
| PN5190B1 v. 3.4 | 20220701     | Product data sheet  | PN5190B1 v. 3.3 |
| Modifications:  |              | <ul style="list-style-type: none"> <li><a href="#">Figure 31 "Two antennas connected to TX1, TX2 each"</a>: corrected</li> <li>EEPROM 0C55h: DWORD for USER_DATA storage had been added</li> <li>EEPROM TEMP_WARNING (address 0014h): description updated in <a href="#">Table 80</a></li> <li>Updated Antenna register configuration <a href="#">Table 13</a> (added "do not care" for TX2_CLK_MODE_TRANS_RM, TX2_CLK_MODE_MOD_RM, TX2_CLK_MODE_CW_RM; TX2_USE_TX1_CONF for single ended TX2 is "0b")</li> <li>Updated Antenna EEPROM configuration in <a href="#">Table 14</a> (removed the EEPROM modification of 0x19 and 0x1A, since that must done via register update after Load Protocol)</li> <li>GPIO0: Pin function description changed from I/O to Input only in <a href="#">Section 8.2</a>.</li> <li>SPI interface timing updated for 15 MHz SPI clock frequency</li> <li>Vtune1 comment removed in description for VFBGA description</li> <li>Description of FW2.05</li> <li>Description EXT_RFOFF_DETECTED corrected</li> <li>Description RX_FRAME_MAXLEN_VIOL corrected</li> <li>Description RX_COLLISION_STOPBIT_DETECTED corrected</li> <li>Description RFOFF_DET_EVENT corrected</li> <li>EEPROM configuration TX_SHAPING_CONFIG description updated</li> <li>EEPROM configuration VDDPA_DISCHARGE description updated</li> <li>System power supply clarification: The Voltage on pin VDDIO must always be smaller or equal to the Voltage on pin VBAT. This limitation is not applicable in power off mode.</li> <li>RX_PROTOCOL_CONFIG (0025h) bit description updated, bist which should not be used set to RFU</li> </ul> |                 |
| PN5190B1 v. 3.3 | 20220419     | Product data sheet  | PN5190B1 v. 3.2 |
| Modifications:  |              | <p><a href="#">Section 9.25.62 "DPC_CONFIG (005Eh)"</a>: Description improved.</p> <p><a href="#">Table 319 "VTUNE0 and VTUNE1 output pins (Tuning DAC)"</a>: Condition for max output voltage updated: VDDIO = 3.3 V</p> <p><a href="#">Table 77 "DAC register (address 0057h) bit description"</a>: TUNING_DAC_2_RANGE description improved</p> <p><a href="#">Table 54 "RX_CRC_CONFIG register (address 0031h) bit description"</a>: Register description added</p> <p><a href="#">Table 3 "Pin description VFBGA64"</a> and <a href="#">Table 4 "Pin description VFLGA40"</a>: Pin VEN - remark added: "Avoid a floating or unexpected toggling of the pin."</p> <p><a href="#">Section 9.26.157 "LPCD_THRESHOLD_COARSE (049Ah)"</a>: Address corrected to 49Ah</p> <p><a href="#">Table 256 "LPCD_AVG_SAMPLES (address 0492h) EEPROM configuration bit description"</a>: Updated description <b>0 to 6</b></p>   |                 |
| PN5190B1 v. 3.2 | 20211117     | Product data sheet  | PN5190B1 v. 3.1 |
| Modifications:  |              | <ul style="list-style-type: none"> <li><a href="#">Section 9.8</a>: TEMP_WARNING address corrected to 14h</li> <li><a href="#">Section 9.26.4</a>: TXLDO_CONFIG description updated with Overcurrent enable and TxLdo current limiter</li> <li><a href="#">Section 9.25.4</a>: EVENT_STATUS and <a href="#">Section 9.25.3</a> EVENT_ENABLE register: TEMP_ERROR_EVENT corrected to / replaced by TX_OVERCURRENT_ERROR_EVENT (bit 5)</li> <li><a href="#">Section 9.5.3.9</a>: Power configuration corrected</li> </ul>   |                 |
| PN5190B1 v. 3.1 | 20210907     | Product data sheet  | PN5190B1 v. 3.0 |
| Modifications:  |              | <ul style="list-style-type: none"> <li>Description for FW2.3 added</li> <li>General update and clarifications added</li> <li>Description for SE antenna configurations added</li> </ul>   |                 |
| PN5190B1 v. 3.0 | 20210421     | Product data sheet  | PN5190B1 v. 1.0 |

Table 331. Revision history...continued

| Document ID     | Release date   | Data sheet status    | Supersedes |
|-----------------|--|----------------------|------------|
| Modifications:  | <ul style="list-style-type: none"><li>• General update</li><li>• Data sheet status changed to "Product data sheet"</li></ul> |                      |            |
| PN5190B1 v. 1.0 | 20210322   | Objective data sheet | -          |
| Modifications:  | <ul style="list-style-type: none"><li>• First official released version</li></ul>  |                      |            |

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### Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

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