AN5299

MM9Z1_638 diagnostic features

Rev. 1.0 — 14 July 2016 Application note

1 Introduction

The MM9Z1_638 Intelligent Battery Sensors contain extensive features for self-diagnostics. This application note lists the features available and explains in detail how to use the acquisition channel diagnostic features.

1.1 Purpose

The purpose of this application note is to show what diagnostic features are available on the MM9Z1_638 device in general and in detail the features related to the acquisition channel.

The acquisition channel diagnostic is available for all three channels the ISENSE (current measurement channel), VSENSE (voltage measurement channel) and the TSENSE (temperature measurement channel).

1.2 Glossary, terms and abbreviation

Acquisition	Acquisition of analog data using a Sigma-Delta Analog-to-Digital Converter
Big Endian	The most significant byte is stored first, at a memory address, the following less significant bytes are stored at incrementing memory addresses
ECC	Error Correction Code
EEPROM	Read only memory for data
FLASH	Read only memory for program and data
LIN	Local interconnect network – 12 V single wire automotive communication interface and standard
IBS	Intelligent Battery Sensor
IFR	Information Row – special read-only area in the Flash memory, used to store compensation values
ISENSE	Current measurement acquisition channel
NVM	None volatile memory (FLASH and EEPROM)
TSENSE	Temperature measurement acquisition channel
VSENSE	Voltage measurement acquisition channel
μC	Microcontroller

2 Overview

The MM9Z1_638 intelligent battery sensor can measure voltage, current, and temperature of a battery system. The chip is optimized to monitor automotive 12 V starter batteries, but can also be used in other battery monitoring applications, like UPS (uninterruptible power supplies), emergency/backup supplies (as are used in elevators, and so on).

Figure 1 shows an application block diagram of a 12 V monitoring system.

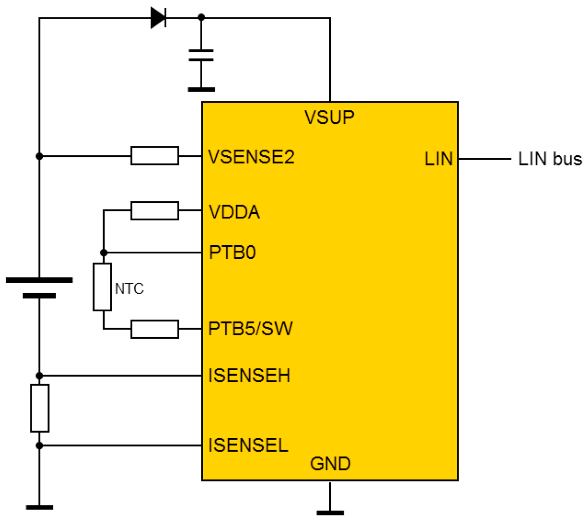


Figure 1. Application diagram (12 V lead acid battery)

The key measurement parameters are battery voltage, current, and temperature, therefore this application note focuses on the diagnostics of those acquisition channels.

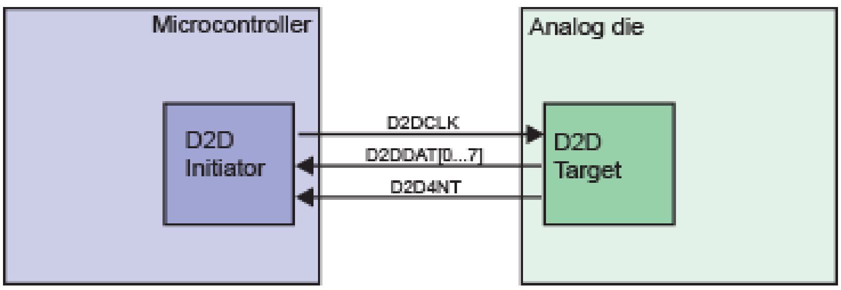
2.1 Diagnostic features

The following lists all diagnostic features available for the MM9Z1_638 product. The MM9Z1_638 is a two chip solution incorporating two die in one QFN-48 package.

2.2 Diagnostics features of the microcontroller

- FLASH and EEPROM memory
  - ECC, single bit correction, double bit detection
  - Optional ECC error interrupt for single bit error
  - ECC machine exception for double bit errors (see S12ZMMCV1)
  - Protection against accidental program and erase
  - Margin read feature for in-system flash verification and production line programming to detect marginal programming of data in the production flow and to monitor the programming level during life time.
- SRAM memory
  - ECC, single bit correction, double bit detection
  - Optional ECC error interrupt for single bit error
  - ECC machine exception for double bit errors (see S12ZMMCV1)
- Clock monitor

  - Detects PLL-out-of-lock condition
  - Detects IRC-loss-of-oscillation
  - Interrupt
  - Reset
  - Register flag for source indication after reset
  - Crystal clock detector and monitor
- Clock settings protectable against unintended overwrite by SW
- Illegal memory address access
  - Machine exception with error code information (S12ZMMCV1)
- Illegal access protection
  - Opcode fetches from register space
  - Opcode fetches from unmapped address ranges
  - Opcode fetches from reserved address ranges
  - Opcode fetches from NVM IFR
  - Load or store accesses to unmapped address ranges
  - Store accesses to EEPROM
  - Store accesses to the NVM IFR
  - Store accesses to the reserved address ranges in normal single-chip mode
  - Store accesses to the reserved read-only address ranges
  - Store accesses to flash
- Unimplemented instruction interrupts
- Watchdog based on independent RC oscillator
  - Conventional
  - Windowed
  - Disabled at power-up (watchdog in analog die is enabled)
  - Can be enabled during stop mode
- Low-voltage detect
  - Interrupt
  - Reset
  - Register flag for source indication after reset
- Diagnostic features of the Die-to-Die Interface. The microcontroller and analog chip communicate using a dedicated interface.



  - Parity bits
    - 1 bit parity per 4 data bits -> 2 bits per 8 data bits
  - Timeout
  - Acknowledge error (during high phase, a bit was sampled low -> possible stuck-at-0)
  - Common error interrupt for all three sources

2.3 Diagnostic features of the analog die

- Measurement channels
  - PTB[0-4] inputs can be routed to both VSENSE and TSENSE ADC (independent measurement with two separate channels)
  - NVM stored reference values for diagnosis measurements (for current, voltage and temperature channels) using independent reference (see Section 3 "Diagnosis of acquisition channels")
  - Current channel: PGA diagnosis by shorting the inputs
  - Voltage/current/temperature measurement result overwritten
  - Band gap reference status (applied or not)
- High temperature
  - Interrupt
  - Shutdown
  - Register flag for source indication after reset
- Low-voltage
  - Interrupt
  - Reset
  - Register flag for source indication after reset
- Watchdog
  - Conventional
  - Window watchdog
  - Enabled at system power-up
- LIN physical layer
  - Overtemperature interrupt & transmitter shutdown
  - Register flag indication of HF disturbance
- SCI (digital part of LIN communication)
  - Parity check (+ error interrupt)
  - Noise detection (+ interrupt)
  - Framing error (+ interrupt)
  - Overrun (+ interrupt)

2.4 Application specific diagnostic features

- Open shunt detection
- High-voltage threshold flag for VSENSE0..3 (ACQ_SR.VTH)
- Calibration request interrupt (on temperature change, to change gain compensation values and detect unexpected or dangerous temperatures if necessary).

3 Diagnosis of acquisition channels

Diagnostics during runtime can achieved by connecting a known signal to the input of the acquisition channel, performing an acquisition and comparing the result against the expected value. This has to be performed for each of the three acquisition channels, individually.

Table 1. Diagnostics reference "known signal" values

Channel to diagnose	Known signal	Expected value (Diagnostics reference value)
ISENSE	V_{REF}T (V_{REF} of TSENSE channel)	IFR_DIAG_ISENSE_ROOM
VSENSE	V_{REF}T (V_{REF} of TSENSE channel)	IFR_DIAG_VSENSE_ROOM
TSENSE	V_{REF}V/I (V_{REF} of VSENSE/ISENSE)	IFR_DIAG_TSENSE_ROOM

The following figure depicts the acquisition channel diagnostics.

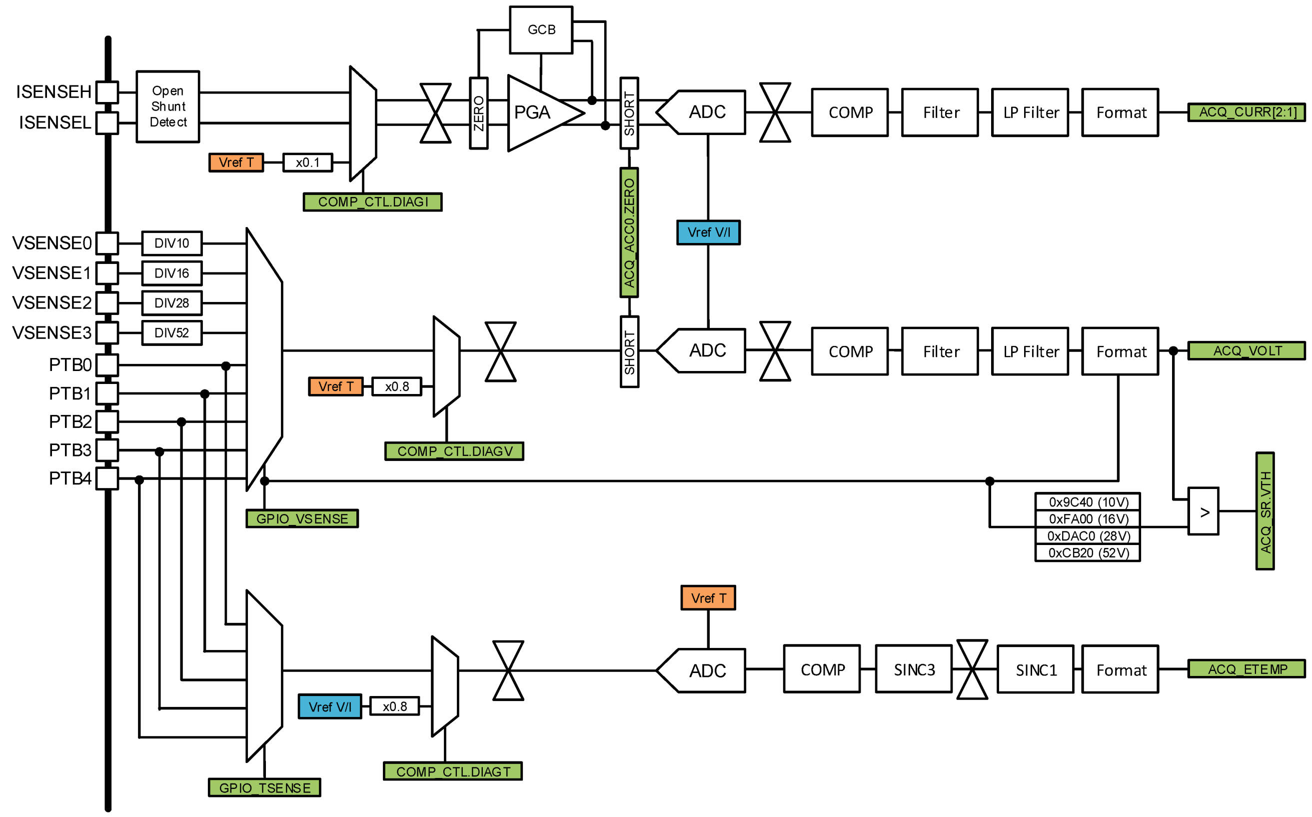


Figure 2. Acquisition channel diagnostics

The expected value varies from devices to device, therefore a device specific diagnostic value is measured during final test of the device, and is stored in none volatile IFR Flash memory of each device.

Respective diagnostic measurements can be obtained by selecting the DIAGI(M), DIAGV(M) or DIAGT(M) bit in the COMP_CTL register.

Offset (165)(166)	0xA0 / 0xA1				Access: User read/write			
	15	14	13	12	11	10	9	8
R	0	0	0	0	0	0	0	0
W	OPENEM		PGAZM	PGAOM	DIAGVM	DIAGIM	DIAGTM	CALIEM
Reset	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
R / W	OPENE		PGAZ	PGAO	DIAGV	DIAGI	DIAGT	CALIE
Reset	0	0	0	0	0	0	0	0

Notes:
165.Offset related to 0x0E00 for blocking access and 0x0F00 for non blocking access within the global address space.
166.This Register is 16-Bit access only.

Figure 3. Compensation Control Register (COMP_CTL)

Finally the diagnostic measurement result is compared against the expected value (see Table 2). The byte order is Big Endian (see http://en.wikipedia.org/wiki/Endianness).

Table 2. Diagnostic value flash (IFR) location

Global address	Type	Description
0x1F_C0F4 (hi) 0x1F_C0F5 (mid) 0x1F_C0F6 (lo)	SINT24	IFR_DIAG_IG4_ROOM Diagnostics reference value for the ISENSE channel (gain 4) at room temperature
0x1F_C0F7 (hi) 0x1F_C0F8 (lo)	UINT16	IFR_DIAG_VSENSE_ROOM Diagnostics reference value for the VSENSE channel at room temperature
0x1F_C0F9 (hi) 0x1F_C0FA (lo)	UINT16	IFR_DIAG_TSENSE_ROOM Diagnostics reference value for the TSENSE channel at room temperature

For comparison additional effects caused by temperature and drifts have to be considered. Those effects are considered to be less than +/−1.5 % of the diagnostic reference value.

Equation 1

$$ref.value * (100\,\% - 1.5\,\%) \le measurement \le ref.value * (100\,\% + 1.5\,\%)$$

All hardware blocks of the acquisition channels are included in this diagnosis method. By cross-checking the ADC references, on top of checking acquisition channels also the references themselves are checked.

Additionally, it is possible to short the inputs of the ISENSE and VSENSE acquisition channel inputs (see Figure 2). The acquisition reflects a result close to zero.

3.1 ISENSE channel diagnostics

This chapter gives practical tips and recommended settings for implementing an ISENSE ACQ channel diagnostics.

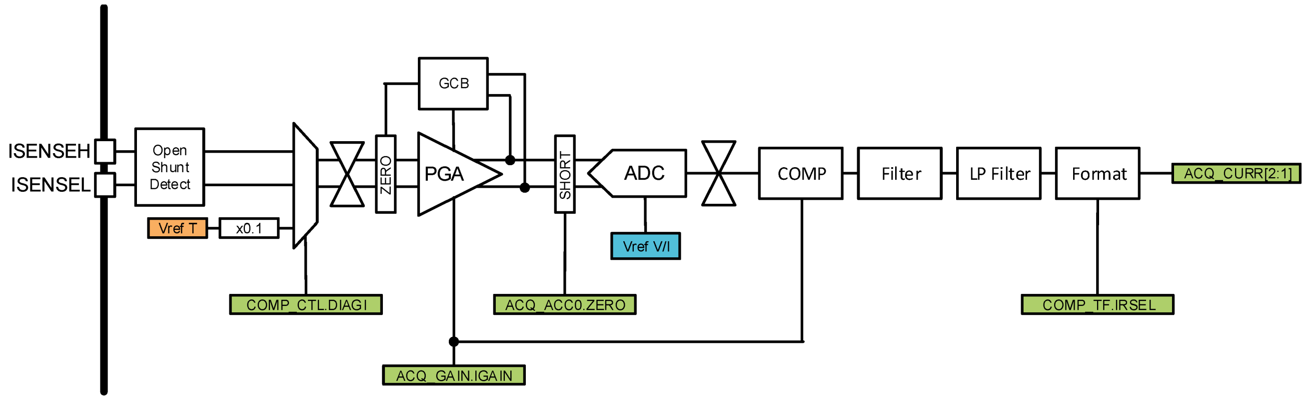


Figure 4. ISENSE diagnostics

In order to run the ISENSE channel diagnostics, the reference V_{REF} T, of the TSENSE channel, has to be connected to the ISENSE ADC by setting the COMP_CTL.DIAGI(M) bit. The TSENSE acquisition channel must be disabled to not to load the V_{REF}T, while performing the diagnostics measurement.

Table 3 shows the recommended settings to run the ISENSE channel diagnostics:

Table 3. ISENSE diagnostic recommended settings

Parameter	Setting	Pseudo code	Comment
Pre-requisite			
Mode	Normal mode	`PCR_CTL = OPM_SET_NORMAL;`	
D2DFCLK (ACQ Clock)	512 kHz	`PCR_PRESC = BUSCLOCKKHZ;`	Set to achieve D2DFCLK = 512 kHz
Startup Trimming	performed	`SYSStartupTrimming();`	
TSENSE channel	disabled	`ACQ_CTL = ACQ_CTL_ITMENM_MASK| ACQ_CTL_ETMENM_MASK|0;`	Must be disabled to no load the V_{REF} T
TSENSE reference signal	disconnected	`CompCtlDiagTDisable();`	disconnect V_{REF} V/I from TSENSE
VSENSE channel	disabled	`ACQ_CTL = ACQ_CTL_VMENM_MASK| 0;`	Should be off
VSENSE reference signal	disconnected	`CompCtlDiagVDisable();`	disconnect V_{REF}V/I from TSENSE
Shunt selection	100 µOhm	`COMP_TF = SHUNT_100uOhm;`	Influences ACQ result scaling/ formatting
PGA autozero	performed		
Channel settings			
Decimation	512	`ACQ_DEC = DEC512;`	1.0 kHz sample rate
GCB auto gain	disabled	`ACQAGCDisable();`	Disable auto gain control
GAIN	4	`ACQ_GAIN = GAIN4;`	Use fixed gain 4
Chopper mode	ON		Chopper is always on
IIR filter	1/32	`ACQ_CVCR = IIR_1_32;`	
Low Pass Filter	Off (or On)	`ACQLPFDisable();`	Off for faster execution (Latency)

Parameter	Setting	Pseudo code	Comment
ISENSE channel compensation	Off	`ACQCCompDisable();`	Compensation must be off
ISENSE reference signal	V_{REF} T	`CompCtlDiagIEnable();`	Connect V_{REF} T to ISENSE channel
Averaging	16 samples	Result = 1/16 * sum(Vn);	Recommended to average in software

Evaluation of the ISENSE diagnostics of seven different samples over temperature are shown in Figure 5. The error between measured value and reference (IFR) value in % is shown.

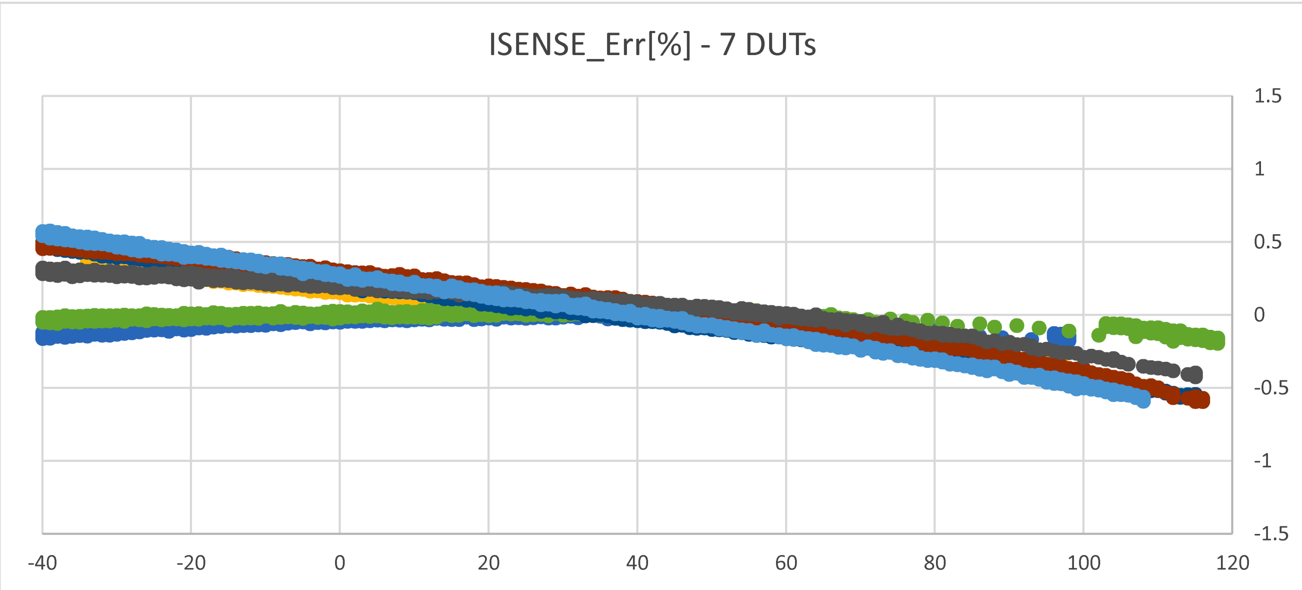


Figure 5. Diagnostic measurement results over temperature

3.2 VSENSE channel diagnostics

This chapter gives practical tips for implementing a VSENSE ACQ diagnostics.

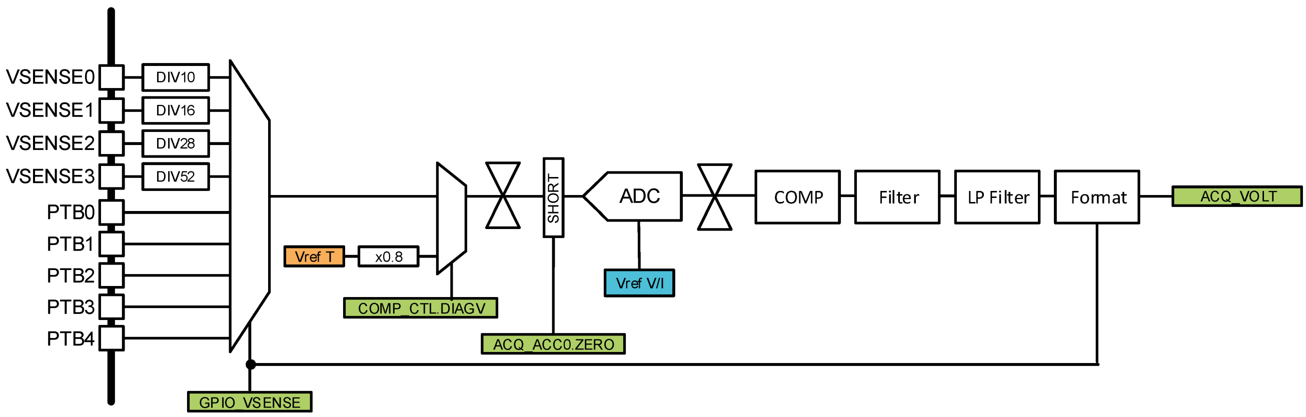


Figure 6. VSENSE diagnostics

In order to run the VSENSE channel diagnostics, the reference V_{REF} T, of the TSENSE channel, has to be connected to the VSENSE ADC by setting the COMP_CTL.DIAGV(M) bit. The TSENSE acquisition channel must be disabled to not load the V_{REF} T.

Table 4 shows the recommended settings to run the VSENSE channel diagnostics:

Table 4. VSENSE diagnostic recommended settings

Parameter	Setting	Pseudo code	Comment
Pre-requisite			
Mode	Normal mode	`PCR_CTL = OPM_SET_NORMAL;`	
D2DFCLK (ACQ Clock)	512 kHz	`PCR_PRESC = BUSCLOCKKHZ;`	Set to achieve D2DFCLK = 512 kHz
Startup Trimming	performed	`SYSStartupTrimming();`	
TSENSE channel	Disabled	`ACQ_CTL = ACQ_CTL_ITMENM_MASK| ACQ_CTL_ETMENM_MASK|0`	Must be disabled to not load the V_{REF} T
TSENSE reference signal	V_{REF} V/I	`CompCtlDiagTDisable();`	disconnect V_{REF} V/I from TSENSE
ISENSE channel	Disabled	`ACQ_CTL = ACQ_CTL_IMENM_MASK| 0;`	Should be off
ISENSE reference signal	V_{REF} T	`CompCtlDiagIDisable();`	disconnect V_{REF}T from ISENSE
Channel settings			
Decimation	512	`ACQ_DEC = DEC512;`	1.0 kHz sample rate
Chopper mode	On	`ACQ_ACC1 = ACQ_ACC1_CVCHOPM_MASK| ACQ_ACC1_CVCHOP_MASK;`	
IIR filter	1/32	`B_ACQ_CVCR = IIR_1_32;`	
Low Pass Filter	Off (or On)	`ACQLPFDisable();`	Off for faster execution (Latency)
Channel compensation	Off	`ACQVCompDisable();`	Compensation must be off
Multiplexer	VSENSE0	`GPIO_VSENSE = VSENSE0;`	Multiplexer setting influences Format/Clamping (and Compensation)
VSENSE reference signal	V_{REF} T	`CompCtlDiagVEnable();`	connect V_{REF}T to VSENSE channel
Averaging	8 samples	Result = 1/8 * sum(Vn)	Recommended to average in software

Evaluation of the VSENSE diagnostics of seven different samples over temperature are shown in Figure 7. The error between measured value and reference (IFR) value in % is shown.

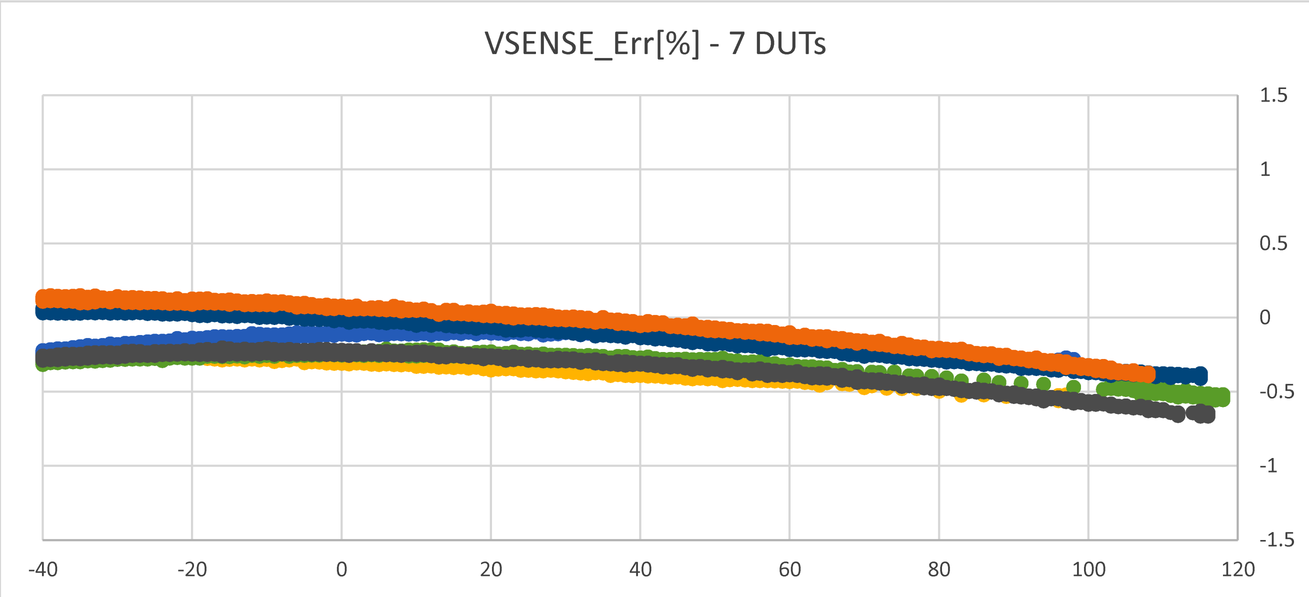


Figure 7. VSENSE diagnostic measurement results over temperature

3.3 TSENSE channel diagnostics

This chapter gives practical tips for implementing a TSENSE ACQ diagnostics.

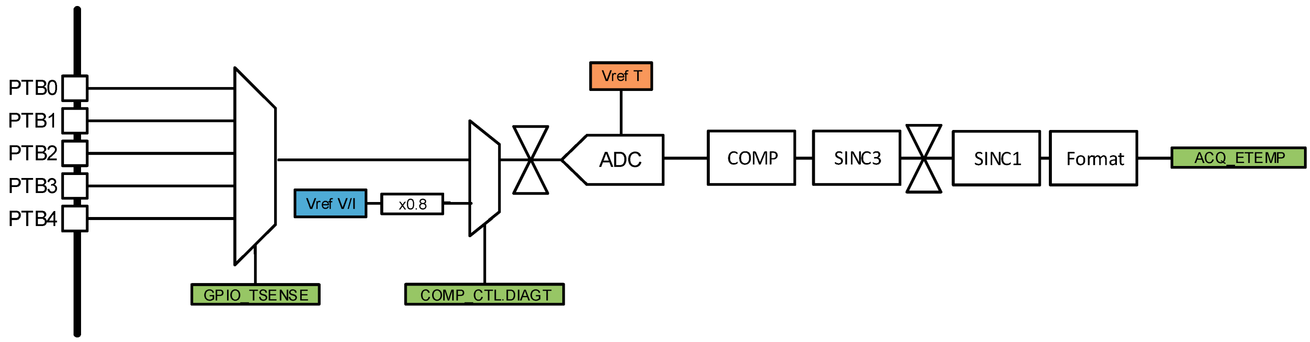


Figure 8. TSENSE diagnostics

To run the TSENSE channel diagnostics, the V_{REF} V/I, of the VSENSE and ISENSE channels, has to be connected to the TSENSE ADC by setting the COMP_CTL.DIAGT(M) bit. The VSENSE and ISENSE acquisition channels must be disabled to not load the V_{REF} V/I.

The diagnostics is using the external temperature channel configuration/result (ACQ_ETEMP).

Table 5 shows the recommended settings to run the TSENSE channel diagnostics:

Table 5. TSENSE diagnostic recommended settings

Parameter	Setting	Pseudo code	Comment
Pre-requisite			
Mode	Normal mode	`PCR_CTL = OPM_SET_NORMAL;`	

Parameter	Setting	Pseudo code	Comment
D2DFCLK (ACQ Clock)	512 kHz	`PCR_PRESC = BUSCLOCKKHZ;`	Set to achieve D2DFCLK = 512 kHz
Startup trimming	performed	`SYSStartupTrimming();`	
ISENSE channel	disabled	`IsenseDisable();`	Must be disabled to not bias the V_{REF} V/I
ISENSE reference signal	V_{REF} T	`CompCtlDiagIDisable();`	disconnect V_{REF} T from ISENSE
VSENSE channel	disabled	`VsenseDisable()`	Must be disabled to not bias the V_{REF} V/I
VSENSE reference signal	V_{REF} T	`CompCtlDiagVDisable();`	disconnect V_{REF} T from VSENSE
Channel settings			
Decimation	128 (fixed)		4.0 kHz data rate (without chopper) 1.0 kHz data rate (with chopper)
Multiplexer	ETS	`B_ACQ_CTL = (B_ACQ_CTL_ITMENM_MASK| B_ACQ_CTL_ETMENM_MASK| B_ACQ_CTL_ETMEN_MASK);`	External temperature measurement
Chopper mode	On	`ACQETChopEnable();`	
Channel compensation	Off	`ACQTCompDisable();`	Compensation must be off
TSENSE reference signal	V_{REF} V/I	`CompCtlDiagTEnable();`	connect V_{REF} V/I to TSENSE channel
Averaging	4 samples	Result = ¼ * sum(Vn)	Recommended to average in software

Evaluation of the TSENSE diagnostics of seven different samples over temperature are shown in Figure 9. The error between measured value and reference (IFR) value in % is shown.

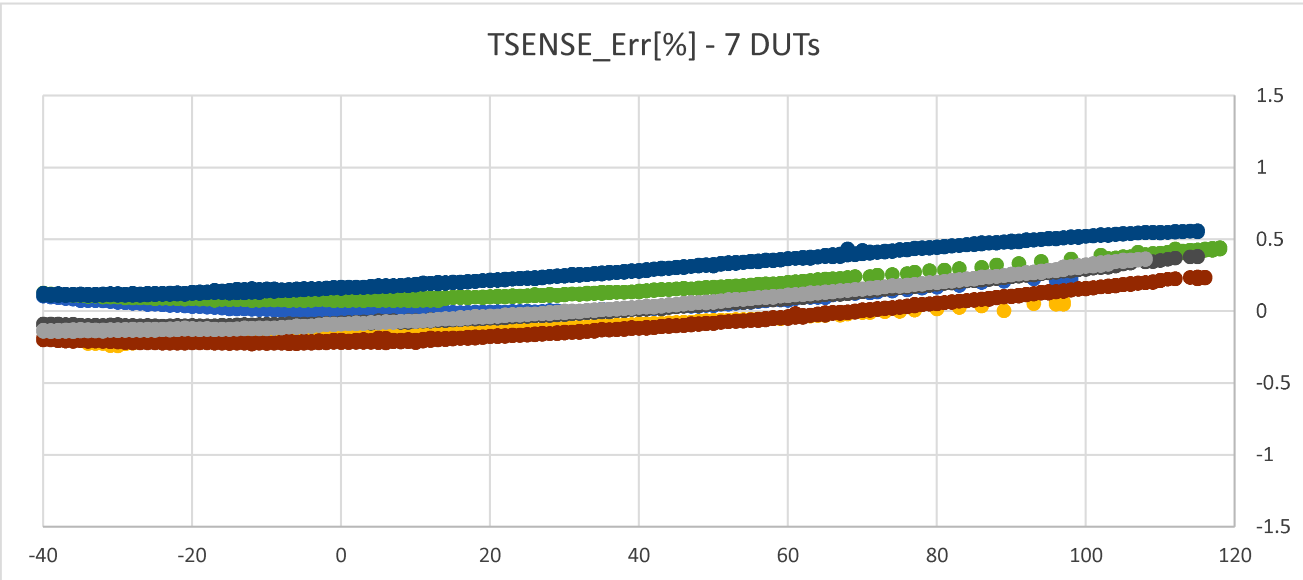


Figure 9. TSENSE diagnostic measurement results over temperature

3.4 Example measurements

Table 6 shows example values for one MM9Z1_638 device (reference only).

Table 6. Example diagnostic values

Parameter	Hex	Dec	Resolution	Vref	Meaning	Nominal
Diag. ISENSE	0x125973	1202547	0.1 µV/LSB	0.1*T	~0.120 V	0.125 V
Diag. VSENSE	0x952C	38188	~25 µV/LSB	0.8*T	~0.954 V	1.0 V
Diag. TSENSE	0xDE13	56851	~19 µV/LSB	0.8*V/I	~1.080 V	1.0 V

The values differ from device to device due to manufacturing variations. The exact values are not critical as the diagnostics is based on relative comparisons (see **Equation 1**).

With the recommended settings the whole diagnostics takes about 47 ms (including PGA_AUTOZERO about 53.5 ms) to execute.

For ISENSE channel:

- Averaging over N = 16 samples, 1.0 kHz ODR, latency 10 ms, PGA auto zero 6.5 ms: $t_{ISENSEDIAG}$ = 1*10 ms + 15*1 ms + 6.5 ms = 31.5 ms

For VSENSE channel:

- Averaging over N = 8 samples, 1.0 kHz ODR, latency 10 ms: $t_{VSENSEDIAG}$ = 1*10 ms + 7*1 ms = 17 ms

For TSENSE channel:

- Averaging over N = 4 samples, 1.0 kHz ODR, latency 2.0 ms $t_{TSENSEDIAG}$ = 1*2 ms + 3*1 ms = 5.0 ms

4 References

Description	URL
MM9Z1_638D1 data sheet	http://www.nxp.com/files/analog/doc/data_sheet/MM9Z1_638D1.pdf
NXP Battery Sensor products	http://www.nxp.com/battery
Wiki Endianess	http://en.wikipedia.org/wiki/Endianness

5 Revision history

Table 7. Revision history

Revision	Date	Description
1.0	7/2016	Initial public release

6 Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/ or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/salestermsandconditions.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — is a trademark of NXP B.V.

the NXP logo — is a trademark of NXP B.V.

Freescale — is a trademark of NXP B.V.

the Freescale logo — is a trademark of NXP B.V.

SMARTMOS — is a trademark of NXP B.V.

Tables

Figures

Contents