EMI EMC Considerations for Energy Meters

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1   Introduction

Energy meters are often tampered with by malicious noise sources to manipulate the energy consumption readings. Thus it becomes a requirement for an energy meter to be fully-functional in challenging noisy electromagnetic environments. Because of this, different *type-tests* are provided in the IEC metering standards. Meter manufacturers must comply with these tests before supplying their product to the market.

It is a joint responsibility of microcontroller designers and PCB designers to provide protection within the metering system, so that the meters are not affected by a noisy environment.

Freescale introduced the MKM34 series of microcontrollers for the single-phase and three-phase metering markets. This series of microcontrollers has a higher immunity against electrostatic discharge (ESD) and high-frequency noise tampers. The MKM34 series of devices produce good results when integrated within a good PCB design.

This application note explains the metering type-tests along with different tampering conditions. It also provides the best practices to create a robust metering system.

Contents

2 Meter type tests

2.1 Impulse/surge voltage test

This test is defined in the IEC 61000-4-5 standard. It is performed to replicate the behavior of lightning on an input line. In this test, a 6 kV impulse voltage is applied ten times with positive polarity and then with negative polarity. The minimum time between pulses must be more than 3 seconds.
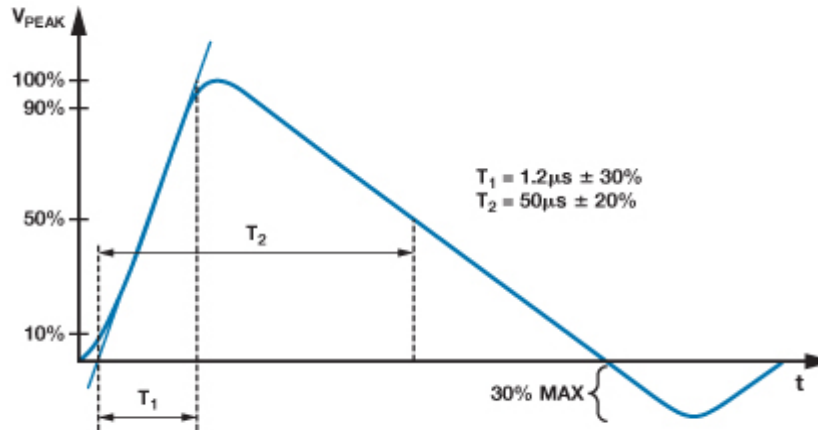

Figure 1. Standard IEC 61000-4-5 wave shape

2.2 Fast transient burst test

This test is defined in the IEC 61000-4-4 standard. It replicates a high voltage condition generated during switching or relay switching. In this test, a continuous impulse of 4 kV is applied on the meter terminal. During this test, the meter must be in operating mode and the operating voltage must be equal to the reference voltage of the meter. There must not be any load connected to the meter—that is, current must not pass through the meter during testing. This test is run for 60 seconds.
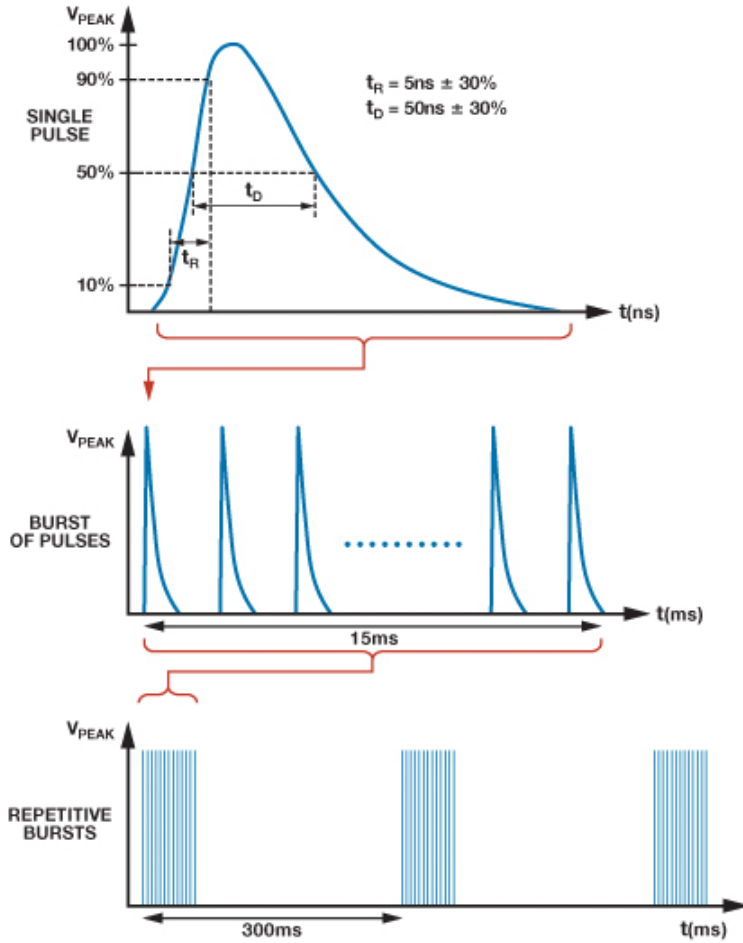
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Figure 2. Standard IEC 61000-4-4 wave shape

2.3   Immunity to ESD discharge test

This test is defined in the IEC 61000-4-2 standard. It replicates a human body model (HBM), machine model, charge device model, and a power ESD model. A continuous high-voltage impulse is applied with 8 kV contact discharge and 15 kV air discharge.
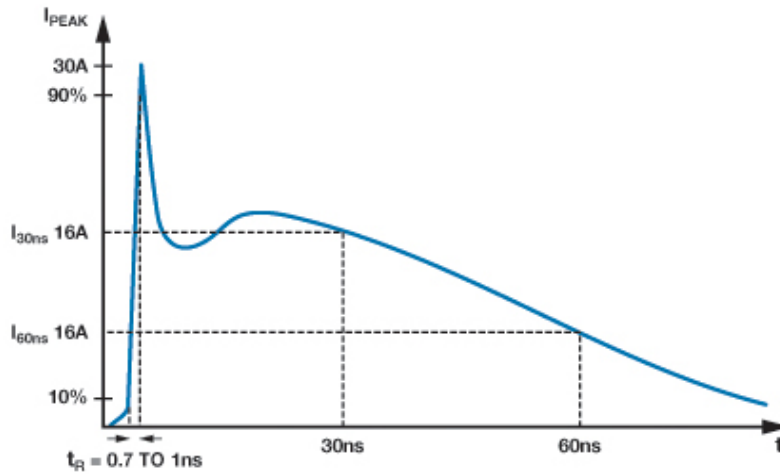
Figure 3. Standard IEC 61000-4-2 wave shape

2.4 Immunity to 35 kV ESD discharge test

This test is performed to evaluate the immunity of the meter to high voltage ESD discharges which are typically used to tamper with an energy meter. In the tampered state, the meter hangs and enables users to consume electricity without the usage registering in the meter. There is no IEC standard defined for this test, however, this test is similar to the IEC 61000-4-2 standard with the discharge voltage level raised to 35 kV. The amount of current generated during discharge is directly proportional to the discharge voltage. Figure 4 shows the electrical characteristics of the electrostatic discharge for the HBM, where series resistance is considered as 330 Ω and capacitance is 150 pF.
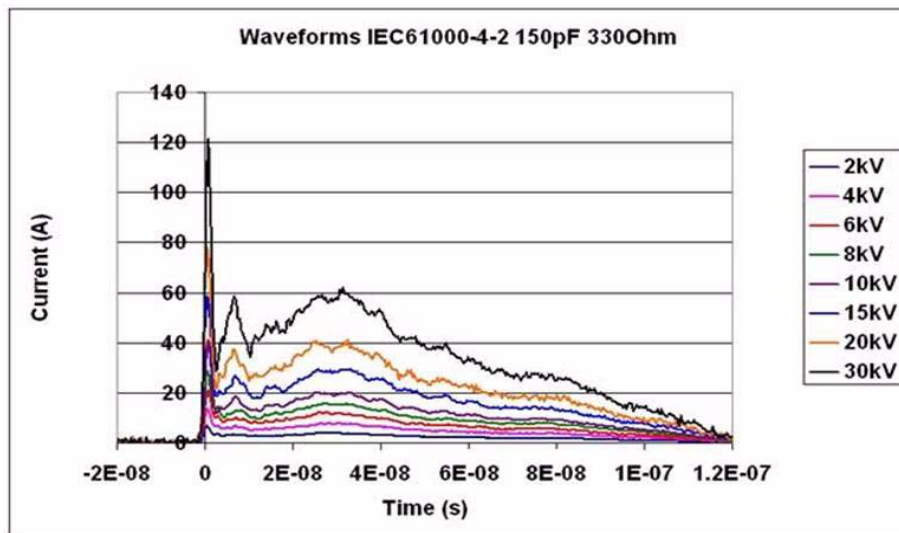

Figure 4. Standard IEC 61000-4-2 current versus discharge voltage

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2.5 AC voltage insulation test

This test is performed to evaluate the insulation of the meter. AC voltage insulation test is further divided in the following two tests:

1. 2 kV AC volt test: In this test, 2 kV AC is applied to all voltage terminals with the current circuit connected on one side and ground on the other.
2. 4 kV AC volt test: In this test, 4 kV AC evaluates additional insulation in meters.

2.6 Immunity to electromagnetic high-frequency fields

This test is defined in the IEC6100-4-3 standard. The purpose of this test is to evaluate the immunity of the energy meter in high-frequency (HF) electromagnetic fields. High-frequency field generators are also used to tamper with energy meters. One of the most common results of these high-frequency fields is that it causes the meter to hang. Electrical standards require a meter to be fully functional and that the application of high-frequency noise must not produce any change in the kWh reading. There are two type-tests to evaluate the immunity of the electromagnetic HF fields, described as follows:

1. **Conducted immunity**: This test evaluates the meter's immunity to high-frequency signals that are directly injected into a system through a conductive path, for example, power line or AMR communication ports. This type of noise is typically present in the frequency band of 150 KHz to 30 MHz.
2. **Radiated immunity**: This test evaluates the meter's immunity to radiated electromagnetic interference. These noise signals travel over air and no physical contact is made between the noise source and the victim, instead these noise signals behave as electromagnetic waves and couple with the signals on the system's PCB. This noise signal is present in the frequency band of 30 MHz to 1000 MHz. This is tested with a field strength of 10 V/m.

2.7 Radio interference test

As discussed in Section 2.6, "Immunity to electromagnetic high-frequency fields," the energy meter is expected to work properly when conductive and radiated noise occurs. The energy meter must not generate its own noise which can affect the functioning of surrounding devices. The following two tests are defined depending upon the noise emitted by the energy meter in the external environment.

1. **Conducted emission:** Noise emitted over conductive media in the range of 150 kHz to 30 MHz.
2. **Radiated emission:** Radiated noise in the range of 30 MHz to 300 MHz.

3 Reasons of system failure during type-tests and tampers

The reasons that a system deviates from its expected behavior during type-tests or tampering are as follows:

1. Mutual inductance
2. Mutual capacitance
3. Antenna effect

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4. High-impedance path for returning currents

The PCB must be designed in such a way that it minimizes mutual coupling or antenna effects within electrical traces on the board and provides the least impedance path for the return current. The return current path plays a major role in defining the electrical and magnetic fields of the PCB. The behavior of PCB's electromagnetic field with the external electromagnetic field determines system performance.

3.1   Mutual inductance

When two coils are within close proximity to each other, then the magnetic field from one coil is linked to the other coil, which results in generation of voltage in second coil. This phenomenon is known as mutual inductance. PCB traces have inductive behavior, therefore they generate magnetic fields for the varying current flowing through them and they also induce the voltage for an external magnetic field. Inductance of PCBs depends on the trace length, which can effectively change the actual signal passing through the PCB traces.

Mutual inductance is defined by following formula:

$$M = K\sqrt{L_1 L_2}$$ **Eqn. 1**

[1] K is the coupling factor
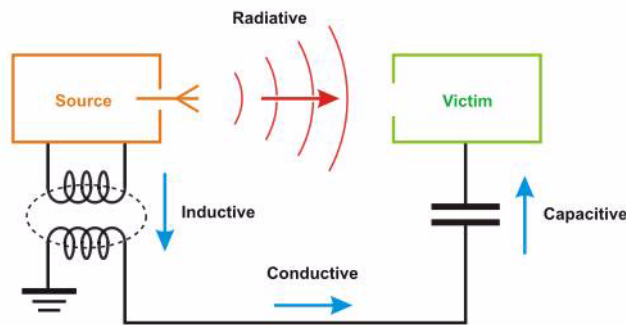[2] L1 and L2 are the self inductance of coils

Figure 5. Different methods of noise coupling

3.2   Mutual capacitance

Mutual capacitance is either intentional or unintentional capacitance that occurs between two charge-holding objects or conductors. In a PCB when two traces are closely spaced together, the air or material separating these traces acts as a dielectric and the traces act as capacitor plates. Any external field can cause capacitance coupling by using air as the dielectric media and induces unwanted noise into the PCB. Similarly, current flowing through the PCB trace can induce noise into the external system by means of mutual capacitance.

Typical capacitance of a PCB trace is defined as:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{D}$$ **Eqn. 2**

[1] *C* is the capacitance, in Farads.

[2] A is the area of overlap of the two plates, in square meters.

[3] ε_r is the relative static permittivity (sometimes called the dielectric constant) of the material between the plates (for a vacuum, $\varepsilon_r = 1$).

[4] ε_0 is the electric constant (ε_0 8.854×10^{12} F m^{-1}).

[5] D is the separation between the plates, in meters.

4 Design techniques used at different levels

To create a robust system, specific design techniques are recommended at different stages of your design. This section provides guidelines to implement these techniques at the system level, within the PCB, and at the circuit level.

4.1 System level

To create a robust system with stronger immunity to tougher environmental EMI and invasive tampering techniques, design the system's chassis so that the meter is isolated from other radiating sources.

4.1.1 Air tight enclosure

Figure 6 illustrates a poor design that enables ESD and electromagnetic noise to penetrate the enclosure.

Side A shows the enclosure has a slit or cut either at a corner or other small area which causes ESD and electromagnetic noise to penetrate the enclosure affecting the performance of the board.

Side B shows a small piece of wire projecting out of the enclosure. This wire exposes the PCB to direct attacks of ESD or conductive noise and also behaves like an antenna for electromagnetic waves catching noise from the surroundings.
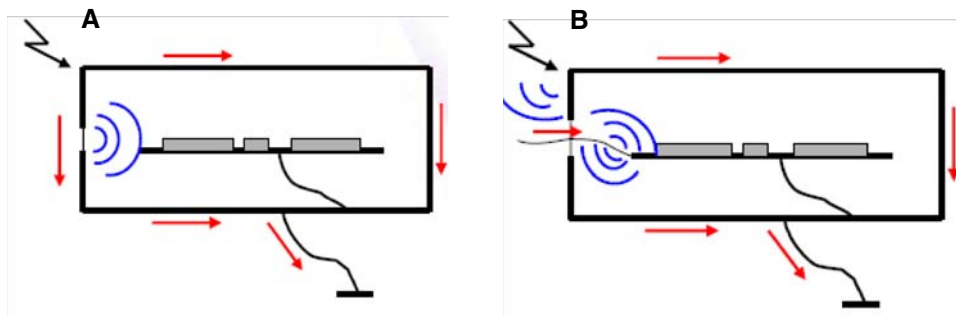

Figure 6. Incorrect enclosure design

The Figure 7 shows the correct design to prevent ESD strikes from entering the PCB area. The enclosure is an insulator and prevents ESD charges and electromagnetic noise from flowing inside. With this design, the only precaution required is to place the device on a surface with a good contact to earth ground, otherwise there is a possibility of ESD shocks due to static charges developed at the outer surface of the enclosure.
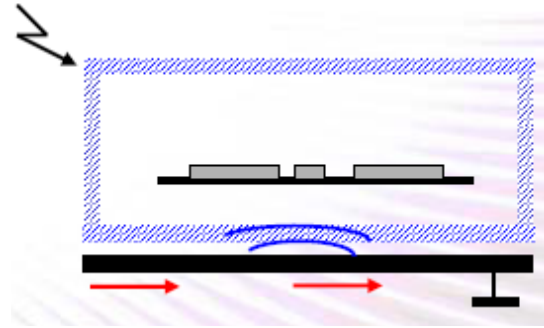
Figure 7. Correct enclosure design

If it is not possible to have a fully enclosed insulator, there are different ways to overcome opening slits, as shown in Figure 8.
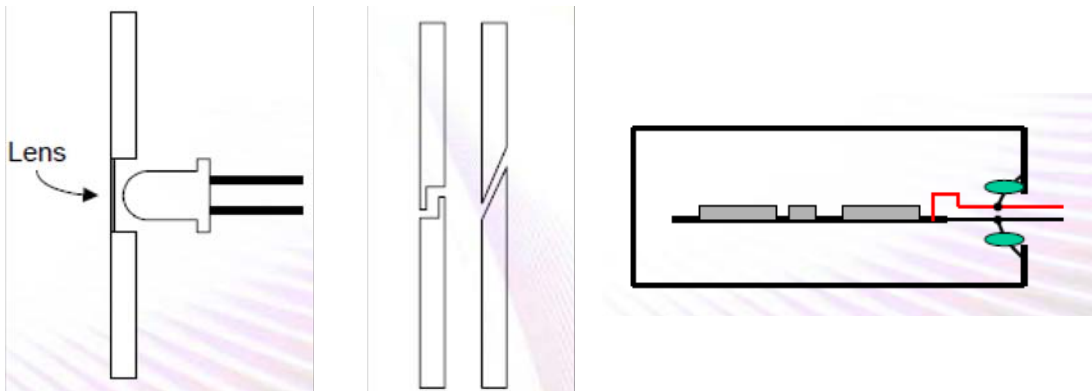

Figure 8. Enclosure slit cover

4.1.2 Wiring harness

All open, non-terminated, and big loop wires act as antennas with long transmission paths, therefore, it is necessary to properly shield the wires and if possible run a return current wire parallel to any long leaded signal wire with either a twisted pair or coaxial wires.

4.1.3 Gap of PCB from the enclosure

The PCB requires sufficient gap from the enclosure, so that static developed on the enclosure does not create an effective electric field within the PCB. If the enclosure is a conductive material, then the PCB must be connected to the enclosure with an insulator arrangement. The component's height must be as low as possible from the PCB and sufficient space must be provided from the inner surface of the enclosure.

4.1.4 Shielding

Shielding is a means to reduce radiated noise from entering or leaving a component, equipment, or system. Shielding decreases radiated emissions from a system and increases the immunity of a system. Shielding is important for a system that contains components such as an SMPS, DC-DC convertor driver, and inverter because these components are sources of RF emissions. In energy meters, components such as the RF transmitter and SMPS power supply must be properly shielded.

There are several factors which affect the performance of shielding, such as:

1. Type of shield
2. Type of shield material and thickness
3. Grounding of the shield
4. Source and victim geometry
5. Compromised shielding

4.2   PCB level

During the PCB design stage, the designer must consider all aspects of electromagnetic intrusions that involve both radiating and conductive EMI intra-systems as well as inter-systems. This section primarily takes into consideration the PCB layout design techniques such as grounding, placement of components, routing, determination of critical signals, analog and digital grounds, and so forth.

4.2.1   Form factor

Form factor must be decided on the basis of a feasibility study which determines the placement and routing of the entire board. The area of the PCB must be sufficient to provide ground, shielding, and the shortest return paths for all signals. The designer must avoid cuts to the PCB surface.

4.2.2   Placement

During the placement stage, designers must identify critical sections on the PCB which can become future EMI sources or victims.

The following are critical for a PCB design:

1. I/O ports—All I/O connectors interfacing with the external world are major sources of ESD and EMI fields. These I/O connectors pass noise from the external surroundings to sensitive sections of the PCB. There must be proper shielding of the I/O connectors and they must be connected to system ground. Critical signal pins must be adjacent to ground pins and each signal connector must be sufficiently grounded.
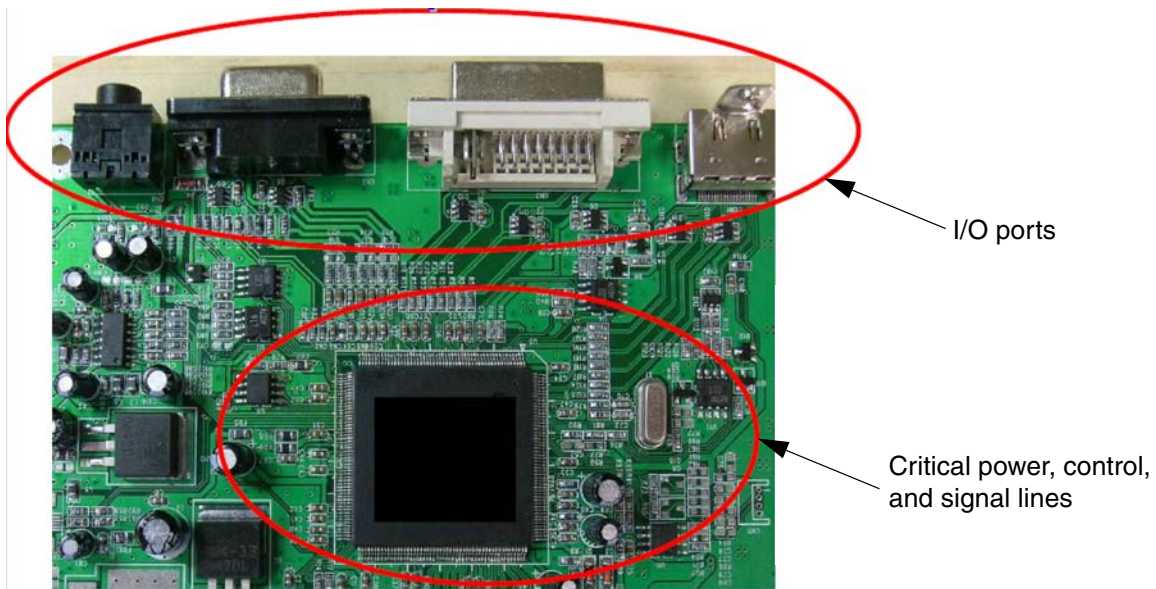2. Critical power, control, clock, and signal lines must be placed as shown in Figure 9.

Figure 9. PCB with sensitive circuitry

3. Placement of microcontroller and sensitive circuits—Place all sensitive circuits at the center of the PCB. Sensitive circuits are susceptible to environmental noise, therefore they must be placed as far away from the PCB edges as possible.

4. Placement of the analog, digital, power, and high-speed sections—Place analog and high speed sections such that there is minimal interference from noise generation circuits such as the digital and power supply sections. The analog, digital, power, and high-speed circuits must have their own shortest return paths directly under or adjacent to the signal paths. See Figure 10.
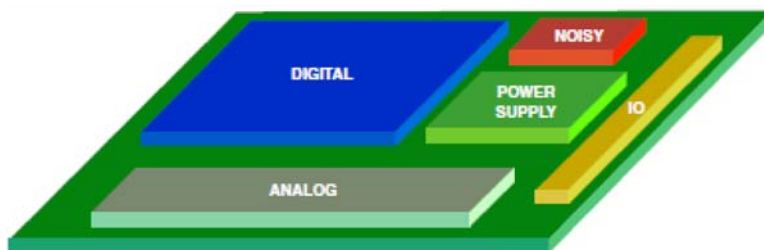

Figure 10. Recommended placement

4.2.3   Layout

The PCB layout plays an important role to define the EMI behavior of the system. With an increase in competition there is a strong emphasis on low-cost systems, so systems are required with a minimum number of PCB layers and the smallest form factor. It is critical to design a layout such that the PCB provides high immunity from external noise sources. This section defines a variety of layout techniques for different system interfaces such as crystal, LCD, analog, power supply, and so forth.

4.2.3.1 Crystal layout

The crystal is the most sensitive and critical part of the system because it is the clock source of the entire controller or system. Crystals are very susceptible to ESD and EMI noise because of their low-amplitude signals. Poorly designed PCBs cause the system performance to downgrade because of unwanted jitter or damping of the oscillation of crystal.

Use the following guidelines to design the crystal section:

- Ensure the crystal is mounted next to the controller. Also, ensure that EXTAL and XTAL traces are as small as possible to act as a lumped circuit with minimum length to avoid noise.
- Ensure that the crystal receives a clean ground underneath and that this ground is connected with the microcontroller ground. See Figure 11.
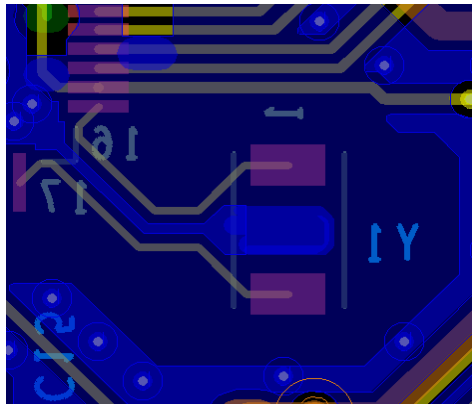

Figure 11. Crystal layout

- Maintain sufficient gap, about 30 mils, between the crystal, the crystal's traces, and other circuitry.

4.2.3.2 Liquid Crystal Display (LCD) layout

LCD interfaces are susceptible to EMI because of the LCD glass capacitance and the increased number of bias voltages. The voltage difference between back planes and front planes becomes more prone to noise and produces incorrect results. Segmented LCDs may have 20 to 30 lines running in parallel from the driver to the LCD glass thereby making the LCD interface sensitive to external noise.

The following list describes the guidelines for an effective LCD layout with examples shown in Figure 12 and Figure 13:

- To minimize the transmission line effect, LCD lines must be routed as straight and short as possible. Parallel routing of LCD traces increases the effective length of the traces and becomes comparable to transmission lines. Because of this effect, it becomes difficult to maintain the characteristic impedance throughout, therefore causing reflections to occur with the result of a ringing signal.
- If the LCD lines need to be routed to a different layer, ensure that they are routed with a minimum number of vias and are accompanied by ground lines throughout the path to minimize coupling.
- Providing series resistance on the lines enables termination of the transmission lines and current limiting in scenarios such as ESD and over current situations as shown in Figure 13.

- LCD lines must be accompanied with guard traces alongside to couple noise from the LCD trace to ground. If that is not possible, then maintain a gap of at least twice the width between the traces as shown in Figure 12.
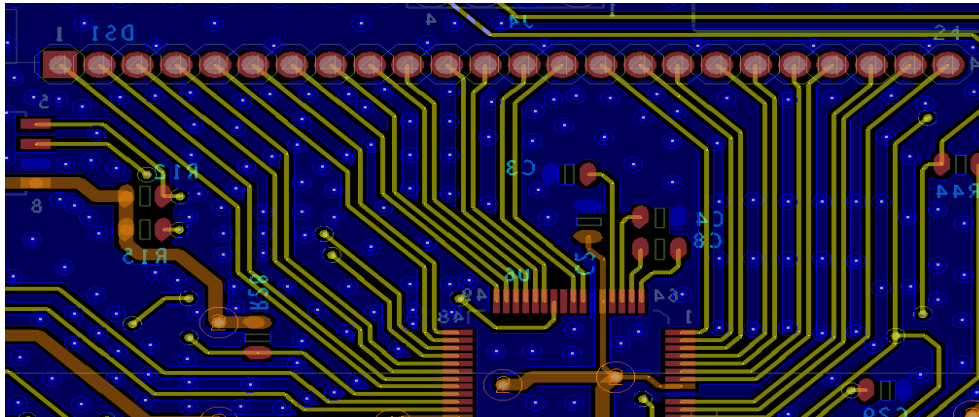
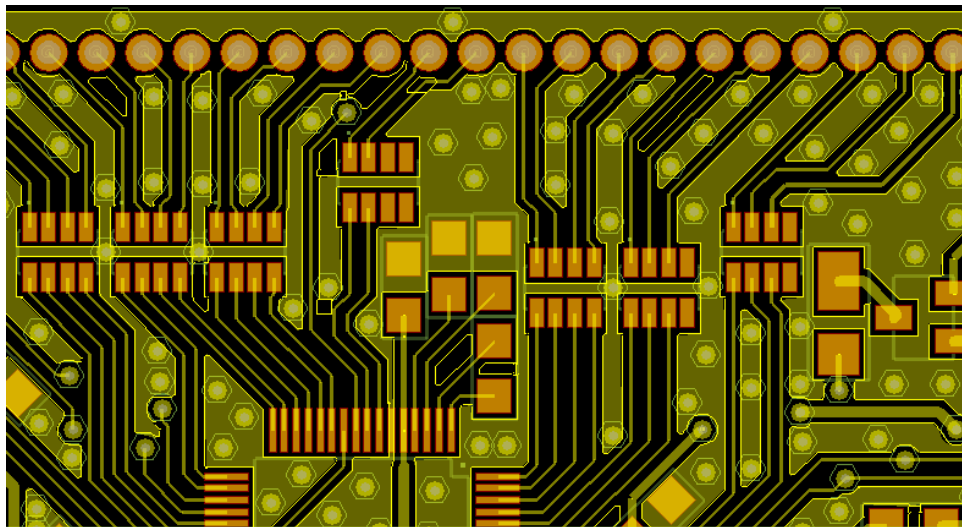

Figure 12. LCD routing technique with ground grads

**Figure 13. LCD routing technique with series resistors**

4.2.3.3 Analog layout

The design of the analog layout on the PCB is critical and defines the accuracy and performance of a system; especially within the energy meters. The analog section contains low-amplitude analog signals that are sampled by ADCs, therefore, any noise can disturb the actual analog signal and decrease the SNR which results in faulty digital values. A good layout prevents coupling of external signals, as well as on-board noise to analog signals.

The following list provides guidelines for an analog layout:

- Analog signals are sensitive so care must be taken to route these signals in isolation to other digital (switching) signals.

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- A proper ground reference must be provided from the start to the end of the signal without any cuts or splits.
- All analog signals must be spaced at least twice the width from each other and from other switching signals.
- Route all differential signals with minimum trace lengths, and minimum vias and corners.
- Maintain the parallelism (skew matching) between D- and D+ of a differential signal. These traces must be the same length. Route these differential signals close enough to each other to reject common mode noise.
- Space between differential signals must be less than or equal to one width.
- Spacing of any differential pair from any other signal must be more than twice the width.
- Additional ground can be provided between the differential pair and other signals.
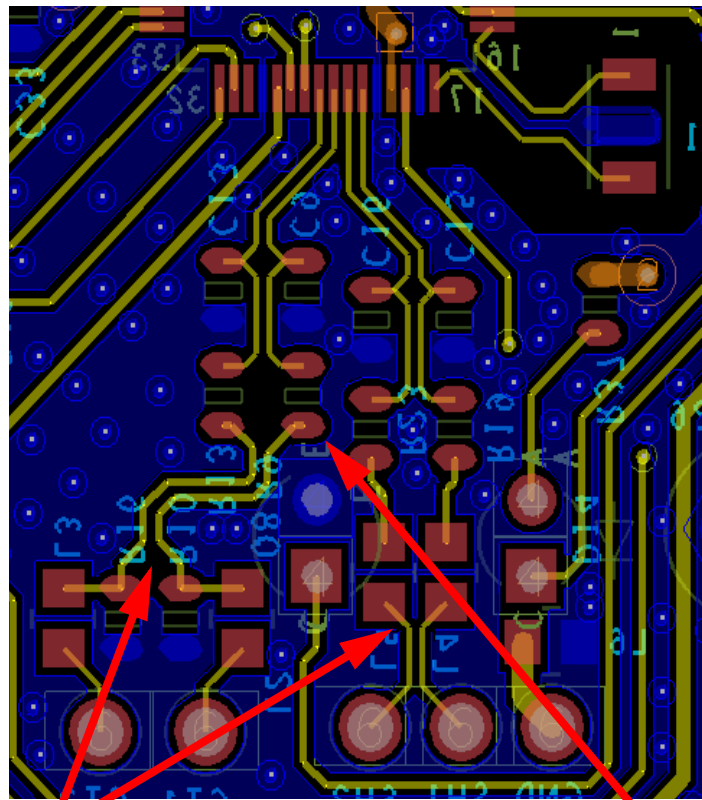
Analog routing   **Ground between two traces**

Figure 14. Differential routing

4.2.4   Power supply and distribution

The power supply is a major area of concern for applications such as metering because of the involvement of analog circuitry for different measurements. The performance of the analog circuit is driven by the Power Supply Rejection Ratio (PSRR) factor and even a small amount of noise in the power supply causes the analog section to be vulnerable. Therefore, noise filtering of the power supply and decoupling of noise

to load circuits is important. During tampering, intentional ESD strikes are injected through AC power lines which directly spread into the entire system. This noise is conductive in nature.

The following two approaches are used to suppress noise in the power rails of the system:

1. Filtration of noise entering into the power supply:

   The designer must ensure that any noise or unwanted electrical transients are suppressed before entering the power supply section. This is achieved with the use of electrical components such as MOVs, high-voltage bidirectional zener or TVS diodes, and filters such as common mode or differential mode choke.

2. Decoupling of noise at loads:

   Even when using noise filtering techniques within the power supply, noise generates on power rails because of the switching components. Therefore bypass and decoupling capacitors must be used in the power supply section to enable smooth and filtered power and to prevent high-frequency transients from entering.

4.2.5 Grounding

Grounding is one of the most critical and difficult concepts in the system design. While the following electrical concepts may appear basic, there is no procedural approach that guarantees linear graph of improvements in the system performance when every step is followed.

Complete ground planes must be provided for all sensitive signals and switching signals. Cuts or splits must be avoided near these switching signals. If a signal return path is increased, it creates a larger loop which is then susceptible to a magnetic field.

The following list provides guidelines to ensure a better ground for the system:

- Allocate ground in all layers when no separate ground plane is provided.
- Provide a common ground for both the analog and digital sections and separate the regions for analog and digital signal routing, so that any switching noise within the digital signal does not affect the analog signal.
- Stitch all ground shapes in different layers with as many vias as possible.
- When placing ground on a signal layer, ensure that the impedance of the original traces remain unaffected because addition of ground can mismatch the impedance of signal traces to the load/source, which can result in reflection of the signal.

4.3 Circuit level

This section describes the selection of components and filter circuits to be considered to avoid noise penetration from various sources.

4.3.1 Capacitor selection

Capacitors play a major role to create a robust system. Proper selection of capacitors avoids many EMI issues within the design. Capacitors are used at different levels within the circuit, described as follows:

1. **Bulk capacitor**: Bulk capacitors are used to shunt AC noise and prevent high transients from entering the system. Bulk capacitors must be placed near the voltage regulator and their value must be based on the system frequency. Typically 10 µF to 100 µF capacitors are used. These bulk capacitors act as a power reservoir to load.

2. **Decoupling capacitor (decap)**: Decaps are used to eliminate noise generated by high frequency switching of the active elements and the surrounding switching devices. They also provide high current requirements of the active devices for short durations. They prevent high frequency noise from returning on the voltage line. They must be placed near active devices so that the inductive nature of PCB traces cannot create unwanted mutual inductance.

4.3.2 Ferrites selection

Ferrites are a type of inductor which provide impedance for high-frequency signals and are typically used to suppress high-frequency noise components. In energy metering, the power cable creates conductive noise which is coupled with the PCB at current transformers and shunts connection points, thus ferrite beads are used to suppress or remove noise. Figure 15 illustrates the example of ferrites selection—that is, the circuit inductor L2 and L3 are used.
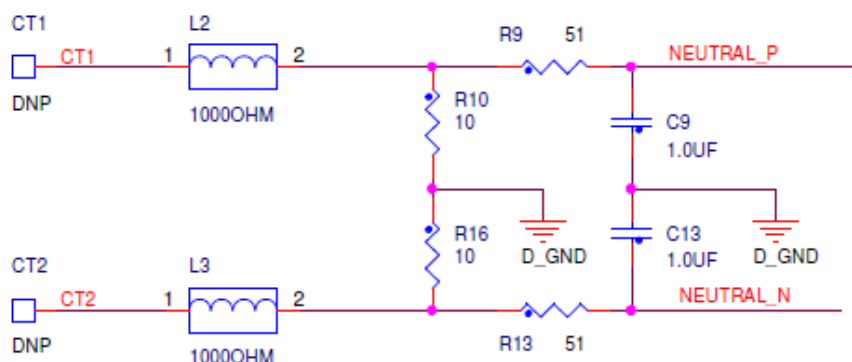

Figure 15. Ferrite bead as noise filter

4.3.3 Filter design

A filter works by creating discontinuity in the impedance detected by a signal travelling along a conductor. Higher discontinuity offers greater attenuation. Various types of filters are used to attenuate unwanted signals. There are different types of filters available and the choice of filter is determined by the types of electronic components used, such as R-only, L-only, RC, and LC. Simple R and L filters create a series of high-impedance paths and must be used when the impedance of unwanted signals is low. C-only filter is used when the impedance of unwanted signal is high. An RC filter is used when a DC or low-frequency signal from a low-source impedance is input to a high-impedance circuit. LC filters can be used to prevent high-frequency noise from entering into the system.

4.3.4 ESD protection components

It is not always possible to design a microcontroller such that it completely prevents high ESD (up to 35 kV) because of shrinking technology size. Integrating ESD protection circuits increases silicon space and increases cost when compared to external ESD protection components. Most MCUs are validated using human body model (HBM), machine model (MM), and charge device model (CDM) standards up to 2 kV. These standards define only a limited subset of electrical behavior which may not replicate real-life scenarios.

In the metering market, ESD strikes are used maliciously to cause malfunction or to tamper with electrical meters, so metering MCUs require external ESD protection components. Commonly used ESD components are transient voltage suppressor (TVS) and metal oxide varistors (MOV). Special care must be taken when deciding which circuit protection device to use. The wrong selection will not only be ineffective, but can also interfere with the normal operation of the circuit.

4.3.4.1 Transient Voltage Suppressor (TVS)

Transient voltage suppressors operate by shunting excess current when the induced voltage exceeds the avalanche breakdown potential. These are clamping devices that suppress overvoltages above the breakdown voltage. Typical of clampling devices, TVSs automatically reset when the voltage returns to normal condition. The circuit protection device must provide the following characteristics for transient voltage suppression in systems:

- Extremely fast response time within the range of 10–100 ns.
- Low-clamping and operating voltages.
- Capacity to handle high-peak ESD currents.
- Ability to remain undamaged by repetitive ESD strikes.
- Minimal size.
- Minimal reverse leakage current.

TVSs can be used on the power rails near the decoupling and bulk capacitors.

4.3.4.2 Metal Oxide Varistor (MOV)

A varistor is an electronic component with a *diode-like* nonlinear current—voltage characteristic. Varistors are primarily used to protect circuits against excessive transient voltages by incorporating them into the circuit in such a way that, when triggered, they will shunt the current created by the high-voltage away from sensitive components. A varistor is also known as voltage-dependent resistor (VDR). A varistor withstands significantly increased current when high voltage is applied. A varistor remains non-conductive as a shunt-mode device during normal operation when the voltage across it remains well below its *clamping voltage*, thus varistors are typically used for suppressing line voltage surges. However, a varistor may not be able to successfully limit a very large surge from an event, such as a lightning strike when the energy involved is many orders of magnitude greater than it can handle. In energy meter applications, these are used at the input power lines.

5 Conclusion

When all the design considerations presented in this application note are applied, metering system performance will be enhanced. These techniques are implemented in single-phase and three-phase energy meter reference design based on MKM34 and results in a robust system passing all known type-tests and tampers.

6 References

The following references are available on freescale.com:

1. *Effective Printed Circuit Board Design: Techniques to Improve Performance* (document AMF-ENT-T0040)
2. *Designing for Board Level Electromagnetic Compatibility* (document AN2321)

7 Revision history

Revision Number	Date	Description of Change
0	06/2014	Initial release

Document Number: AN4941
Rev. 0
06/2014