

# Schematic and PCB Layout Guidelines for Digital Signal Controllers

by: Mohammad Kamil

## 1 Introduction

This application note provides guidelines for Printed Circuit Board (PCB) layouts for systems using Freescale Digital Signal Controllers (DSC), plus provides additional circuit and component (resistor, capacitor) recommendations.

## Contents

1	Introduction .....	1
2	Test pins on DSC device (JTAG) .....	2
3	Power supply layout .....	3
4	Terminate all unused DSC device pins.....	4
5	Analog input pins.....	4
6	Use an external crystal oscillator .....	5
7	References .....	5
8	Revision history .....	6

## 2 Test pins on DSC device (JTAG)

Freescale DSC devices include an Enhanced On-Chip Emulation (EOnCE) module, which is used to debug application software running on the chip. JTAG/EOnCE provides unobtrusive real-time debugging that is independent of processor speed. With the 56F80x core, the JTAG/EOnCE port can also be used to program the internal Flash memory EOnCE module.

**Table 1.** JTAG/OnCE pins

Pin	After reset, the default state is	Description
Test Data Input (TDI)	TDI	TDI is sampled on the rising edge of TCK and has an internal pullup resistor.
Test Data Output (TDO)	TDO	TDO is driven in the shift-IR and shift-DR controller states, and it changes on the falling edge of TCK.
Test Clock Input (TCK)	TCK	TCK is connected internally to a pullup resistor. A Schmitt trigger input is used for noise immunity. NOTE: Always tie the TCK pin to $V_{DD}$ through a 2.2 k $\Omega$ resistor.
Test Mode Select Input (TMS)	TMS	TMS is sampled on the rising edge of TCK and has an internal pullup resistor. - If you need to keep an on-board debug capability, always tie the TMS pin to $V_{DD}$ through a 2.2 k $\Omega$ resistor. -If you do not need to keep an on-board debug capability, then directly tie the TMS pin to $V_{DD}$ .
RESET or RESETB	RESET	A direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity.  The internal reset signal is deasserted synchronously with the internal clocks after a fixed number of internal clocks.

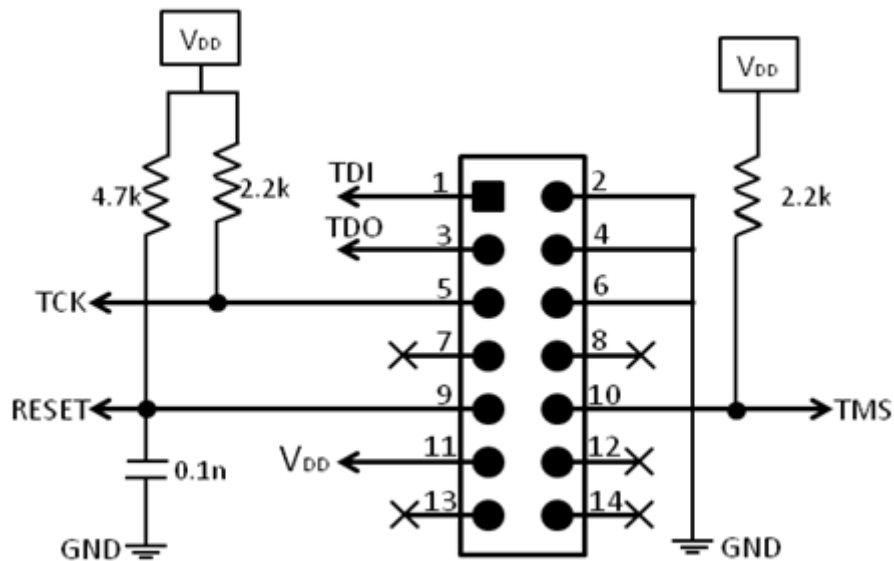


Figure 1. JTAG connector

- If the device will be used in a noisy system, then connect an external RC circuit to the RESET pin. The resistor value should 4.7 to 10 k $\Omega$ ; the capacitor value should be 0.1 to 4.7  $\mu$ F.
- To improve noise transient immunity in noisy environments, configure the RESET pin as GPIO output during normal operations.
- If a JTAG converter is not present, then add a 2.2 k $\Omega$  external pullup on the TMS pin of the JTAG port, to keep the device in normal operating mode (and not in test mode).

### 3 Power supply layout

This section describes schematic and PCB layout recommendations for the auxiliary power supply used to power a DSC:

- To avoid internal device stress,  $V_{DD}$  and  $V_{DDA}$  should not differ by more than 0.1 V.
- Provide low-impedance paths from the board power supply to each  $V_{DD}$  pin on the device, and from the board ground to each  $V_{SS}$  (GND) pin.
- Use two capacitors at  $V_{DD}$  and  $V_{SS}$  pins: an approximately 10  $\mu$ F tantalum capacitor plus a ceramic capacitor. Ceramic capacitors (0.01–0.1  $\mu$ F) should be positioned as near as possible to the package  $V_{DD}$  pins. It is recommended to place one ceramic capacitor on each of the  $V_{DD}/V_{SS}$  pairs, including  $V_{DDA}/V_{SSA}$ . Ceramic and tantalum capacitors usually provide better tolerances.
- The printed circuit traces that connect to the chip's  $V_{DD}$  and  $V_{SS}$  (GND) pins should be as short as possible. If a through-hole is used, then ensure that the capacitor leads are as short as possible.
- To stabilize the core voltage regulator output required for proper device operations, connect a 2.2  $\mu$ F or greater bypass capacitor between each VCAP pin and  $V_{SS}$ . Ceramic and tantalum capacitors are recommended.
- For high frequency signals, minimize PCB trace lengths.

- When calculating capacitive loads at  $V_{DD}$ , consider all device loads on  $V_{DD}$ , as well as parasitic capacitance due to PCB traces. This is critical in systems with higher capacitive loads, which could create high transient currents in  $V_{DD}$  and  $V_{SS}$  circuits.
- Take special care to minimize noise levels on the  $V_{REF}$ ,  $V_{DDA}$ , and  $V_{SSA}$  pins.
- To eliminate PCB trace impedance effects, each ADC input should have an RC filter (33 pF and 10  $\Omega$  RC minimum).
- Use separate power planes for  $V_{DD}$  and  $V_{DDA}$ , and separate ground planes for  $V_{SS}$  and  $V_{SSA}$ . Connect the power planes (analog and digital) and ground planes as near as possible to the auxiliary power supply output capacitors. If analog and digital circuits are powered by the same power supply, then connect a small inductor or ferrite bead in between  $V_{DD}$  and  $V_{DDA}$ . Short the digital and analog ground at the board to a solid ground connection (preferably a ground plane). If a ground plane is not possible, then route to ground returns using wide short connections for the lowest ground impedance.
- Separate analog and noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. To isolate an analog signal trace from digital traces, place an analog ground trace around an analog signal trace.

## 4 Terminate all unused DSC device pins

This section describes the information about how to terminate the unused pins of DSC.

- For reliable device operation, tie all unused pins to an appropriate voltage level, or configure the unused pins as a digital output pins with logic zero output and tie those digital output pins to ground directly.
- After reset but before the I/O pins are initialized, all I/O pins are tristated.
- To tristate any GPIO pin without switching that pin to input mode, use open-drain mode for that pin. This capability is useful for keypad interfaces.

## 5 Analog input pins

For motor and power conversion designs, use special care for the analog feedback circuit layouts.

- If a pair of analog channels must be converted simultaneously, then those analog channels must be connected to different ADC blocks (ADCA and ADCB).
- Differential inputs should be routed together or in parallel with ground shielding.
- There is an internal clamping circuit for every ADC input (except for the 56F8006/2 devices), but the required injected current should be less than 3 mA. To do this, use an input RC low-pass filter with a suitable current limiting resistor.
- If injected current to an ADC pin is more than 3 mA, or if the analog voltage may go beyond  $V_{DD}$  and ground (for example, during a short circuit or overload, the current sense analog voltage might shoot up to much higher value), then use protection diodes to connect the analog input to ground and  $V_{DD}$ .

## 6 Use an external crystal oscillator

For accurate clocking in your DSC system, an external crystal oscillator should be used, with special care for its PCB layout:

- Place the crystal oscillator and its load capacitor as near as possible to the XTAL and EXTAL pins of the DSC device.
- For better clock performance, have ground traces surrounding the crystal oscillator circuit, but do not create a ground "island".
- The trace connecting the crystal oscillator circuit (and its load capacitor) to the DSC device pin should be straight and short, with no via used (best case) or minimal via used (if necessary).
- The load capacitor ground should connect directly to the V<sub>SS</sub> pin of the DSC device using a trace and not to the nearby ground plane.

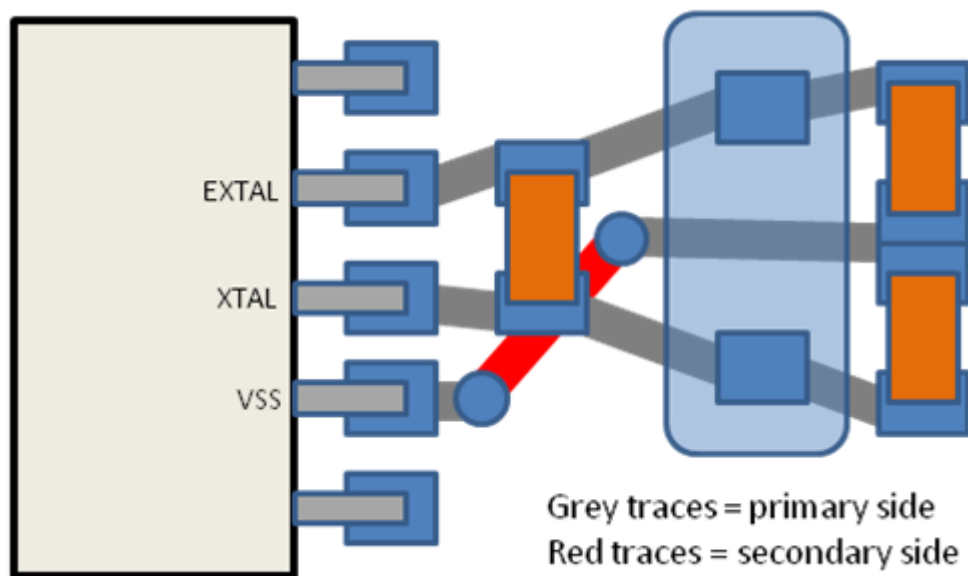


Figure 2. Crystal oscillator layout

## 7 References

The following references are available on [freescale.com](http://freescale.com):

- Freescale Digital Signal Controllers datasheets.
- *Programming On-Chip Flash Memories of 56F80x Devices Using the JTAG/OnCE Interface Application Note* (document AN1935)

## 8 Revision history

Revision number	Date	Substantial changes
0	11/2013	Initial release
1	02/2014	Editorial changes



**How to Reach Us:**

**Home Page:**

[freescale.com](http://freescale.com)

**Web Support:**

[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Documents Number: AN4826  
Rev. 1  
02/2014

