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MPC5643L Hardware Requirements

by: Anita Maliverney, Masato Oshima, and Eugenio Fortanely

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1 Introduction

The MPC5643L microcontroller is based on the Power Architecture® and targets electric power steering, chassis, and safety applications that require a high safety integrity level. The host processor core of the device is a member of the e200z4 Power Architecture compatible core family.

For more details, see MPC5643LRM: MPC5643L Reference Manual and MPC5643L Data Sheet, available on **freescale.com**

2 Power supplies

The on-chip voltage regulator module provides the following features:

- Single high-supply requires nominal 3.3 V.
- An external ballast transistor is used to reduce dissipation capacity at high temperature but an embedded transistor can be used if power dissipation is maintained within package dissipation capacity (lower frequency of operation).
- All I/Os are at same voltage as external supply (3.3 V nominal).
- The core voltage supplies are not under user control. The core supplies are generated by the on-chip voltage regulator.

For details on the power supply pin numbers and recommended operating voltage conditions, see MPC5643L Data Sheet, available on **freescale.com**.

2.1 Power management unit (PMU) overview

The PMU generates the 1.2 V core logic supply from a 3.3 V (nominal) input supply by means of a linear voltage regulator driving an external NPN bipolar transistor (emitter-follower configuration) or an internal pMOSFET.

The PMU always starts up using the internal ballast transistor. It then executes an automatic procedure that detects (during the system reset phase) whether an external ballast transistor is operational. If a functional external ballast transistor is detected, the power is supplied to the system through the external transistor only. The information whether the internal or the external ballast transistor is used is available via Configuration Status Bits of the PMUCTRL status register (PMUCTRL_STATUS[CTB]).

The operating voltages are monitored by a set of on-chip supervisory circuits to ensure that this device works within the correct voltage range. These circuits are:

- Low-Voltage Detector (LVD)
- High-Voltage Detector (HVD)
- Comparators

Main digital low- and high-voltage monitoring circuits are tested by integrated self-test circuitry. The Voltage Regulator, IO and flash-dedicated low-voltage monitoring circuitries which are called LVD_MAIN1, LVD_MAIN2, and LVD_MAIN3 are redundant in order to improve the safety coverage. The LVDs and the comparators provide their output signals to the Reset Generation Module (MC_RGM) and to the Fault Collection and Control Unit (FCCU).

See MPC5643LRM: MPC5643L Reference Manual and MPC5643L Data Sheet, available on **freescale.com**, for more details on the PMU Voltage Architecture.

The 3.3 V supply domains are called High-Voltage (HV) domains, while the 1.2 V supply domains are called Low-Voltage (LV) domains.

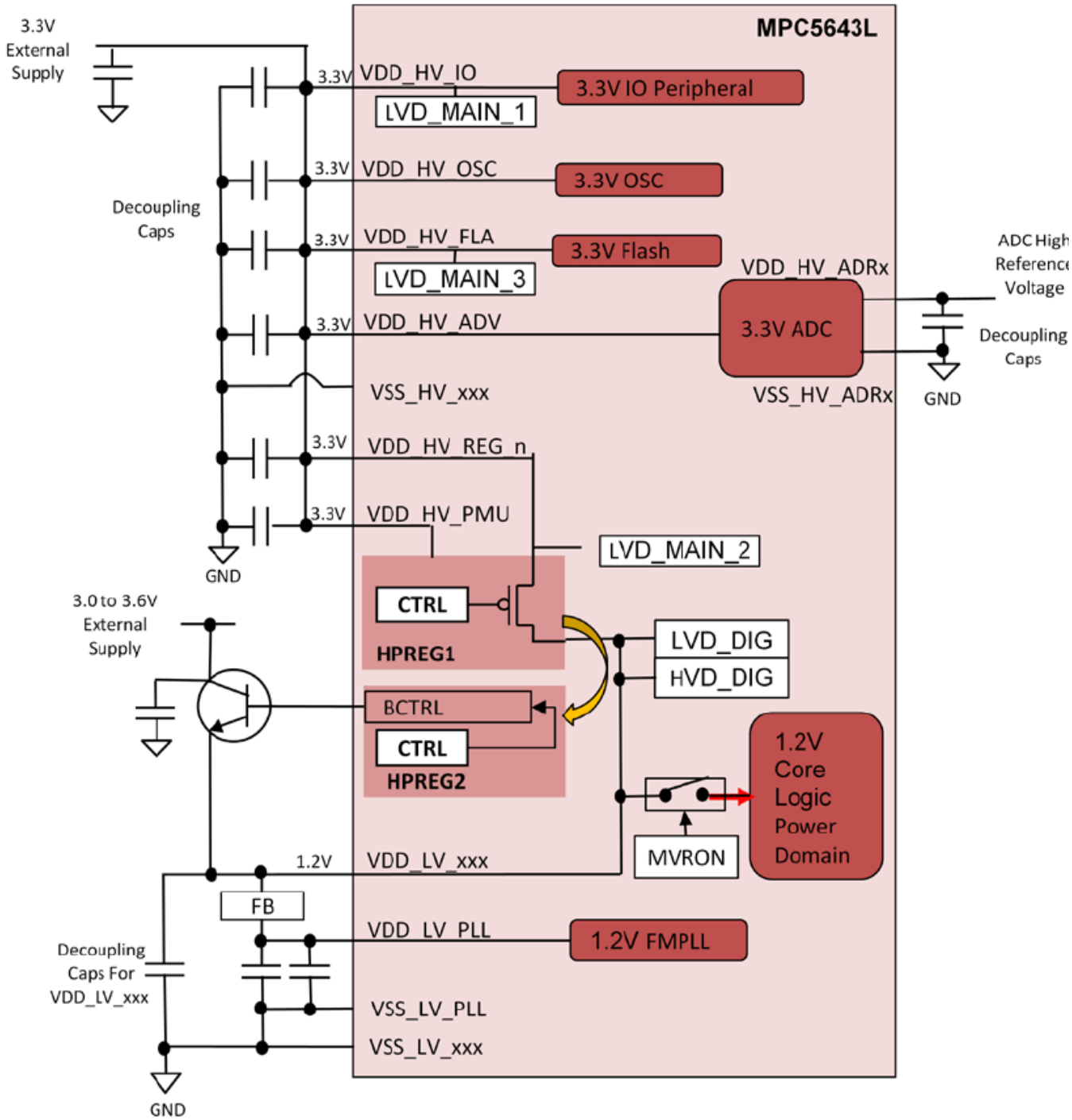


Figure 1. MPC5643L power domains

High-voltage (3.3. V) domains, as shown in Figure 1 include:

- I/O supply domain VDD_HV_IO
- Oscillator supply domain VDD_HV_OSC
- Flash supply domain VDD_HV_FLA
- ADC converter supply domain VDD_HV_ADV
- ADC converter reference voltage domain VDD_HV_ADRx
- VDD_HV_PMU for HPREG1 and HPREG2

High-voltage (1.2 V) domains, as shown in Figure 1 include:

- Core logic supply domain VDD_LV_COR / VDD_LV
- FMPLL supply domain VDD_LV_PLL

3 Voltage regulator operating configurations

Depending on the application's requirements concerning ambient operating temperature range and the associated power dissipation from the internal 3.3 V to 1.2 V voltage regulator, two operating modes of the voltage regulator can be selected:

- Internal ballast transistor mode: Main voltage regulator HPREG1 and the associated internal ballast transistors are used to drive the internal 1.2 V power domain. See Figure 2.
- External ballast transistor mode: Secondary voltage regulator HPREG2 and the connected external ballast transistor is used to drive the internal 1.2 V power domain. See Figure 3.

It is not allowed to directly connect the VDD_LV pins to an external 1.2 V supply.

3.1 Voltage regulator using internal ballast transistor mode

The internal 3.3–1.2 V voltage regulator based on the three integrated ballast transistors are used to supply the core logic. In this mode, no external ballast transistor needs to be connected to the BCTRL pin. See Figure 2. The second voltage regulator HPREG2 is not used in this mode. The device always powers up using the main voltage regulator HPREG1 with the internal ballast transistors. HPREG1 can supply up to 450 mA. If the device temperature doesn't exceed T_J, the operation based on only HPREG1 is valid. Therefore, care has to be taken about the maximum ambient temperature and the maximum power dissipation because power is fully dissipated in the internal HPREG1 in this mode.

In this mode, power dissipation is calculated using the following equations:

$$P_D = 3.3V * I_{DDMAX}$$

$$T_J = T_A + P_D * \theta_{JA}$$

where P_D = power dissipation

T_J = junction temperature

T_A = ambient temperature

θ_{JA} = Thermal resistance from junction to ambient [°C/W]

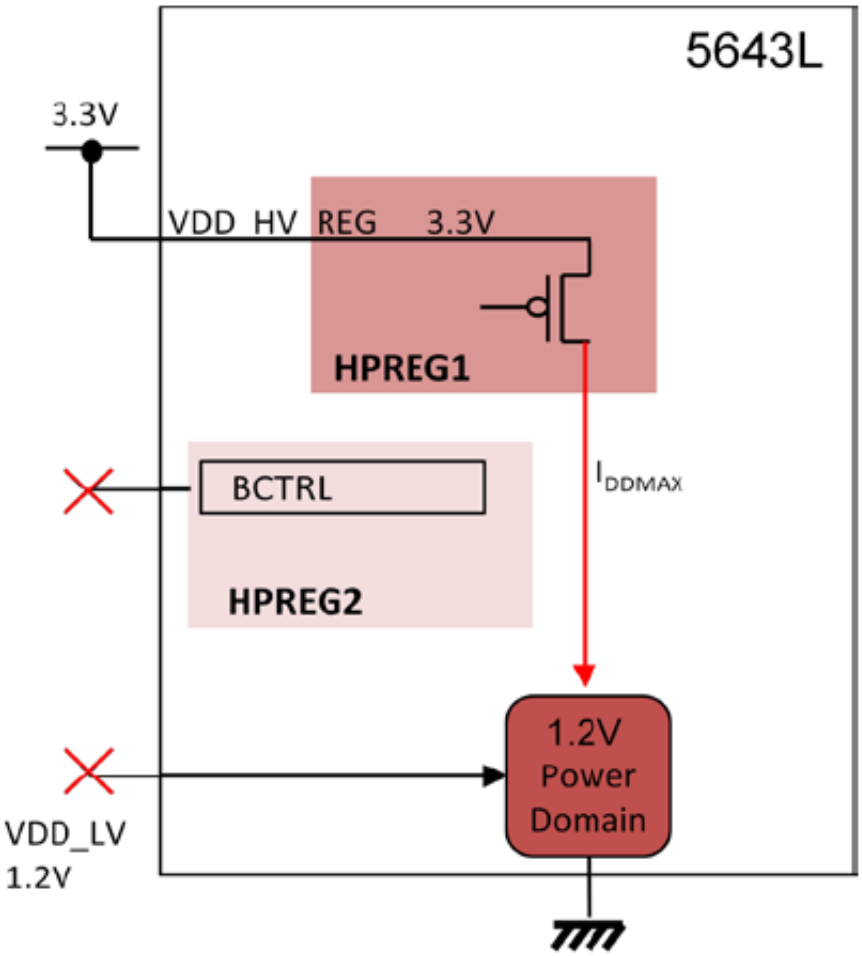


Figure 2. MPC5643L using internal ballast transistor

3.2 Voltage regulator using external ballast transistor

In this mode, the internal core supply voltage of 1.2 V is generated by the external NPN transistor which is controlled by the second voltage regulator on the device, HPREG2. The main voltage regulator, HPREG1, is used during startup phase. After the HPREG1 regulator reaches its target output value, HPREG2 is switched on. After that, the device determines whether an external NPN transistor is connected and selects the operation mode. If the external ballast transistor is detected, the device makes a transition from HPREG1 to HPREG2 automatically. See Figure 3.

NOTE

VDD_HV_REG_x signals must be connected to a 3.3V power supply to provide power to HPREG1 during the startup phase.

The power dissipation generated inside the device is less in this mode than in the internal ballast mode, as the main power is dissipated in the external ballast transistor regulating the 3.3 V down to the core voltage of 1.2 V.

Therefore in this mode, power dissipation P_D can be calculated using the following equations.

$$P_D = 1.2V * I_{DDMAX}$$

$$T_J = T_A + P_D * \theta_{JA}$$

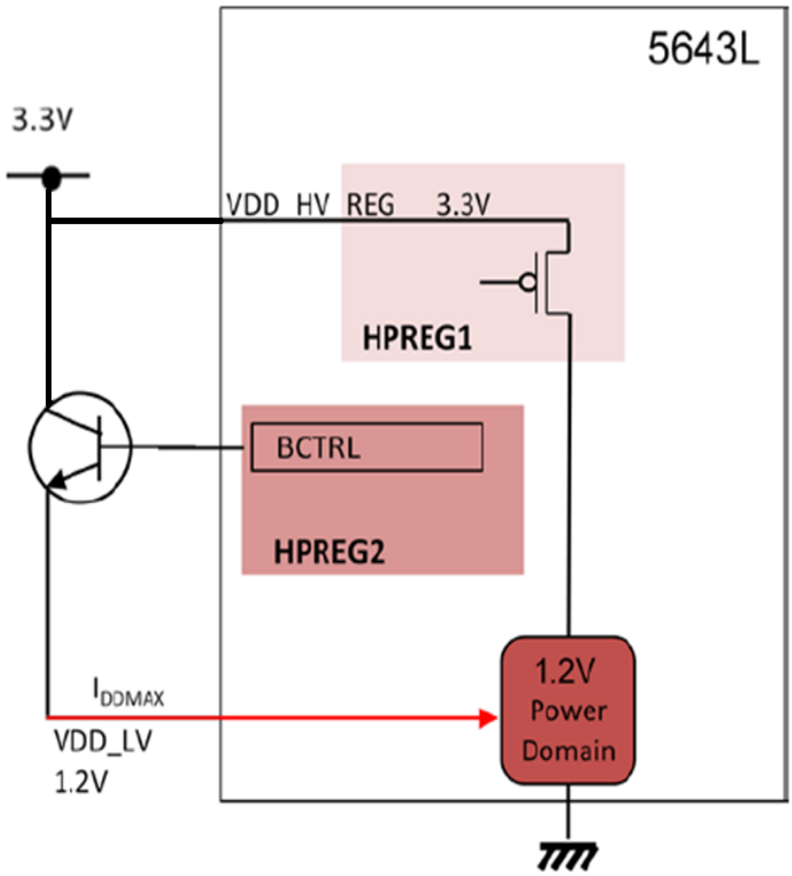


Figure 3. MPC5643L using external ballast transistor

NOTE

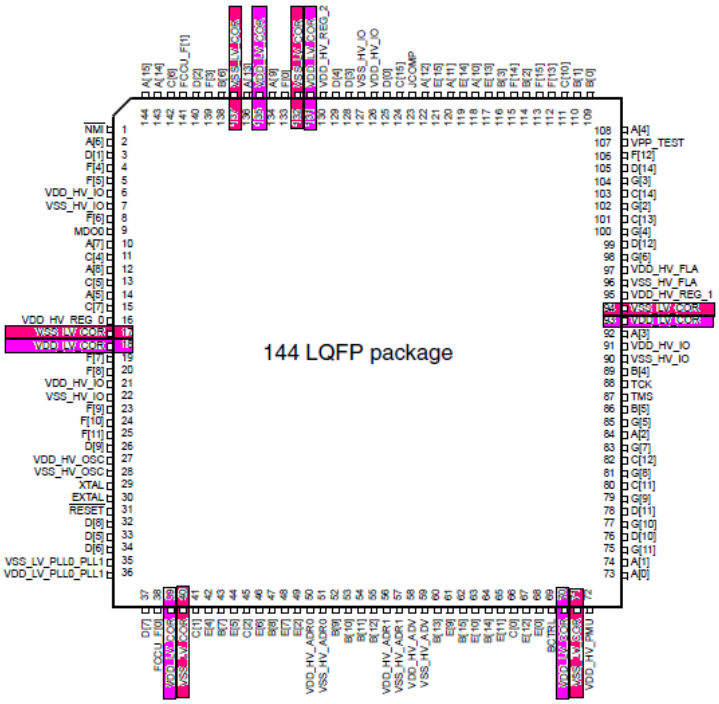
VDD_HV_REG_x signals must be connected to a 3.3V power supply to provide power to HPREG1 during the startup phase.

4 Recommendations on external components

4.1 Bypass capacitors

4.1.1 1.2 V core supply domain VDD_LV_COR (144 LQFP) and VDD_LV (257-pin MAPBGA)

On the 144 LQFP package of MPC5643L, 6 pin pairs are connected to the VDD_LV_COR supply. All of these must be taken into account for the connection of external bypass capacitors. On the 257 MAPBGA package, 4 pin pairs in addition to the inner pad are associated with the VDD_LV/VSS_LV supply pins. See the following figure.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_HV\_ADR1}$	$V_{DD\_HV\_ADR1}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]										NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]										D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]										V_{SS_HV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$										V_{SS_HV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]										NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC										NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC										C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$

NC = Not connected (the pin is physically not connected to anything on the device)
Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

If the internal ballast transistor operation is selected, three pins are internally connected to the three internal ballast transistors.

For the selection of the external capacitors, following constraints and recommendations are valid:

- For stability / decoupling purposes, a larger capacitance value of 12 µF to 40 µF must be connected to the VDD_LV_COR/VSS_LV_COR pin pairs. Taking aging and temperature variations into account, a typical capacitance value of around 26 µF is recommended.
- This capacitance can be split between the different pin pairs. Whenever the microcontroller suddenly demands a large amount of current, first of all the internal device capacitance (~30 nF in MPC5643L) will provide this current. The external capacitance is not seen at the beginning due to parasitic bonding inductance. After the transient, external capacitance starts charging the internal capacitors. It is better for the device if external capacitors are distributed equally because it will provide parallel paths to charge the internal capacitors. This ensures that the internal voltage is not dropping much during transient events and it is restored quickly at every point inside the device. Therefore ideally, the capacitance must be split into equal values for each pin pair. On the 144 LQFP package with 6 pin pairs for example, 6x4.7 µF is a possible setup.
- To optimize the layout space, the number of larger capacitor packages can be reduced and a non-symmetrical setup in the combination of different capacitance values is possible. Even only one capacitor in the range of 27 µF would be possible if the other requirements like equivalent series resistance (ESR) can be fulfilled. The three pin pairs, which are connected to the internal bypass capacitors must be selected with priority for the placement of the larger capacitors.
- For the purpose of fast transient response, smaller bypass capacitors are recommended in addition to the stability capacitors. The total value of all smaller capacitors together must be in the range from 300–900 nF.
- The pin pairs, which are not connected to one of the larger stability capacitors must have a small bypass capacitor connected, and the total capacitance to be taken in account must be in the range 300-900 nF. Taking aging and temperature variations into account, a typical total capacitance value of around 470 nF is recommended.
- The total ESR of 1–100 mΩ for all the VDD_LV_COR capacitances combined is related to a frequency of 1 MHz, which is the bandwidth of the internal voltage regulator. Minimum value is linked to the worst case conditions when taking maximum aging and temperature variation into account.
- If capacitors with slightly smaller ESR than the minimum value are selected, choose a larger capacitance value to compensate this.
- It is not recommended to compensate the ESR in the layout by adding trace capacitance, as the involved inductance of those traces have a negative effect on the voltage regulator stability. The shortest possible connection between the pins and the capacitances should be routed.

Three possible setups on the VDD_LV_COR circuitry are described as an example for the 144 LQFP package:

Setup 1: 6x 4.7 µF, 100 nF capacitor in parallel to each 4.7 µF capacitor.

- Total capacitance of larger capacitors = 28.2 µF. This value is not right in the center of the recommended range suggested above, but acceptable (ideal center would be 26 µF)
- Total capacitance of smaller capacitors for transient response = 600 nF . This value is right in the middle of the recommended range, which would provide maximum tolerance in terms of aging and temperature variations.
- ESR per capacitor is typically 5 mΩ. So, the ESR of 6 big capacitors would be 0.83 mΩ. This value is outside the recommended range, but is acceptable, taking the resistance of board traces into account.
- Good response for large currents as capacitance is equally distributed on each pin pair.

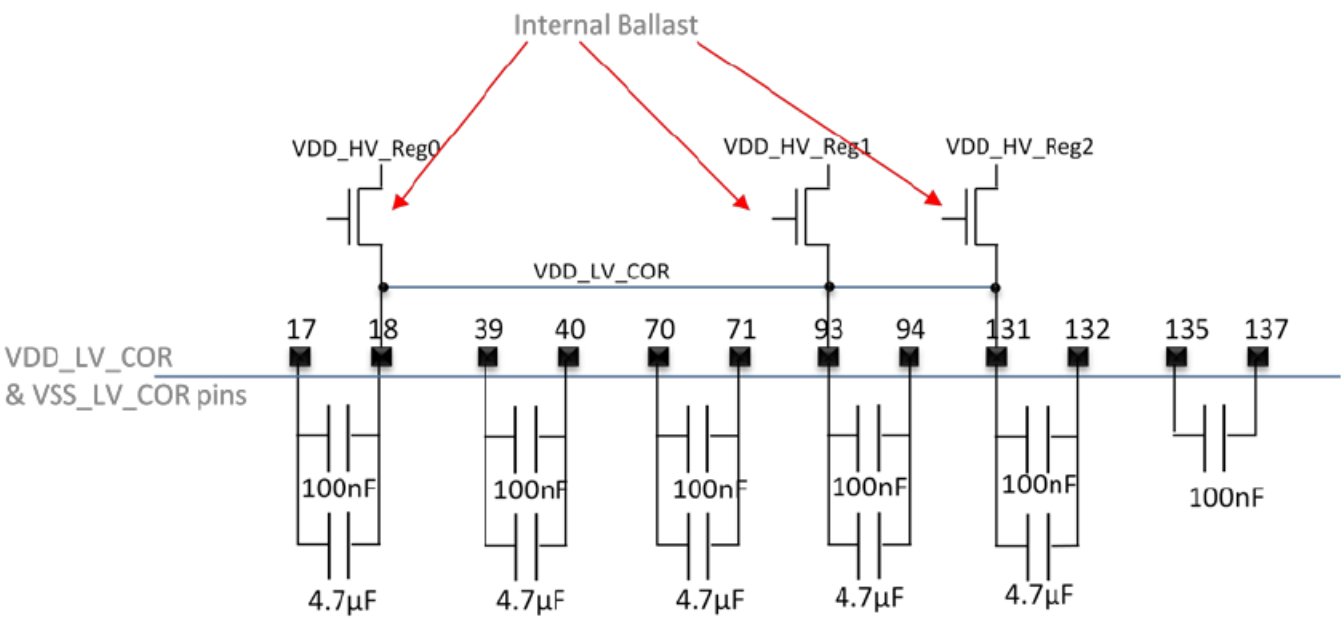
Setup 2: 5x 4.7 µF, 1x100 nF, and 100 nF in parallel to each 4.7 µF capacitor

- Total capacitances of larger capacitors is 23.5 µF. This value is not right in the center of the recommended range, but acceptable.
- ESR of the 5 larger capacitors is in the range of 1 mΩ.
- ESR is more than setup 1; this would also have better effect on parasitic inductance than setup 1.
- Total capacitance of smaller capacitors for transient response = 600 nF. This value is right in the middle of the recommended range, which provides maximum tolerance in terms of aging and temperature variations.

Setup 3: 2x 10 µF capacitors, each with with ESR = 2 mΩ, 1x 4.7 µF capacitor and 3x 220 nF and 100 nF in parallel to the larger capacitors. The larger capacitors are connected to the pins with the internal ballast.

- Total capacitance of larger capacitors = 24.7 µF
- Total ESR of larger capacitors is 0.83 mΩ. This value is outside the 1 mΩ rule, but taking the resistance of board traces into account, it is acceptable.
- ESR is less than that of setup 2 , which means this example would be worse in terms of effect from parasitic inductance than setup 2.

One recommended example setup for 144 LQFP package when using internal bypass capacitors (setup 2) is shown in the following figure.

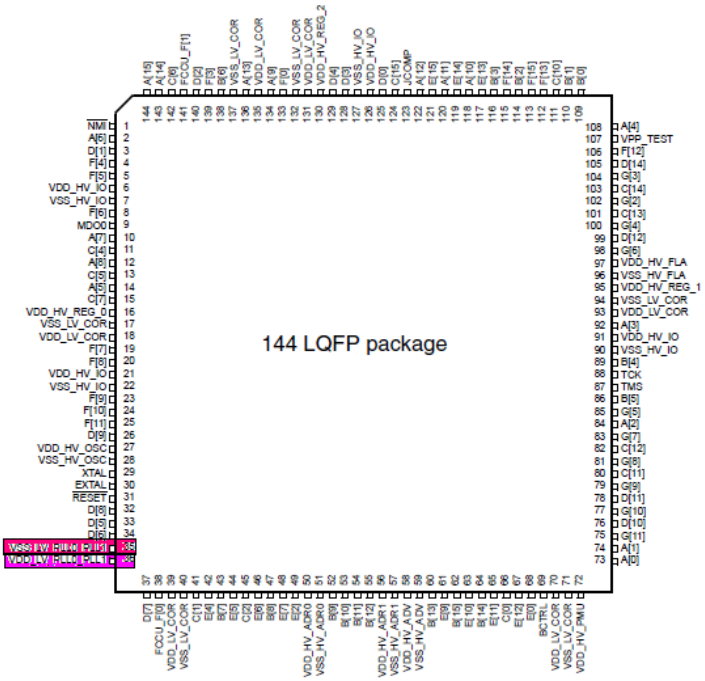


Alternative to above setup, an additional parallel 4.7 µF capacitor on the pin pair at pin 135/137 can be placed to optimize large current demand response (setup 1).

If an external ballast transistor operation is selected, almost all the above recommendations apply as well for the VDD_LV_COR supply pins. The capacitors must be placed as close as possible to the device pins. This mode is more sensitive to the minimum ESR requirement of 1 mΩ.

4.1.2 1.2 V PLL supply domain VDD_LV_PLL

One 1.2 V based supply pin pair for the integrated system PLL is located on the 144 LQFP (pins 35/36) and 257 MAPBGA package (pins N4/P4). See the following figure.



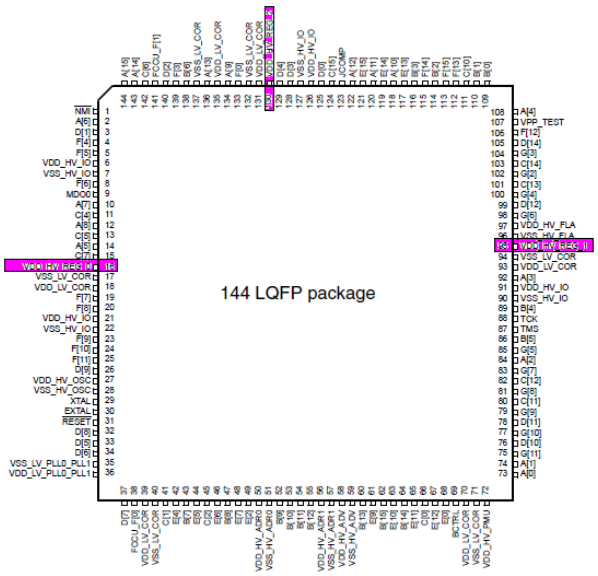
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_HV\_BIR}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_HV\_BIR}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

For this pin pair, a small bypass capacitor for noise filtering in the range of 22–100 nF is recommended to be placed as close as possible.

4.1.3 3.3 V internal regulator ballast transistor supply domain VDD_HV_REG_x:

Three high-voltage signals are internally supplying the three internal ballast transistors of the Regulator HPREG1. On 144 LQFP package, 3 pins are connected to those three signals: VDD_HV_REG_0, VDD_HV_REG_1, VDD_HV_REG_2 (pins 16, 95, 130). On the 257 MAPBGA package, 6 pins are connected to those signals. (pins J3/J4, H15/J15 , C7/C8). See the following figure.

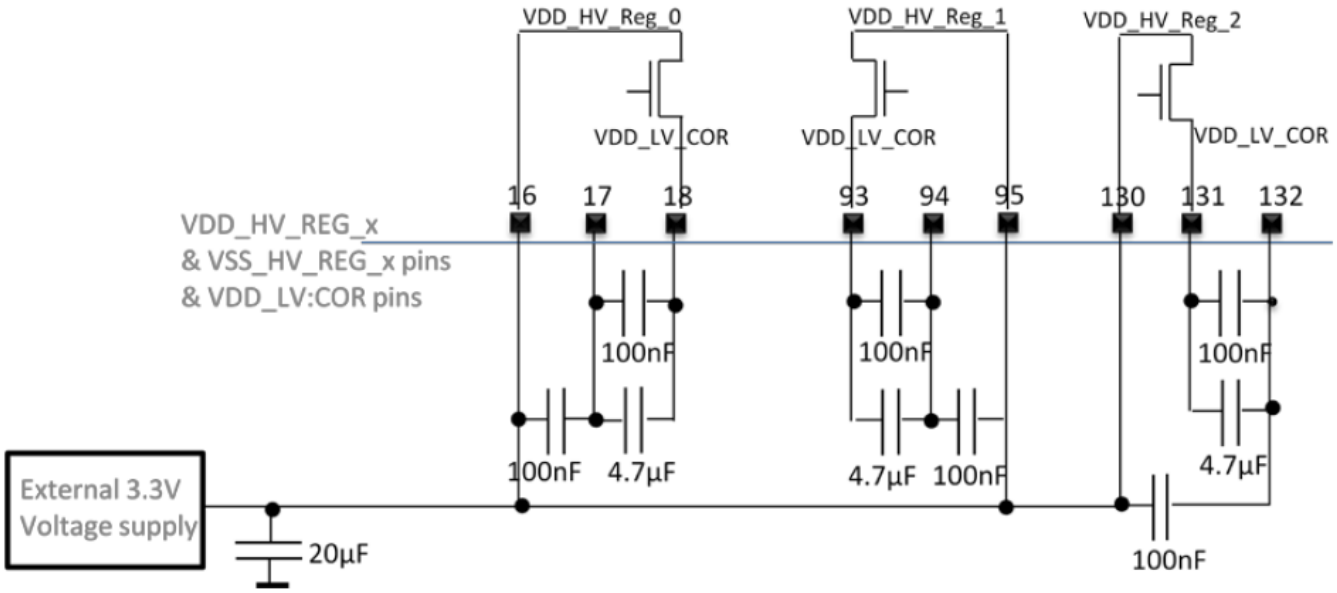


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	V_{RC_HV} (REG)	V_{RC_HV} (REG)	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	V_{RC_HV} (REG)	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	V_{RC_HV} (REG)	V_{RC_HV} (REG)		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	V_{RC_HV} (REG)	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	$\overline{RESET}$	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

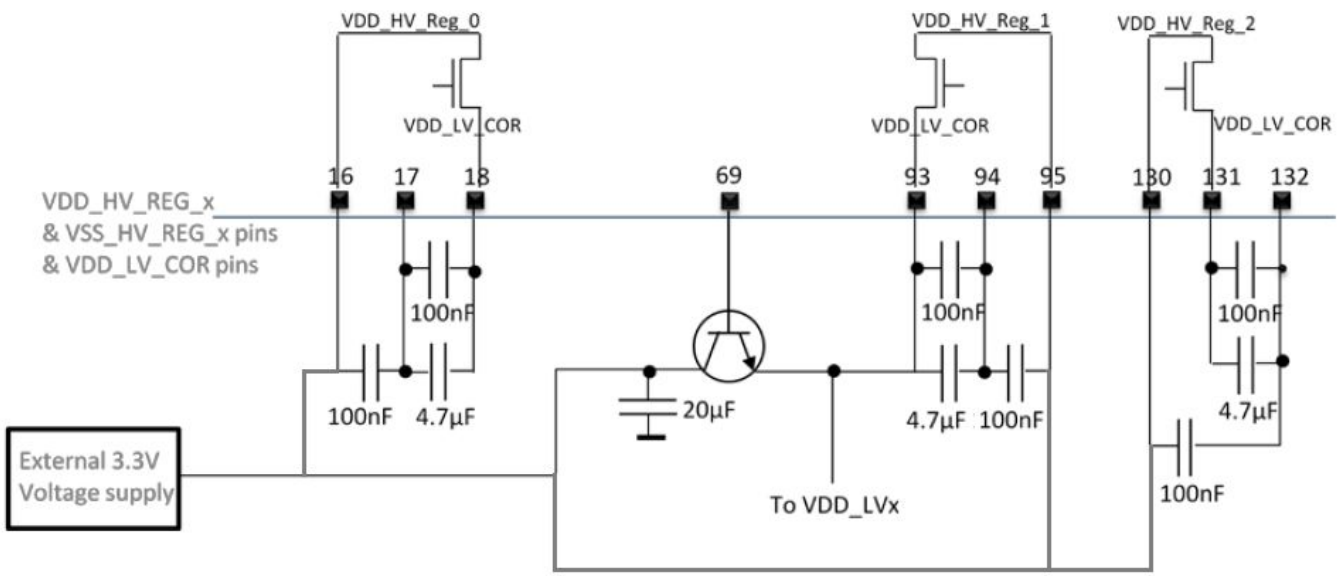
If the internal ballast transistor operation is selected, following recommendations apply:

- One stability capacitor in the value range of 20 µF must be placed directly at the 3.3 V voltage regulator output, taking into account aging and temperature variations.
- This capacitor is not deciding any stability parameter. Therefore, no minimum ESR is required for it. In terms of maximum limit of ESR, it is mandatory not to place a very high ESR capacitor (Tantalum) on these pins. High ESR will isolate these capacitors from their respective traces. This could lead to a voltage drop on these lines whenever current is demanded from these supplies. Therefore, it is recommended to use the same maximum ESR guideline for VDD_HV_REG and VDD_HV_PMU as for VDD_LV_x supply pins (100 mΩ).
- One smaller bypass capacitor in the range of 22–100 nF for fast transient response must be placed on each supply pair. See the following figure.



If an external bypass capacitor is used, following recommendations apply.

- The stability capacitor in the range of 20 µF must be placed as close as possible at the collector of the externally connected bypass transistor.
- This capacitor is not deciding any stability parameter. Therefore, no minimum ESR is required for this capacitor. In terms of maximum limit of ESR, it is mandatory not to place a very high ESR capacitor (Tantalum) on these pins. High ESR will isolate these capacitors from their respective traces. This could lead to a voltage drop on these lines whenever current is demanded from these supplies. Therefore, it is recommended to use the same maximum ESR guideline for VDD_HV_REG and VDD_HV_PMU as for VDD_LV_x supply pins (100 mΩ).
- One smaller bypass capacitor on each supply pair must be placed in the range of 22–100 nF. See the following figure.

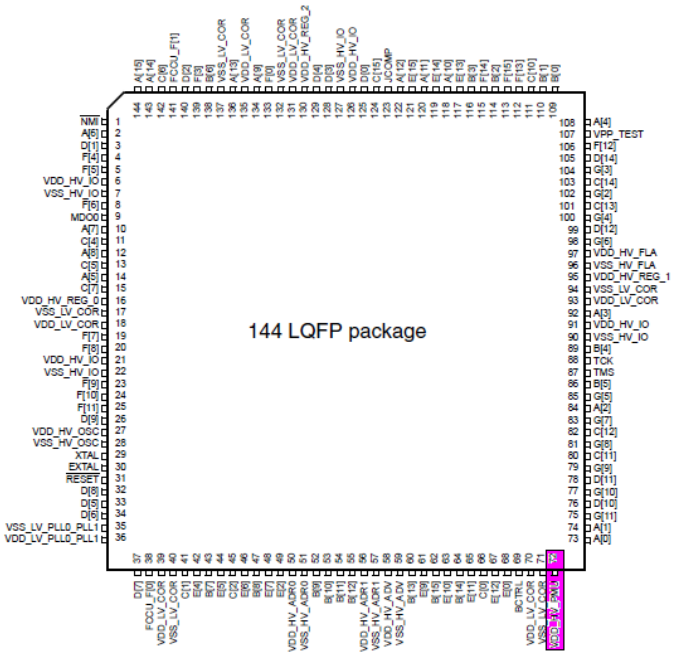


NOTE

VDD_HV_REG_x signals must be connected to a 3.3V power supply to provide power to HPREG1 during the startup phase.

4.1.4 3.3 V voltage regulator supply domain VDD_HV_PMU

The control block of the internal voltage regulator of the device is connected to the supply pin 72 for 144 LQFP and pin U14 for 257 MAPBGA package. See the following figure.



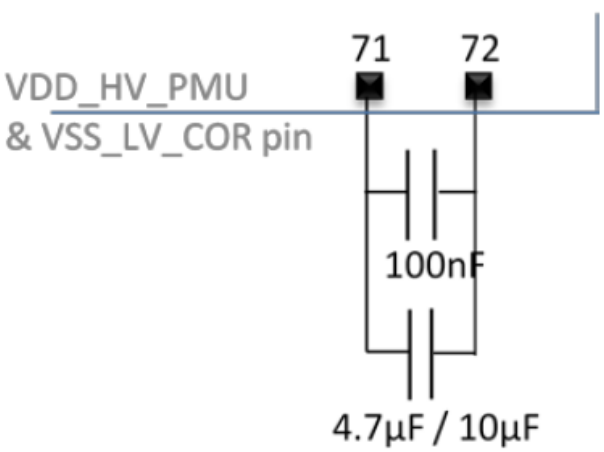
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_LV\_RAM}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

In addition to the mentioned larger capacitor on the 3.3 V supply VDD_HV_REG, one large capacitor on the 3.3 V supply pin VDD_HV_PMU, has to be placed. These capacitors will make sure that there is no large transient drop on 3.3 V supply, when the 1.2 V supply demands current. A minimum capacitance of 4.7/10 µF, is the recommended capacitance size on this pin.

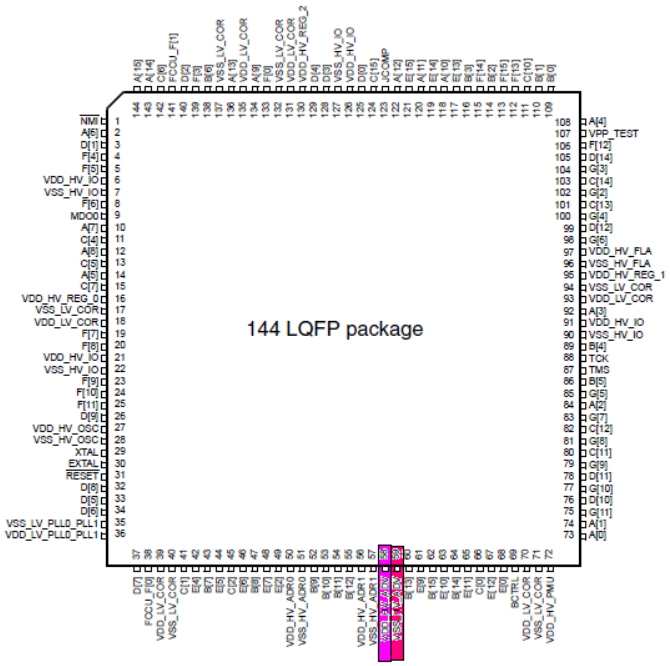
A parallel smaller bypass capacitor for fast transient response is recommended to be placed there, as well.

This capacitor is not deciding any stability parameter. Therefore, no minimum ESR is required for it. In terms of maximum limit of ESR, it is mandatory not to place a very high ESR capacitor (Tantalum) on these pins. High ESR will isolate these capacitors from their respective traces. This could lead to a voltage drop on these lines whenever current is demanded from these supplies. Therefore, it is recommended to use the same maximum ESR guideline for VDD_HV_REG and VDD_HV_PMU as for VDD_LV_x supply pins (100 mΩ). See the following figure.



4.1.5 3.3 V ADC converter supply domain VDD_HV_ADV

One ADC supply pin pair is located on the 144 LQFP (pins 58/59) and 257 MAPBGA package (pins U9/U10). See the following figure.



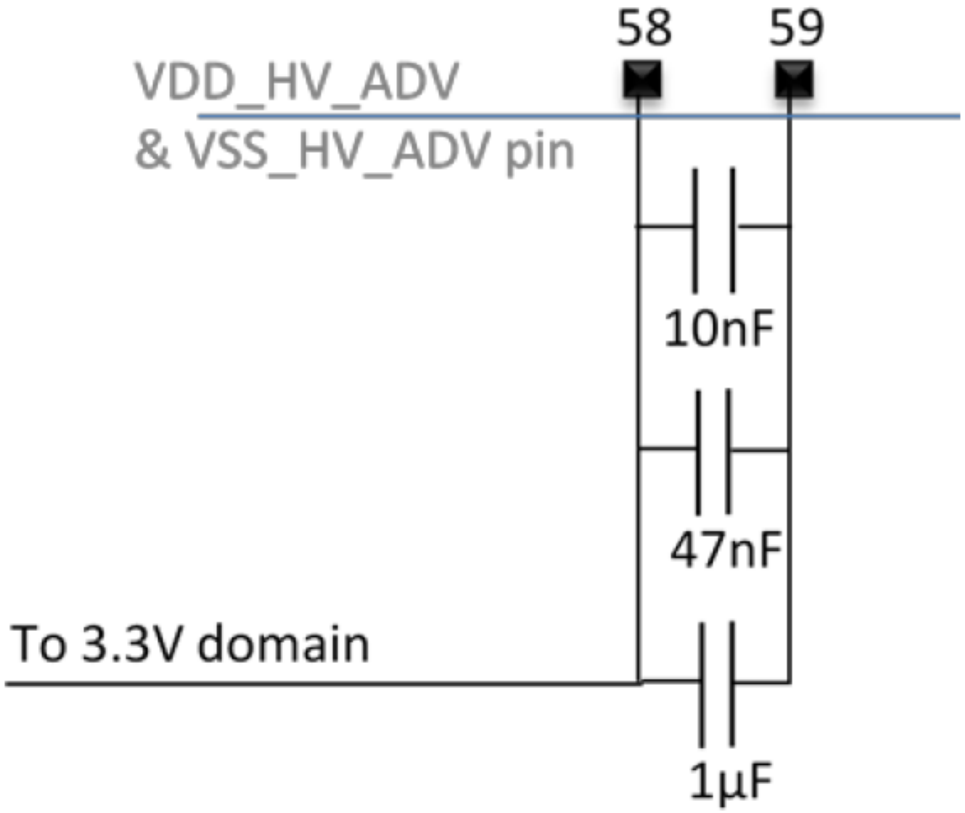
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

The ADC requires careful decoupling of the dedicated supply and reference pins to reduce ADC performance degradation through noise lines induced by the device itself and other component present on the application board.

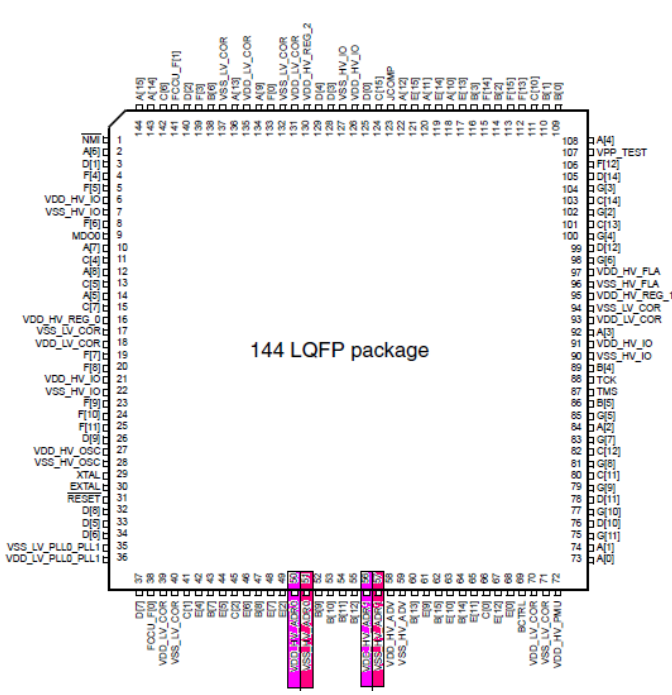
The recommended capacitors on the VDD_HV_ADV/VSS_HV_ADV pin pair are:

- 1 µF (electrolytic or tantalum);
- 47 nF ceramic; low inductance package and mounted as close as possible to the chip.
- It is suggested to add a third 10 nF low inductance package ceramic capacitor to better reject high frequency coupling, closer to the chip than the 47 nF one. See the following figure.



4.1.6 3.3 V ADC reference voltage VDD_HV_ADR0/1:

There are two reference voltage pin pairs on the 144 LQFP (pins 50/51 and pins 56/57) package and 257 MAPBGA package (pins R7/T7 and pins R9/T9).



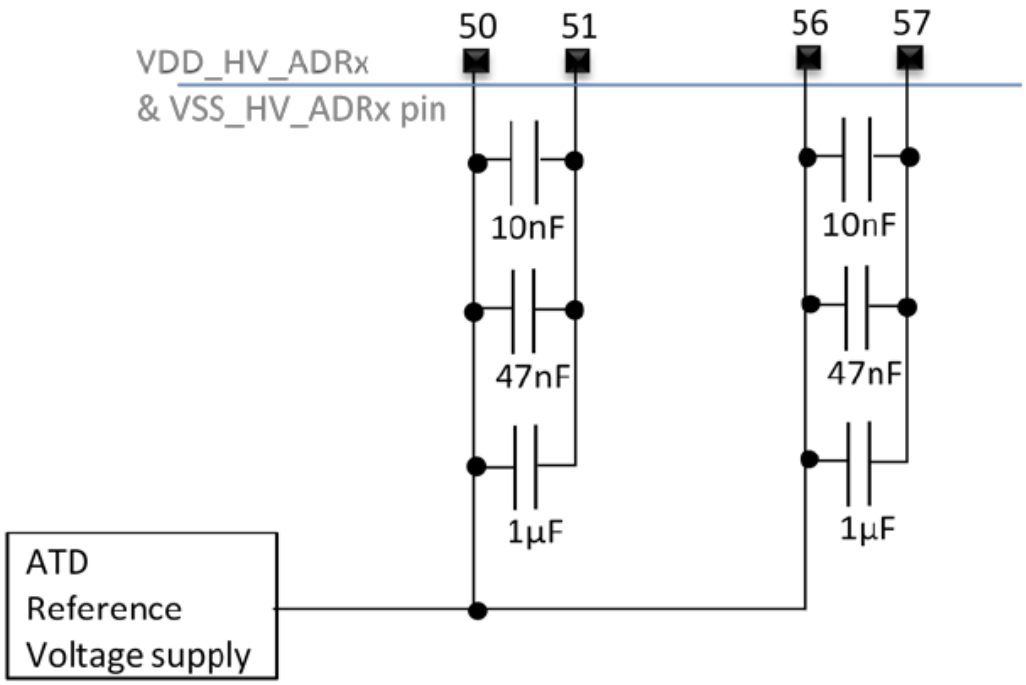
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]										NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]										D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]										V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$										V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]										NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC										NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC										C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_LV\_ADR0}$	B[11]	$V_{SS\_LV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

For the ADC reference pins, same recommendations apply as for the ADC supply pins (See 3.3 V ADC converter supply domain VDD_HV_ADV).

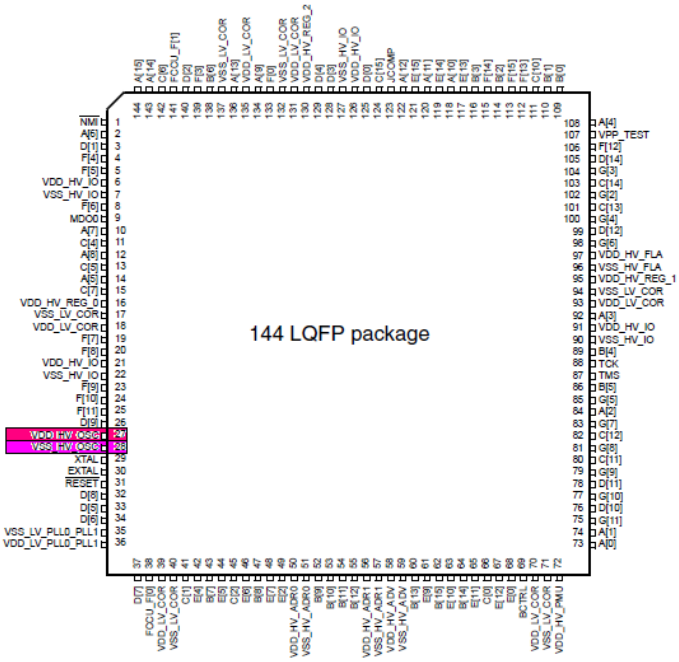
The recommended capacitors on the VDD_HV_ADRx/VSS_HV_ADRx pin pair are:

- 1 µF (electrolytic or tantalum);
- 47 nF ceramic; low inductance package and mounted as close as possible to the chip.
- It is suggested to add a third 10 nF low inductance package ceramic capacitor to better reject high frequency coupling, closer to the chip than the 47 nF one. See the figure below.



4.1.7 3.3 V oscillator supply domain VDD_HV_OSC

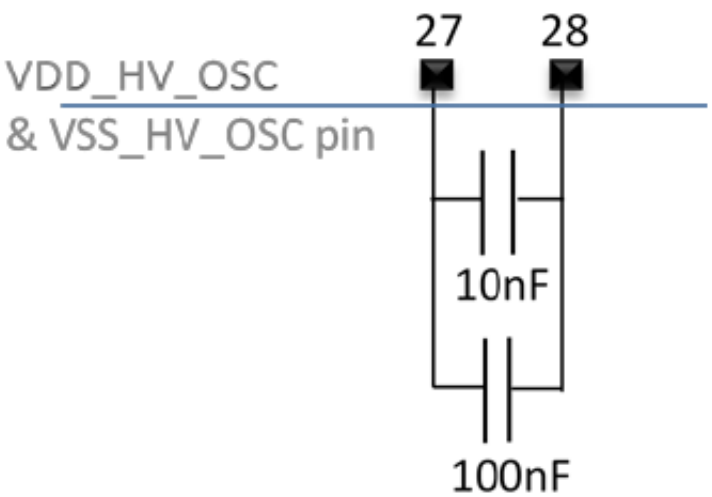
There is one 3.3 V pin pair on the 144 LQFP (pins 27/28) package and 257 MAPBGA package (pins M1/P1) for the crystal oscillator amplifier supply. See the following figure.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	V_{DD_LV} (OSC)	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	V_{SS_HV} (OSC)	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

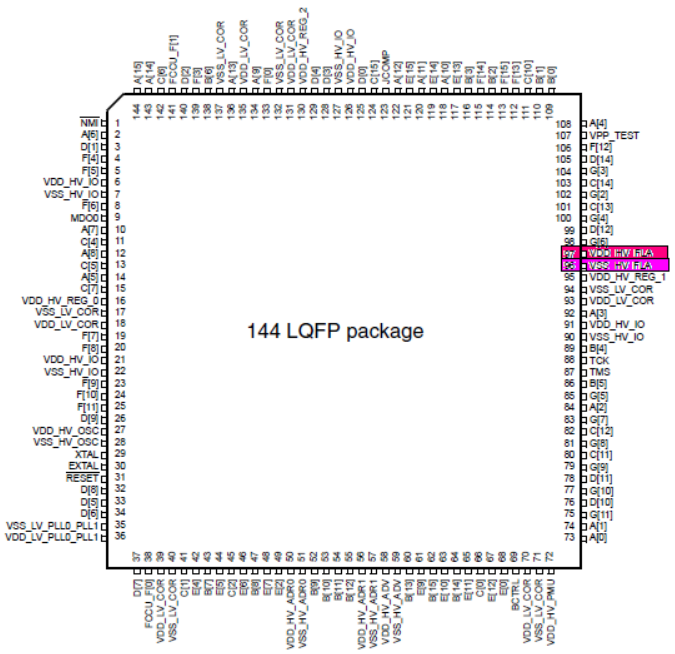
1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

On the oscillator supply pins VDD_HV_OSC and VSS_HV_OSC, two small bypass capacitors for fast transient filtering are recommended; a 100 nF and a parallel connected 10 nF capacitor, as shown in the figure given below.



4.1.8 3.3 V flash supply domain VDD_HV_FLA

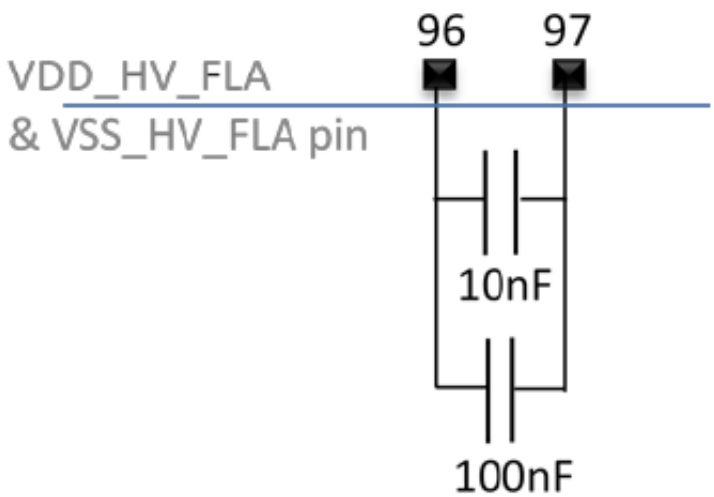
There is one 3.3 V pin pair on the 144 LQFP (pins 96/97) package and 257 MAPBGA package (pins J16/H16) for the oscillator supply. See the figure below.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC[1]	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_LV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_LV\_FLA}$	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$

1 NC = Not connected (the pin is physically not connected to anything on the device)
2 Pin K3 is NC on cut1 and $\overline{RDY}$ on cut2/3.

On the flash supply pins VDD_HV_FLA and VSS_HV_FLA, two small bypass capacitors for fast transient filtering are recommended; a 100 nF and a parallel connected 10 nF capacitor, as shown in the following figure.



4.2 External ballast transistor

The recommended external ballast transistor is the bipolar transistor BCP68, with a gain range of 85 to 375 (for IC = 500 mA, VCE = 1 V), provided by several suppliers, such as On Semiconductor®, Infineon®, and NXP®. This recommendation includes gain variations BCP68-10, BCP68-16, and BCP68-25.

In addition to the BCP68 transistor, the 2SCR573D A08 bipolar transistor from Rohm Semiconductor® is also recommended. Refer to Engineering Bulletin EB787, *MPC5643L Additional Supported Bipolar Transistor*, for more details.

The most important parameters for the interoperability with the integrated voltage regulator are the DC current gain (hFE) and the temperature coefficient of the gain (XTB). While the specified gain range of most BCP68 vendors is the same, there are slight variations in the temperature coefficient parameter.

MPC5643L voltage regulator operation was simulated against the typical variation on temperature coefficient and against the specified gain range to have a robust design.

As mentioned in 3.3 V internal regulator ballast transistor supply domain VDD_HV_REG_x:, for the stable operation of the voltage regulator in the external bypass mode, it is important that the stabilization cap of about 20 µF is placed as close as possible at the collector of this bipolar transistor. See Figure 3.

5 /RESET pin and power-up

The /RESET pin is an open-drain bidirectional signal (input and output).

The /RESET pin may be externally asserted low in order to reset the device. The /RESET pin must be externally asserted low at least 500 ns so that the device can recognize RESET assertion. When a reset occurs (internally or externally), the device drives the /RESET pin low until the reset sequence finishes.

Do not externally drive the /RESET pin high. A push-pull output driver is not allowed to switch the /RESET pin. The /RESET pin has an internal weak pulldown, unlike /RESET pin on other Freescale products that might have an internal weak pullup. See Figure 4.

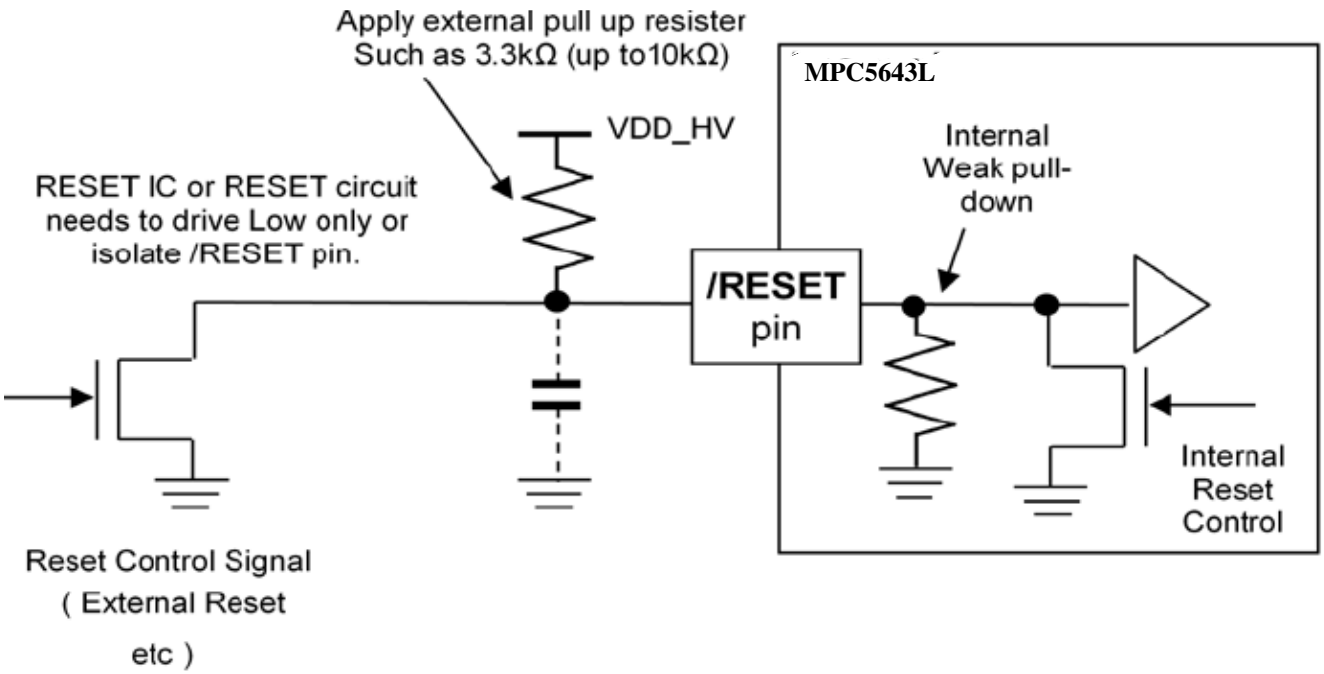


Figure 4. MPC5643L /RESET pin configuration

The /RESET pin must be externally asserted low during power up until VDD_HV_xxx supply voltage exceeds the minimum operating limit. If external reset circuit does not assert the /RESET pin, after the device reset sequence finishes, the device releases the /RESET pin.

After the device powers up, the PMU performs the following functions:

- Automatically detects whether an external ballast is present
- Applies the factory-specified trimming to the output
- Performs the built-in self-test (BIST)

See the Power Management Unit (PMU) chapter of the MPC5643L Data Sheet and MPC5643LRM, available on **freescale.com**, for further details on power-up and initialization.

6 External oscillator (XOSC)

The device provides an oscillator/resonator driver. See Figure 5 which describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

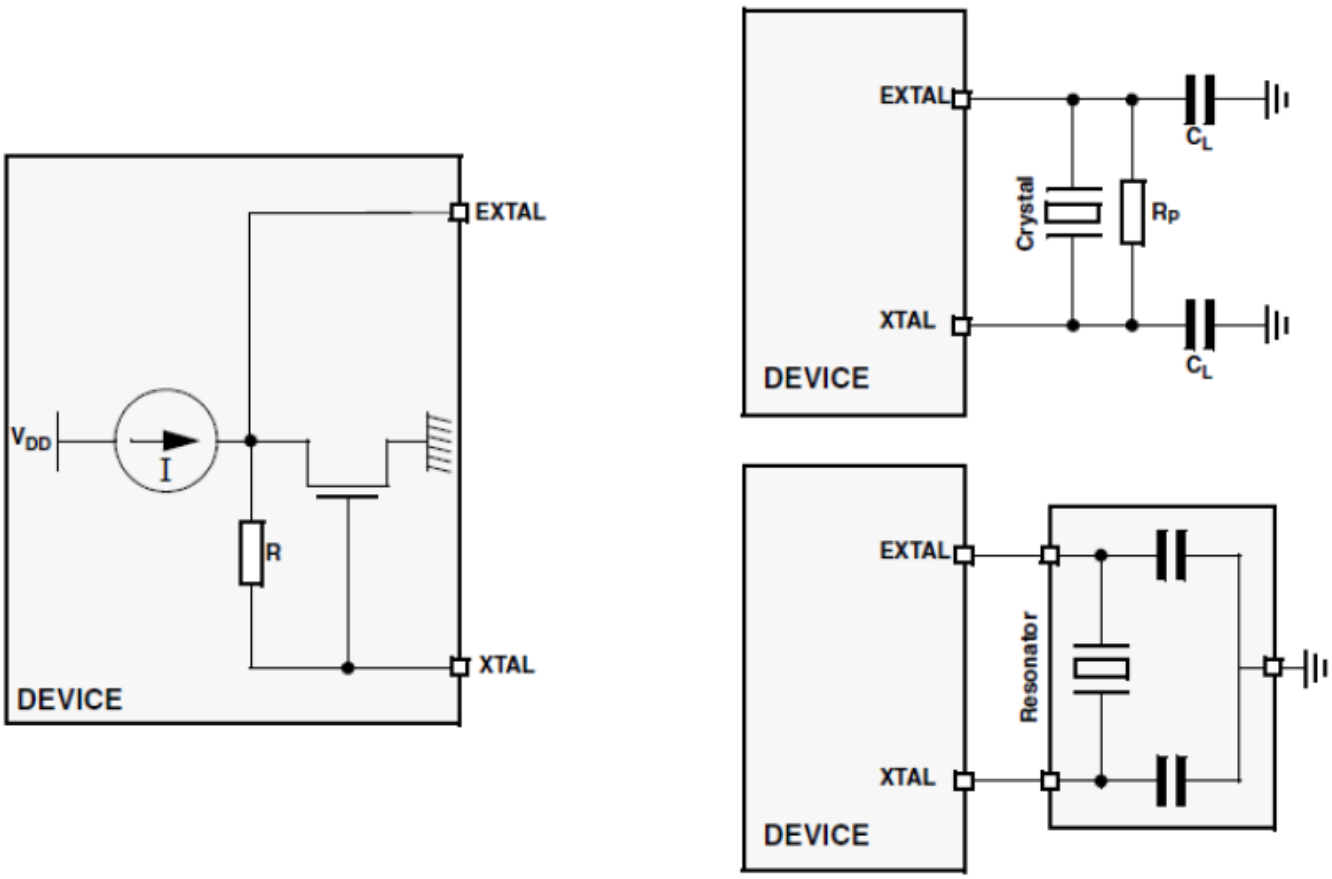


Figure 5. Crystal oscillator and resonator connection scheme

External feedback resistor Rp is not needed with MPC5643L. Matching and evaluation by the crystal/resonator vendor is needed to determine the value of C_L (see Figure 5). See the main oscillator electrical characteristics section of MPC5643L Data Sheet, available on **freescale.com** for further details regarding XOSC.

7 Unused system pin termination

Information regarding unused systems pin termination:

- /NMI is always internally pulled up, so it can be left open if not used.
- TMS/TCK high and JCOMP low makes JTAG TAP controller stay in the reset state.

  These JTAG pins have internal weak pulls to stay TAP controller reset if not used.
- FCCU_F[0,1] are not multiplexed with GPIO. They are dedicated system pins.

See the System pins section of MPC5643L RM, available on **freescale.com** for further details regarding system pins.

8 References

The following reference documents are available on **freescale.com**.

- MPC5643LRM, *Qorivva MPC5643L Microcontroller Reference Manual*
- MPC5643L, *Qorivva MPC5643L Microcontroller Data Sheet*

9 Revision history

Revision number	Date	Description of changes
0	11/2012	Initial version.
1	10/2013	• Voltage regulator using external ballast transistor : Added note that VDD_HV_REG_x signals must be connected to a 3.3V power supply; revised Figure 3 to show the 3.3V power supply connection. • 3.3 V internal regulator ballast transistor supply domain VDD_HV_REG_x: Revised third figure to show additional 3.3V power supply connections. • External ballast transistor : Added information about the recommended 2SCR573D A08 bipolar transistor from Rohm Semiconductor; added reference to EB787. • Editorial changes and improvements throughout.

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