Freescale Semiconductor
Application Note

Document Number: AN4499
Rev. 0, 04/2012

MC68302 to MPC8306/S Migration Guide

by Freescale Semiconductor, Inc.

Contents

1 Objective

The objective of this document is to serve as a guide for migrating MC68302 based designs to MPC8306/S PowerQUICC II based designs, which are based on the e300 Power™ core. It describes the differences between the MC68302 and MPC8306/S chips, and recommends appropriate literature for further details.

2 References

MPC8306 PowerQUICC II Pro Integrated Host Processor Reference Manual

MPC8306 PowerQUICC II Pro Integrated Host Processor Reference Manual Addendum

MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications

MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications

3 H/W Block Listing

Table 1 gives a comparison of Hardware-blocks in both the SoCs.

Table 1. List of IPs

IP	MC68302	MPC8306/ MPC8306S	Benefit to customer w/ MPC8306/S
Core	68K Core Max frequency 33 MHz	e300c3 Max frequency 266 MHz	Offers upto 512 DMIPS enabling more complex software
Cache	Nil	I-Cache - 16KB D-Cache - 16KB	Better performance
DDR Controller	None	16-bit DDR2 SDRAM	Replaces costly SRAMs with cheaper and more accessible DDR2 memory
Communications Complex	Communications Processor Module – RISC controller 3 Serial Communication Controllers 2 Serial Management Controllers (SMCs)	QUICC Engine – RISC Controller with 48KB IRAM and 16KB MURAM; No ROM Independent Serial DMA channels 5 Unified Communication Controllers	Supports a richer set of protocols and interfaces, and micro code programmability preserves hardware investment
UART	Up to 3 as part of SCC	2 Independent DUART Either 4 x two-wired Or 2 x four-wired 5 UCCs can also be configured as UART	Greater number of ports available for user, increased design flexibility and options
HDLC	Up to 3 as part of SCC	2 UCCs can be configured as HDLC	
TDM	Nil	2	Greater number of ports available for user
I2C	Nil	2	Supports many popular peripherals, including ZigBee, HomePlug Green PHY, etc.
SPI	1	1	Supports low-rate data communications, such as ZigBee, HomePlug Green PHY, etc.
GPIO	Up to 28	Up to 56	More number of ports available for user
JTAG	—	Present	Simpler debug interface
Interrupt controller	Present	Present	Advanced features for priority programming
USB	None	1x USB 2.0 OTG	Can interface to many popular peripherals, including Wi-Fi, NAS, etc.
External Bus Interface	23 bits of address and 16 bits of data bus. No NAND flash support	26-bit multiplexed address bus and 16-bit data bus with support for NAND FLASH	Larger address space, Boot from NAND supported

Table 1. List of IPs (continued)

IP	MC68302	MPC8306/ MPC8306S	Benefit to customer w/ MPC8306/S
Chip Selects	4	4 dedicated and 4 multiplexed with other signals	Greater number of chip selects available to user, increased design flexibility
DMAC	SDMA supported	Two DMA Engines – 1 x Sixteen channel and 1 x Four channel	Higher performance
Timers	2 timers + WDT	4 x 16-bit or 2 x 32-bit or 1 x 64-bit WDT PIT	Greater number of ports available for user
RTC	None	Present	
Ethernet	Nil	Up to 3 x 10/100Mbps MII/RMII (over UCC) IEEE1588 protocol supported	Well suited for transition to IP networks, as well as Industrial Automation, Smart Energy applications
eSDHC	None	Compatible with SDHC/MMC Std Ver 2.0 Clock frequency of 33.25 MHz with transfers @ up to 133 Mbps Block sizes up to 4KB 1-bit/4-bit SD and SDIO modes	Can be used to interface with SD/MMC/SDIO cards
FlexCAN	None	4 ports	Popular protocol for industrial applications
Package	PGA 132 13*13 PQFP 132 TQFP 132	MAPBGA 369 19*19*1.61 P0.8	BGAs have higher assembly yields, are less fragile and easier to handle that QFP/PGA devices
Power	467.5 – 715mW at 5.5V for 25 MHz operation	451 – 925mW for 266/200/133 MHz (Core/QE/CSB) operation	Greatly improved Power/Performance ratio
Ambient Operating Temperature	-40C to 105C version and 0C to 105C version	0C to 70C and -40C to 85C	Suited for full industrial temperature range
Collateral	—	Development system available with Linux and MQX support	Enables rapid development, lowers risk and speeds time to market
Status	Nearing EOL	Active Member of Freescale Longevity Program with assured lifetime of 10 years	Future proof solution

4 Migration Considerations

4.1 Core

Table 2 provides a list of differences between 68000 and e300C3 cores

Table 2. Differences Between Cores

Feature	68000 core	e300c3 (MPC8306/S)
PVR value	Not applicable	0x8085_00xx
FPU support	Not supported	Yes
MSR[FP]	Not supported	Supported
MSR[FE0], MSR[FE1]	Not supported	Supported
Performance Monitor support	No	Yes
Perf. Mon. exception	Not supported	Supported Offset 0xF00, belongs to async exception category w/ priority = 6 (lower than External Internal but higher than Decrementer Interrupt)
MSR[PMM]	Not supported	Supported To mark a process that will enable the statistics collection
PMC0-3, UPMC0-3 Perf. Mon. Counter regs.	Not supported	Supported PMC0-3 are 32bit counters and UPMC0-3 (RO) are used by User level to read the counter values
PMGC0, UPMGC0 Perf. Mon. Global Control reg.	Not Supported	Supported PMGC0 provides global control for all the PM counters and UPMGC0 (RO) is used by User level to read the reg. value
PMLCa0-3, UPMLCa0-3 Perf. Mon. Local Control regs	Not Supported	Supported PMLCa0-3 provide local control to their corresponding PM counter and UPMLCa0-3 (RO) are used by User level to read the reg. value
mtpmr, mfpmr new instructions to move the data between PM cfg regs. and GPRs	Not Supported	Supported Functionally, mtpmr and mfpmr are similar to mtspr and mfspr, but they work with PM cfg regs only, while the latter work with SPR regs.

In summary, e300c3 core is a significantly advanced core compared to the 68000 core offering ~2 DMIPS/MHz performance. These significant advances may require software changes to the existing code base of MC68302. To ease the migration, Freescale offers freely downloadable Linux BSP and Netcomm driver software. With these packages as the base, customers can migrate their legacy code to MPC8306/S with low effort.

4.2 DRAM Controller

MPC8306/S integrates a DDR2 SDRAM controller that supports a 16-bit interface @ 233 MHz, giving significant performance improvement over MC68302, which does not have a DDR SDRAM controller. This also ensures lower system cost and higher longevity.

4.3 QUICC Engine

4.3.1 Differences in architecture

For the MC68302, the u-code is stored in the internal ROM. MPC8306/S does not have an internal ROM for storing the QUICC Engine RISC u-code. The u-code must be loaded into I-RAM from a non-volatile memory like EPROM/FLASH on-board by software, before using any QE functionality or interface. Table 3 summarizes the hardware architecture differences between the Communication Processor Module and QUICC Engine on MC68302 and MPC8306/S respectively.

Table 3. QE/CPM H/W Differences

Hardware	MC68302 CPM	MPC8306/S QE
Internal ROM	Available	Not Available
I-RAM Size	1152 bytes	48KB
MURAM Size	Not available	16KB
Number of UCCs	None	5
Number of SCCs	2	None
Number of SMC	1	None
Number of RISC	1	1
Number of SI	None	1
Max Frequency	16 MHz	233 MHz

4.3.2 Protocol support

Table 4 shows the comparison of QE interface/protocols supported by MC68302 and MPC8306/S.

Table 4. Interface/Protocols supported

Interface/Protocol	MC68302	MPC8306/S
MII	No	Supported
RMII	No	Supported
IEEE1588	No	Supported (not on MPC8306S)
TDM	No	x2 Normal/Bus

Table 4. Interface/Protocols supported

Interface/Protocol	MC68302	MPC8306/S
Async HDLC	No	Supported
Eth Management Interface	No	Supported
BISYNC	Supported	No
HDLC Bus	Supported	Supported
Transparent	Supported	Supported

4.4 External bus interface

4.4.1 Address/Data bus

The external bus interface on MC68302 provides non-multiplexed 23-bit address bus and 16-bit data bus. MPC8306/S provides multiplexed 26-bit address bus and 16-bit data bus. For MPC8306/S based devices, an address latch device must be used outside the SOC to de-multiplex address signals [0:15] and data signals [0:15]. The external bus interface of MPC8306/S can operate at 66MHz, a much higher rate compared to the MC68302. This ensures better performance in accessing devices connected to the external bus.

4.4.2 Clocks

MC68302 drives out a single CLKO signal, which directly sets the bus frequency. MPC8306/S drives out two LCLK signals that set the frequency of the external bus interface controller.

4.4.3 Modes of operation

The external bus interface controller on MC68302 is suited for connecting to general purpose peripherals like EEPROMs, NOR Flash and SRAM without any glue logic. Connection to other memory devices like DRAM require glue logic.

The external bus interface controller on MPC8306/S supports General Purpose Controller Machine (GPCM), User Programmable Machine (UPM) and Flash Control Machine (FCM). FCM facilitates a direct interface between NAND flash memory and SoC.

4.5 UART

MPC8306/S provides two DUART (DUART1 and DUART2). Each DUART has two 2-wire interfaces (RxD, TxD). Therefore, there are total four 2-wire interfaces.

Each DUART can also be configured as a single 4-wire interface (RxD, TxD, RTS, CTS). The 2-wire or 4-wire configuration can be done through programming the relevant fields of an SICR register. Refer to the section on signal multiplexing under the Software Changes section of this document.

In addition, the Quicc Engine's UCCs can also be optionally configured to function as UART ports.

In comparison, for MC68302, there are no dedicated UART ports. The only option is to use one or more of the SCC ports in UART mode.

4.6 Power Management

MPC8306/S supports four power states, i.e. Full Power, Doze, Nap and Sleep.

In Full Power mode, the e300 core and SOC operate normally.

In Doze mode, the e300 core stops dispatching new instructions and disables most of its functional units. However, the core time base and clocks continue to operate, with other functional blocks of the SOC.

In Nap mode, the core is stopped along with its clocks, except the time base. Other functional blocks of the SOC operate normally.

In sleep mode, the core along with its clocks and time base are stopped, except the interrupt unit. Other functional blocks of the SOC operate normally.

Refer to the Power Management Control section of the *MPC8306 PowerQUICC II Pro Integrated Host Processor Reference Manual* for further details and programming.

5 Software Changes

5.1 Tool-chain

e300c3 tool-chain should be used to compile the sources.

5.2 IDs

PVR (processor version register), SVR (system version register) and SPRIDR (System Part and Revision ID Register) registers show unique ID of any SoC. For MPC8306/S use following values.

PVR - 0x8085_00xx

SVR - 0x81100210

SPRIDR - 0x81100210

5.3 Reset Configuration Words

The main difference of Reset Configuration Words (RCW) is the core clock and QE PLL setting.

The Reset Configuration Word Low Register (RCWLR) and Reset Configuration Word High Register (RCWHR) for most common MPC8306/S systems are shown in Table 5, Table 6, and Table 7.

SYS_CLK_IN at 33.33 MHz , Core clock @ 266 MHz, DDR clock @ 266 MHz, system bus @ 133 MHz and QE clock @ 200 MHz:

RCWLR - 0x4404_0006

Table 5. Reset Configuration Word Low Register (RCWLR) Example

LBCM	DDRCM	SVCOD	SPMF	—	CVCOD	CIMF	CFMF	—	CEVCOD	CEPDF	CEPMF	RCWLR
0	1	0 0	0 1 0 0	0	0 0	0 0 1 0	1	0 0 0 0 0 0 0 0	1 0	0	0 0 1 1 0	0x4405 0086

Table 6. Individual Clock Frequency Description

Desc	SYS_CLK_IN	SVCO	SVCOD	XLB	LBIU	DDR	CVCO	Core	CEVCO	CEVCOD	CE
Freq(MHz)	33.33	533	266	133	133	266	533	266	400	200	200

Boot memory space (BMS) from 0x0000_0000 to 0x007F_FFFF, Local Bus 16-bit boot ROM:

RCWHR - 0x0060_0000

Table 7. Reset Configuration Word High Register (RCWHR) Example

—	COREDIS	BMS	BOOTSEQ	SWEN	ROMLOC	RLEXT	—	TPR	—	TLE	LALE	—	RCWHR
0 0 0 0	0	0	0 0	0	1 1 0	0 0	0 0 0 0 0 0 0 0 0 0	0	0 0 0 0	0	0	0 0	0x00 6000 00

For more details, refer to the section on Reset, Clocking and Initialization in the *MPC8306 PowerQUICC II Pro Integrated Host Processor Reference Manual*, and the section on Clocking in the *MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications* and *MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

5.4 IPIC vector locations

Coding of "IVEC" field has been changed. This field shows the highest priority regular interrupt source pending to core. Table 8 lists the IPIC vector locations for MPC8306/S.

Table 8. IPIC Vector Locations

Interrupt ID Number	Interrupt Meaning
0	Error (No Int)
1-3	Reserved
4-8	Reserved
9	UARTx

Table 8. IPIC Vector Locations

Interrupt ID Number	Interrupt Meaning
10	FlexCANx (Not applicable for MPC8306S)
11-13	Reserved
14	I2C1
15	I2C2
16	SPI
17	IRQ1
18	IRQ2
19	IRQ3
20-31	Reserved
32	QE High
33	QE Low
34-37	Reserved
38	USB DR
39-41	Reserved
42	eSDHC (Not applicable for MPC8306S)
43-47	Reserved
48	IRQ0
49-63	Reserved
64	RTC SEC
65	PIT
66-67	Reserved
68	RTC ALR
69	Reserved
70	SBA
71	DMA Engine 2
72	GTM4
73	Reserved
74	QE Ports
75	GPIOx
76	DDRC

Table 8. IPIC Vector Locations

Interrupt ID Number	Interrupt Meaning
77	eLBC
78	GTM2
79	Reserved
80	PMC
81-83	Reserved
84	GTM3
85-89	Reserved
90	GTM1
91-93	Reserved
94	DMA Engine 1
95-127	Reserved

5.5 IMMR memory map

Table 9 defines the memory map of various IP within MPC8306/S.

Table 9. Memory Map

Block Base Address	Block	Actual Size	Window
0x0_0000–0x0_01FF	System configuration	512 bytes	512 bytes
0x0_0200–0x0_02FF	Watchdog timer	16 bytes	256 bytes
0x0_0300–0x0_03FF	Real time clock	32 bytes	256 bytes
0x0_0400–0x0_04FF	Periodic interval timer	32 bytes	256 bytes
0x0_0500–0x0_05FF	Global timers module 1	64 bytes	256 bytes
0x0_0600–0x0_06FF	Reserved	64 bytes	256 bytes
0x0_0700–0x0_07FF	Integrated programmable interrupt controller (IPIC)	128 bytes	256 bytes
0x0_0800–0x0_08FF	System arbiter	30 bytes	256 bytes
0x0_0900–0x0_09FF	Reset module	44 bytes	256 bytes
0x0_0A00–0x0_0AFF	Clock module	44 bytes	256 bytes
0x0_0B00–0x0_0BFF	Power management control module	20 bytes	256 bytes
0x0_0C00–0x0_0CFF	GPIO 1	24 bytes	256 bytes
0x0_0D00–0x0_0DFF	GPIO 2	24 bytes	256 bytes
0x0_0E00–0x0_12FF	Reserved		1.25 Kbytes

Table 9. Memory Map (continued)

Block Base Address	Block	Actual Size	Window
0x0_1300–0x0_13FF	QUICC Engine port interrupts		256 bytes
0x0_1400–0x0_17FF	Reserved		1 Kbyte
0x0_1800–0x0_1FFF	Reserved		2 Kbytes
0x0_2000–0x0_2FFF	DDR memory controller		4 Kbytes
0x0_3000–0x0_30FF	I2C controller 1		256 bytes
0x0_3100–0x0_31FF	I2C controller 2		256 bytes
0x0_3200–0x0_44FF	Reserved		4.75 Kbytes
0x0_4500–0x0_46FF	DUART1 (UART1 and UART2)		512 bytes
0x0_4700–0x0_48FF	Reserved		512 bytes
0x0_4900–0x0_4AFF	DUART2 (UART3 and UART4)		512 bytes
0x0_4B00–0x0_4FFF	Reserved		1.25 Kbytes
0x0_5000–0x0_5FFF	eLBC		4 Kbytes
0x0_6000–0x0_6FFF	Reserved		4 Kbytes
0x0_7000–0x0_70FF	SPI		256 bytes
0x0_7100–0x0_7FFF	Reserved		3.75 Kbytes
0x0_8000–0x0_82FF	DMA Engine 2		768 bytes
0x0_8300–0x2_83FF	Reserved		256 bytes
0x0_8400–0x0_84FF	I/O sequencer		256 bytes
0x0_8500–0x1_BFFF	Reserved		78.75 Kbytes
0x1_C000–0x1_CFFF	FlexCAN 1 (Reserved on MPC8306S)		4 Kbytes
0x1_D000–0x1_DFFF	FlexCAN 2 (Reserved on MPC8306S)		4 Kbytes
0x1_E000–0x2_2FFF	Reserved		20 Kbytes
0x2_3000–0x2_3FFF	USB DR (Device/ OTG)		4 Kbytes
0x2_4000–0x2_8FFF	Reserved		20 Kbytes
0x2_9000–0x2_9FFF	FlexCAN 3 (Reserved on MPC8306S)		4 Kbytes
0x2_A000–0x2_AFFF	FlexCAN 4 (Reserved on MPC8306S)		4 Kbytes
0x2_B000–0x2_BFFF	Reserved		4 Kbytes
0x2_C000–0x2_DFFF	DMA Engine 1		8 kbytes
0x2_E000–0x2_EFFF	eSDHC (Reserved on MPC8306S)		4 Kbytes
0x2_F000–0xE_FFFF	Reserved		772 Kbytes
0xF_0000–0xF_7FFF	On chip Boot ROM		32 Kbytes
0xF_8000–0xF_FFFF	Reserved		32 kbytes

Table 9. Memory Map (continued)

Block Base Address	Block	Actual Size	Window
0x10_0000–0x1F_FFFF	QUICC Engine		1 Mbytes
0x20_0000–0xFF_FFFF	Reserved		14 Mbytes

5.6 Signal Multiplexing

On MPC8306/S, signal muxing selection is done through programming the System IO Configuration Registers. For details of the SICR registers, refer to the System Configuration section in the *MPC8306 PowerQUICC II Pro Integrated Host Processor Reference Manual*.

6 Hardware/Board Design considerations

6.1 Package and pin-out

MPC8306/S and MC68302 are not package and pin compatible. MPC8306/S is a 0.8mm pitch, 19mm x 19mm 369-MAPBGA device.

6.2 Clocking scheme

The clock inputs frequency specification changes are given in Table 10.

Table 10. Clock Input Frequency

Clock Input	MC68302	MPC8306/S
XTAL-EXTAL	10 MHz to 10.66 MHz crystal	Not applicable
SYS_CLK_IN/EXTCLK	10 MHz to 10.66 MHz OR 45 MHz to 66 MHz	24 MHz to 66.67 MHz
RTC_PIT_CLOCK/PIT_CLK	—	32.768 kHz
QE_CLK_IN	—	24 MHz to 66.67 MHz

For detailed specifications of clocking on MPC8306/S, please refer to the Clocking and Clock Input Timing sections of the *MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications* and *MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

6.3 Power Supply Specifications

Table 11 summarizes the power rails of MC68302 and MPC8306/S.

Table 11. Power rails of MC68302 and MPC8306/S

Rail	MC68302	MPC8306/S
VDD/VDD (Core Power Supply)	3.3V for C.65µ 5V for C.8µ	0.95V to 1.05V
AVDD (PLL power supply)	Not applicable	0.95V to 1.05V
OVDD (I/O power supply)	Not applicable	3.0V to 3.6V
GVDD (DDR2 i/f power supply)	Not applicable	1.7V to 1.9V

NOTE

Signals of MPC8306/S are NOT 5V tolerant. Refer to the *MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications* and *MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications* for the absolute maximum ratings of the device.

A typical power consumption estimate for MPC8306/S is given in Table 12.

Table 12. Power Consumption Estimation

System Configuration e300 = 266 MHz QE = 200 MHz	DDR2 GV_{DD} Power (W)	NV_{DD} Power (W)	Core V_{DD} Power (W)	Total Power (W)
MPC8306/S 16-bit DDR2	0.14	0.15	0.45	0.74

Settings for estimation in Table 12:

Typical Voltages (1.0V for Core VDD, 1.8V for GVDD, 3.3V for NVDD), Temperature at 25 oC ambient.

6.4 Reset Configuration Pins Changes

There are 4 reset source configuration pins for MPC8306/S. Since MPC8306/S supports NAND Flash boot up, there is a pin to either enable or disable ECC checking for NOR Flash during RCW load. The following Table 13 provides all reset configuration signals changes.

Table 13. Reset Configuration Pins

Reset Configuration Signal	MPC8306/S
Configuration Reset Source	CFG_RESET_SOURCE[0:3]
Enable/Disable ECC for Flash during RCW load	LB_POR_CFG_BOOT_ECC
Status of ECC error during boot loading from flash	LBC_PM_REF_10 is an output signal which is not required to be configured.
Configuration clock in division selection	N/A
Selects multiplexing for address/data bus of the LBC block	N/A

6.5 Power supply sequencing

For MPC8306/S, it is advisable to apply VDD and AVDD before applying GVDD and OVDD. Refer to the section on Power Sequencing in the *MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications* and *MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

6.6 Pull-up pull-down Requirement for Miscellaneous Signals

Refer to the section on System Design Information in the *MPC8306 PowerQUICC II Pro Integrated Host Processor Hardware Specifications* and *MPC8306S PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: AN4499
Rev. 0
04/2012