MSC815x and MSC825x DSP Family Design Checklist

This application note identifies resources and provides guidance for developing applications using the MSC815x and MSC825x DSP devices. It includes a check list for design phases of projects that incorporate the DSPs, including:

- *Definition phase*. This document highlights design requirements, such as pin multiplexing, reset timing, and other design considerations.
- *Design implementation phase*. This document reviews relevant issues for schematic development and testing.

NOTE

The MSC815x family includes the MSC8151, MSC8152, MSC8154, MSC8154E, MSC8156, and MSC8156E DSP devices. The MSC825x family includes the MSC8251, MSC8252, MSC8254, and MSC8256 DSP devices.

— Revision 2.1 mask 0M52Y (orderable part number ends in B, for example MSC8156VT100B)

Contents

1 Background

Developing a project that integrates one or more MSC815x/MSC825x devices requires planning that identifies:

- The specific interfaces required for the design.
- How the interfaces are used including whether the interfaces use dedicated signal lines or must share signal lines during device initialization and/or operation (signal multiplexing).
- How the device is initialized/booted during normal operation.

After identifying the high-level system requirements, the designer must define the following hardware requirements:

- Basic power system.
- Clocking system.
- Reset/initialization system.
- Power-up/start-up sequencing system.
- Required memory and memory interface system.
- Interface connections.
- Disposition of unused signal connections to minimize power consumption.

To support the hardware configuration, the designer must also provide software (not discussed in this document) to support device operation, including:

- Device initialization software (reset sequence, booting, and interface setup).
- Interrupt service routines (ISRs) to handle normal DSP core intervention tasks and error interrupts/exceptions.
- Protocol-defined data management and processing software (which may include standard Ethernet frame processing or any of several vocoder implementations, security algorithms for security-enabled devices, and so forth).
- Other software, such as power-management and reporting or overall process management, as required.

The device specific reference manual and core subsystem reference manuals supply the configuration programming information required to develop the application-specific system environment as well as data transfer management and coprocessor execution. The core reference manual provides detailed programming information required to develop the application-specific algorithm core processing software including ISR processing. Support can be provided or recommended by Freescale Semiconductor. Contact your local sales office or representative for additional information.

2 Supporting Documentation

The MSC815x/MSC825x devices are supported by the following types of documentation:

- Product brief. Device specific document that includes a high-level description of critical performance metrics, detailed lists of product features, and an overview of available hardware and software development environment tools.
- Data sheet. Device specific document that provides a general description of product features, functional block diagrams, signal/pin assignment for the device packaging, detailed physical and electrical specifications including operating parameter values, general hardware design guidelines, ordering information, and detailed packaging specifications.
- Reference manuals. Each device is supported by four reference manuals:
  - Device specific. Includes detailed information about the device for each module/subsystem with specific programming models to allow configuration, programming, and operation monitoring. In addition, this document describes device level functionality including interrupt processing and debugging.
  - *SC3850 DSP Core Reference Manual*. Includes a detailed description of core functionality and operation including the core instruction set programming.
  - *MSC8156 SC3850 DSP Core Subsystem Reference Manual*. Includes a detailed description and programming information for the memory management unit (MMU), extended programmable interrupt controller (EPIC), and internal memories (including cache memories) supported in each subsystem.
  - *QUICC Engine Block Reference Manual with Protocol Interworking*. Includes a detailed description and programming information for the QUICC Engine subsystem including the dual RISC processors, internal memory, communication controllers and interfaces, baud rate generators and counters, and lists which components in this subsystem are used by the MSC815x/MSC825x DSPs.
- Application notes. Individual documents that provide specific recommendations and guidelines for configuration and operation of the device for specific applications or for specific interface enablement and optimization.

NOTE

Before starting an application design, refer to the latest device errata document for the corresponding device. Contact your local sales office or representative for details.

3 Power Supply Requirements

The following sections discuss the various aspects to consider for power supply selection and design.

3.1 Power Supply and Ground Inputs

Each MSC815x/MSC825x device requires the power supplies and grounds listed in **Table 1**. Refer to the device specific technical data sheet for minimum and maximum voltage levels.

Table 1. MSC815x/MSC825x Power Inputs

Signal Name	Symbol	Description	Required Voltage
POWER			
VDD	V_{DD}	Core and Internal logic power	1.0 V
M3VDD	V_{DDM3}	M3 memory Power. Only for 1024 KB, the rest 32 KB are powered with V_{DD}.	1.0 V
MVDD	V_{DDM}	MAPLE-B Power	1.0 V
GVDD1, GVDD2	V_{DDDDR}	DDR Interface Power. Each controller has it's own supply.	1.5 V (DDR3) 1.8 V (DDR2)
M1VREF, M2VREF	MV_{REF}	DDR Reference Voltage	= V_{DDDDR}/2 V
NVDD, QVDD	V_{DDIO}	Input/Output Power. MSC815x/MSC825x I/O voltage is 2.5 not like the 814x family which has 3.3 I/O voltage.	2.5 V
SXPVDD1, SXPVDD2	V_{DDSXP}	RapidIO Pad Power (also used for SGMII and PCI Express). Each HSSI port has it's own supply.	1.0 V
SXCVDD1, SXCVDD2	V_{DDSXC}	RapidIO Core Power (also used for SGMII and PCI Express). Each HSSI port has it's own supply.	1.0 V
PLLx_AVDD	V_{DDPLLx}	System PLL x Power (x = 0, 1, 2)	1.0 V
SR1_PLL_AVDD, SR2_PLL_AVDD	$V_{DDRIOPLL}$	RapidIO PLL Power (also used for SGMII and PCI Express)	1.0 V
GROUND			
VSS	GND	Internal logic and I/O Ground	0 V
SR1_PLL_AGND, SR2_PLL_AGND	GND_{RIOPLL}	RapidIO PLL Ground (also used for SGMII and PCI Express)	0 V
SXCVSS1, SXCVSS2	GND_{SXC}	RapidIO Transceiver Core Ground (also used for SGMII and PCI Express)	0 V
SXPVSS1, SXPVSS2	GND_{SXP}	RapidIO Transceiver Pad Ground (also used for SGMII and PCI Express)	0 V

Actual requirements depend on the specific design implementation. Refer to the product-specific technical data sheet for detailed specifications. The data sheet also lists the required reference voltage source for each signal connection. Some implementations may require different voltage levels for the specified power supplies. For example, DDR3 memories use a nominal 1.5 V whereas DDR2 memories use a nominal 1.8 V. Select the appropriate voltage level to meet your design requirements using the values recommended in the device-specific data sheet.

3.2 Power Consumption

Use the following guidelines when considering power consumption and dissipation requirements:

- For each power supply rail, select a source that can supply both the average expected current and peak power requirements. Typical and peak requirements are application dependent. See the device specific technical data sheet for device power characteristics and power supply design recommendations.
- Use the thermal characteristics and consideration guidelines provided in the device-specific data sheet to perform thermal analysis when designing board layout.
- Some applications that do not use some of the device modules can reduce power consumption by connecting some of the power signals to GND instead of the active supply. Refer to the application note *MSC8156 DSP Family Lower Power Modes* (AN4184) for details on powering down certain power domains.
- A power calculator tool is available upon request under NDA. Contact your local sales office or representative for details.

3.3 Decoupling

When developing a specific board design, include decoupling capacitors to minimize noise propagation and maintain proper power levels. It is very important that particular attention is paid to decoupling for the supplies for the PLL circuits to minimize radiated emissions and promote stable frequency generation and clocking. **Section 3.2** of the data sheet includes decoupling guidelines for the PLL power circuits. As a reference, the user can review the design of the MSC8156ADS, available under NDA from Freescale. This board design include:

- Bulk capacitors for V_{DD}. The bulk capacitors decrease low frequency noise. Bulk capacitors should be placed as close as possible to the MSC815x/MSC825x power balls to minimize voltage spikes on the V_{DD}. In the case of the MSC8156/MSC8156E/MSC8256, a total of seven 150 µF capacitors are required. Five of 150 µF need to be placed close to the DSP device as shown in **Figure 1**. For the MSC8151/MSC8152/MSC8154/MSC8154E/MSC8251/MSC8252/MSC8254, a total of five 150 µF capacitors are required. Three of the 150 µF need to be placed close to the DSP device.

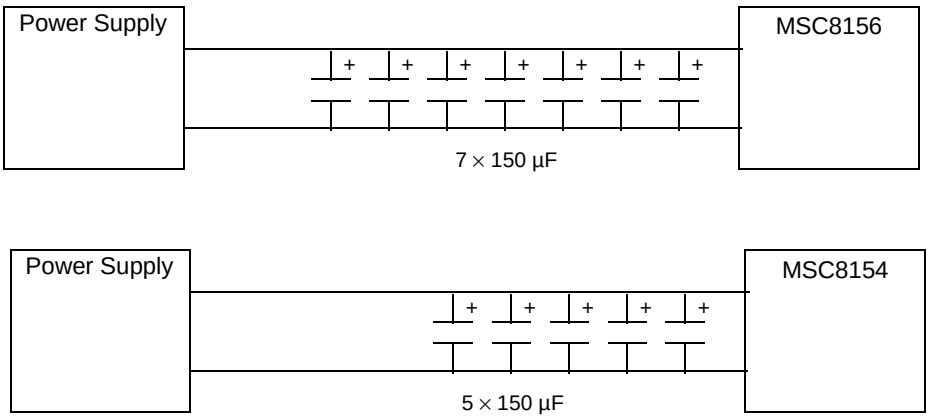


Figure 1. Bulk Capacitors Placement for MSC815x/MSC825x

- Bulk Capacitor for V_{DDDDR} on the MSC815x/MSC825x. Two 47 µF bulk capacitors are placed on V_{DDDDR} (for each of the two controllers) in the MSC815x/MSC825x to decrease low frequency voltage spikes. Bulk capacitors should be placed as close as possible to the DSP device
- Bulk Capacitor for V_{DDM3} on the MSC815x/MSC825x. One 47 µF bulk capacitor is placed on V_{DDM3} in the DSP to decrease low frequency voltage spikes. Bulk capacitors should be placed as close as possible to the DSP.
- Bulk Capacitor for V_{DDM} on the MSC815x/MSC825x. One 47 µF bulk capacitor is placed on V_{DDM} in the DSP device to decrease low frequency voltage spikes. Bulk capacitors should be placed as close as possible to the DSP device.
- Bypass Capacitors for all power supplies on the MSC815x/MSC825x. Should be combined from four types of capacitors. 0.01 µF, 0.1 µF, 1 µF, 4.7 µF bypass. Every power ball should be connected to a 0.01 µF or 0.1 µF or 1 µF capacitor, with the total number to include the same number of capacitors of each value. For example, for 60 power balls, there would be 20 capacitors of each size. Spread three to four 4.7 µF capacitors among the power balls. The capacitors should be ceramic capacitors with low ESR/ESL and placed on the DSP board for filtering high frequency noise. Ceramic capacitors should be placed on the device ball.
- Refer to the device-specific data sheet for details on PLL decoupling circuits.
- In addition to information about power supply decoupling, *AN3634: Designing a Core Power Supply for MSC8144 DSPs* also includes power plane layout and other design tips to achieve a stable voltage supply for the MSC8144 device. You can apply similar guidelines to the MSC815x/MSC825x board design.

3.4 I/O Signal Levels

NOTE

This section is not relevant to Serial RapidIO and DDR I/O signal levels.

The MSC815x/MSC825x GPIO voltage is 2.5 V. Many industrial standard peripheral devices such as I^2C, SPI, and UART devices can support a range of I/O voltage between 1.8 V–3.3 V.

CAUTION

Direction connection of 3.3 V devices can cause damage to the DSP device. Never connect 3.3 V devices directly to the DSP GPIO pins

If the MSC815x/MSC825x device connects to a peripheral device that drives signals with a voltage level that is not 2.5 V (for example, 3.3 V devices that drive the TDM, I^2C, SPI, UART, CLKIN, or RESET signals), the design must employ a voltage translator on the board to avoid applying voltage levels to the DSP above specified nominal values.

The hardware logic of the CodeWarrior USB TAP has two remote power supplies:

- The main logic (power processor, CPLD, and so on) feeds from the Vbus of the USB cable.
- The output buffers are powered from sense signal on pin number 11 of the 14-pin OnCE cable connected to the target, and should be connected to 2.5 V to provide correct signal level on JTAG port.

4 Power-Up Sequence and Start-Up Timing

Device start-up requires a synchronization between starting and applying the various device power supplies. Refer to the Section 3 of the device-specific data sheet for guidelines on power supply ramp-up sequence and timing.

5 System Clocking

The following sections provides guidelines and descriptions for the various clocking systems used with and in the MSC815x/MSC825x.

5.1 Clock Signals

MSC815x/MSC825x devices use clock signals for internal clocking and for synchronous interfaces. Each of the clock signals has its own unique requirements. Clock signals include the following:

- General:
  - CLKIN
  - CLKOUT
- Serial RapidIO/SGMII/PCI-Express:
  - SRx_REF_CLK/$\overline{\text{SRx\_REF\_CLK}}$ (differential pair)
- TDM:
  - TDMxRCK
  - TDMxTCK
- Timers:
  - TMRx
- JTAG:
  - TCK
- DDR:
  - MxCK[0–2]/$\overline{\text{MxCK[0–2]}}$ (differential pairs)
- Ethernet:
  - GEx_RX_CLK
  - GEx_TX_CLK
  - GEx_GTX_CLK
  - GE_MDC
- SPI:
  - SPI_SCK
- I^2C:
  - I2C_SCL

Refer to the device specific technical data sheet in **Section 2.6.1** through **Section 2.6.9** for the individual signals requirements. For each clock signal, make sure that you comply with each of the following specifications:

- Clock frequency limits.
- Clock slope limits.
- Jitter limits.
- Output clock load requirements.
- Clock tree for the DDR-SDRAM balancing with zero delay buffers for large loads.
- Special startup sequencing requirements for clock signals during reset.

As shown in **Chapter 7** *Clocks* of the device-specific reference manual, the MSC815x/MSC825x device has a flexible clocking scheme to deliver the clock frequencies used by the various subsystems and external interfaces. During power-on reset, the user configures a specific clock mode that defines the various clock frequencies and domains in the device. The specific clock mode is selected using the MODCK[5–0] field in the reset configuration word. **Table 7-1** in the device specific reference manual shows the relationships between the input clock (CLKIN) and the mode (MODCK), and the internal clock domains.

Table 7-2 in the device specific reference manual shows the relationships between the mode (MODCK) and the output clock (CLKOUT), according to the CLKOUT configuration defined during power up sequence.

NOTE

For each MODCK selected, a specific frequency is selected for each clock domain and a specific CLKIN frequency is required (66.67 Mhz or 100 Mhz). **Table 7-1** in the device specific reference manual has detailed information about the MODCK options. Evaluate each clock and make sure that CLKIN frequency and clock mode (MODCK) yield the desired internal frequencies.

5.2 Serial RapidIO Reference Clock

Because the serial RapidIO reference clock is an external signal, the detailed description and requirements are discussed with other interface signal requirements. See the device specific data sheet for details.

5.3 QUICC Engine Subsystem Clocks

The QUICC Engine subsystem requires input clocks as shown on the right of **Figure 2** to drive the UCC clock signals. The clock signals for each of the UCCs driven by the MSC815x/MSC825x are based on the clock inputs shown in **Figure 2**, For example, the 125 MHz clock source GTX_CLK125 connects GE1_TX_CLK, which is used to drive GE1_GTX_CLK as a clock output from the MSC815x/MSC825x to the Ethernet PHY. RX_CLK of the Ethernet PHY can connect to GE1_RX_CLK, which is used to drive UCC1 Rx as clock input from the Ethernet PHY. Refer to the device specific data sheet and reference manual for connection options and details.

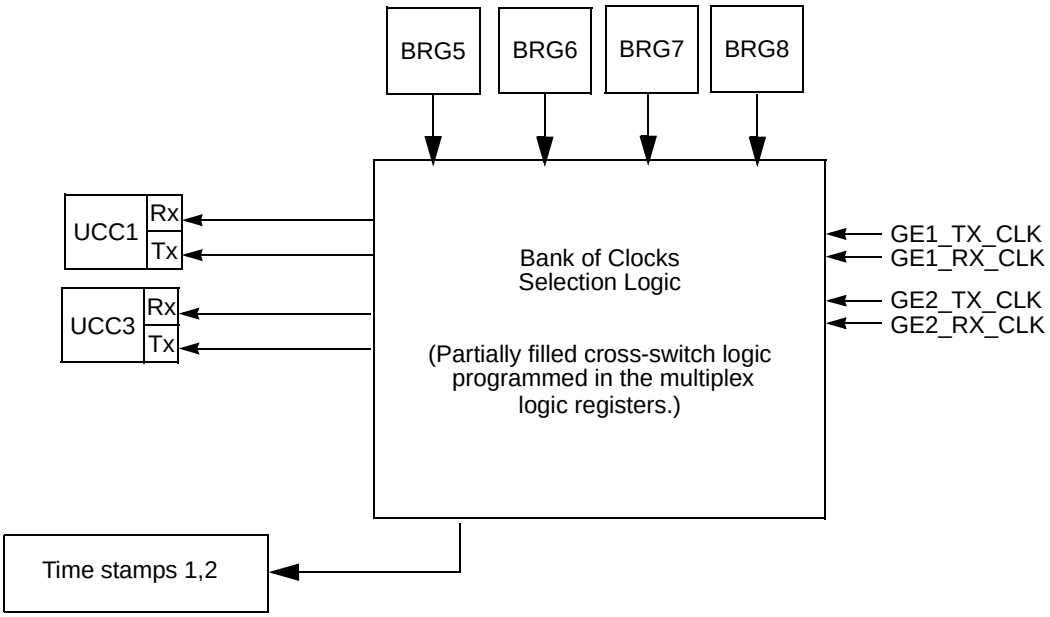


Figure 2. Bank of Clocks in the QUICC Engine Subsystem

Table 2. Clock Source Options Using External Clock Signals

Clock	External CLK			
	GE1_RX_CLK	GE1_TX_CLK	GE2_RX_CLK	GE2_TX_CLK
UCC1 Rx	V			
UCC1 Tx		V		
UCC3 Rx			V	
UCC3 Tx				V
Time Stamp 1			V	V
Time Stamp 2			V	V

Although SPI is part of the QUICC Engine subsystem, it does not receive its clock signal from the Bank of Clocks. SPI_SCK is selected by configuring the GPIO17 signal (see **Chapter 24** *GPIO* in the device specific Reference Manual for details). The clock signal operation (clock invert, clock phase, and clock gap) are configured in the SPIMODE register (see **Chapter 20** *Serial Peripheral Interface (SPI)* in the device specific Reference Manual for details).

5.4 I^2C Clock

I2C_SCL is selected by configuring the GPIO30 signal (see **Chapter 24** *GPIO* in the MSC815x/MSC825x device specific Reference Manual for details). See **Chapter 26** *I^2C* in the MSC815x/MSC825x device specific Reference Manual for details on the clock operation.

5.5 Clock Mode Tool

A spreadsheet tool that calculates all component frequencies depending clock mode and clock source for the MSC815x/MSC825x DSPs is available under NDA. This tool also validates configured clock schemes by clock specifications. **Figure 3** shows an example of the tool spreadsheet. Contact your local Freescale sales office or representative for details.

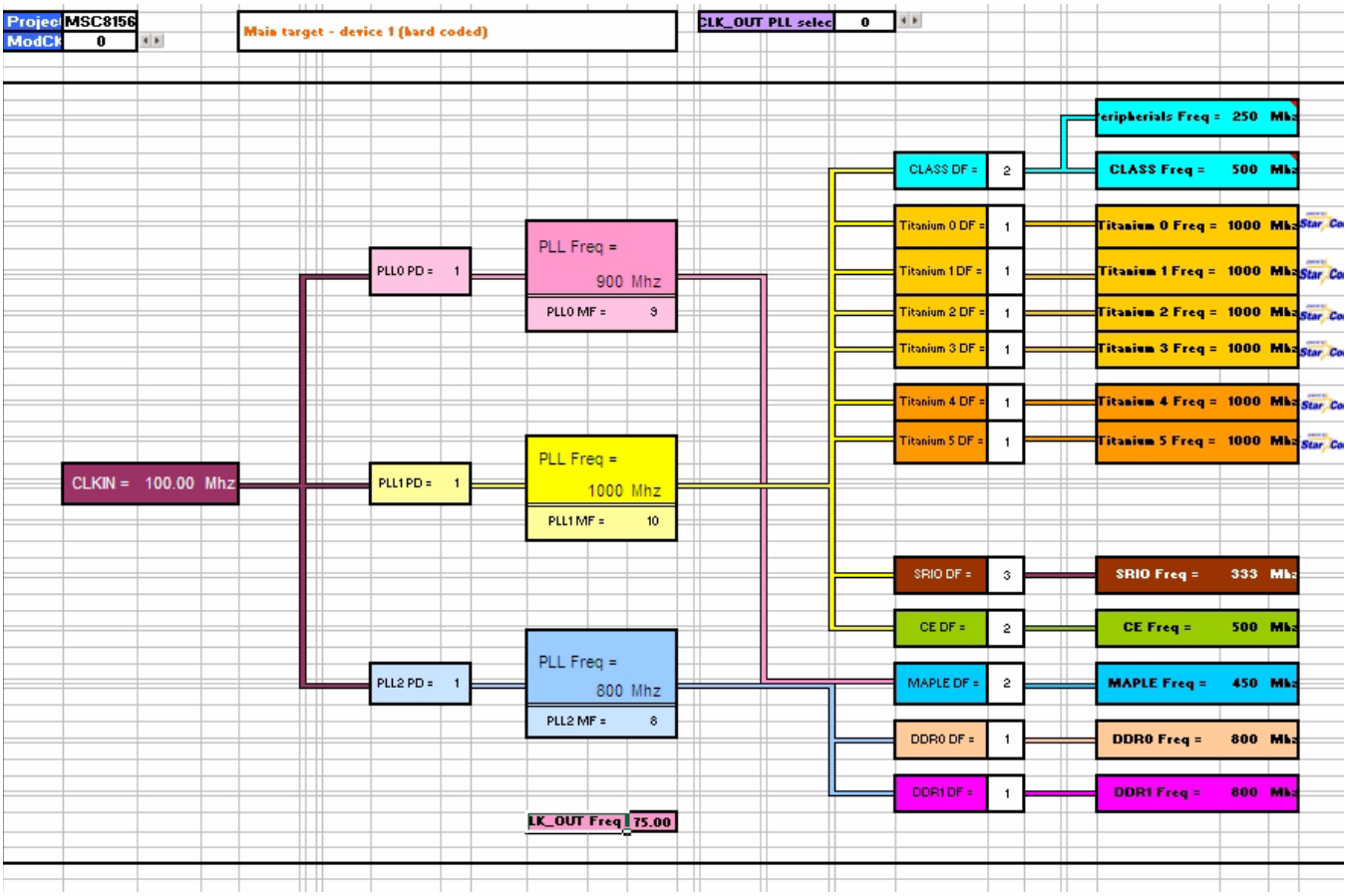


Figure 3. Clock Mode Tool Spreadsheet Example

6 Reset

Use the following reset guidelines:

- Ensure that the $\overline{\text{SRESET}}$ pin is not driven by external logic.
- Connect the $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ pins to 4.7 KΩ pull-up resistors.
- When a debugger is not used, $\overline{\text{TRST}}$ must be tied directly to $\overline{\text{PORESET}}$ as shown in Figure 4.
- When a debugger is used, $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ must be connected as shown in Figure 5.
- Refer to the device data sheet for the $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ electrical requirements.
- Refer to the device reference manual for the functional description of the reset sequence.

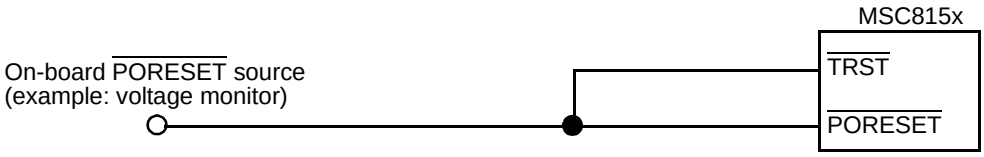


Figure 4. Reset Connection in Functional Application

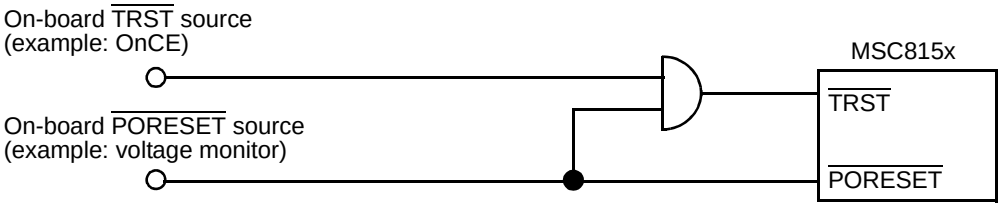


Figure 5. Reset Connection in Debugger Application

7 Boot

Chapter 6 *Boot Program* of the device specific reference manual describes the functionality and operation of the boot program.

Use the following boot guidelines:

- Implement an I^2C EEPROM of at least 8 KB in size in the system to support boot patches.
- Contact your local sales office or representative to obtain the boot patch files.

For additional information, see:

- *Using an I^2C EEPROM During MSC8156 Initialization* (AN3670)
- *Advantages of Using I2C EEPROMs During Reset and Boot Flow for MSC8156 DSPs* (EB728)

8 I/O Multiplexing

Use the following I/O multiplexing guidelines:

- Based on the system requirements, select the required interfaces using the Pin Mux Tool. The tool spreadsheet confirms all pin availability based on application requirements, such as DDR memory, peripherals, GPIO/$\overline{\text{IRQ}}$ pins, and so on. In addition, this tool validates power supplies and displays all pin mapping based for the application. Contact your local sales office or representative to obtain the Pin Mux Tool. **Figure 6**, **Figure 7** and **Figure 8** show examples of the tool spreadsheet displays.
- Verify that all device interfaces meet the AC specifications listed in the data sheet for the DSP device. Note that the AC specifications are specific with regard to external loads. Also, remember to account for signal propagation delays, clock jitter, and any other factors that can impact signal timing.

Configuration Selection			
Item	**Mode Selection**		
Maple	Used		
M3 Size	1056KB		
TDM0	Full duplex (RX/TX clock & sync are shared)	Yes	2 links
TDM1	Full duplex (RX/TX clock & sync are shared)	Yes	2 links
TDM2	None	No	1 link
TDM3	None	No	1 link
Ethernet1	None		
Ethernet2	SGMII on HSSI port #1		
Ethernet Management	Yes		
SPI	Yes		
RapidIO1	None		
RapidIO2	4x 3.125		
PCIe	None		
DDR1	DDR2 32bit	With ECC	
DDR2	DDR2 32bit	With ECC	
DMA External Request #0	Yes		
DMA External Request #1	None		
Uart	None		
I2C	Yes		
JTAG	Yes		

The MSC8156/4 supports that configuration selection.

The selected configuration is supported as is.

Valid, but not power optimal (RapidIO1 1x lane is active as well as SGMII1 lane on port #1). To save power, use SGMII1 on port #1 or move RapidIO to port #1 and use SGMII2 on port #2.

TMR Usage	Free / Used	Select
TMR0	Free	No
TMR1	Free	No
TMR2	Free	No
TMR3	Free	No
TMR4	Free	No

IRQ Usage	Free / Used	Select
IRQ0	Free	No
IRQ1	Free	No
IRQ2	Free	No
IRQ3	Free	No
IRQ4	Free	No
IRQ5	Free	No
IRQ6	Free	No
IRQ7	Free	No
IRQ8	Free	No
IRQ9	Free	No
IRQ10	Free	No
IRQ11	Free	No
IRQ12	Free	No
IRQ13	Free	No
IRQ14	Used for other function	No
IRQ15	Used for other function	No

GPIO Usage	Free / Used
GPIO0	Free
GPIO1	Free
GPIO2	Free
GPIO3	Free
GPIO4	Free
GPIO5	Free
GPIO6	Free
GPIO7	Free
GPIO8	Free
GPIO9	Free
GPIO10	Free
GPIO11	Free
GPIO12	Free
GPIO13	Free
GPIO14	Used for other function
GPIO15	Used for other function
GPIO16	Free
GPIO17	Used for other function
GPIO18	Used for other function
GPIO19	Used for other function
GPIO20	Used for other function
GPIO21	Free
GPIO22	Free

Figure 6. Functions Selection Worksheet in Pin Multiplexing Tool

MSC8156/4 power supplies	Symbol	Supply Connectivity
Core supply voltage	VDD	1.0V
Maple supply voltage	MVDD	1.0V
M3 supply voltage	M3VDD	1.0V
I/O voltage (excluding DDR and RapidIO)	NVDD, QVDD	2.5V
DDR1 memory supply voltage	GVDD1	1.8V
DDR2 memory supply voltage	GVDD2	1.8V
HSSI1 C voltage	SXCVDD1	1.0V
HSSI1 P voltage	SXPVDD1	1.0V
HSSI2 C voltage	SXCVDD2	1.0V
HSSI2 P voltage	SXPVDD2	1.0V
Please see details in the device data sheet as for the right connectivity of the following: VDDPLL0 VDDPLL2, M1VREF, M2VREF, VDDRIOPLL1 and VDDRIOPLL2.		

Figure 7. Power Supplies worksheet in the Pin Multiplexing Tool

Pin #	Ball Name	Pin Name	Selected Functions	Usage during power on reset	Functional Usage	Reference Supply
1	R1	CLKIN	CLKIN	-	USED	QVDD
2	T6	CLKOUT	CLKOUT	-	USED	QVDD
3	T3	PORESET_B	PORESET#	-	USED	QVDD
4	P4	HRESET_B	HRESET#	-	USED	QVDD
5	N3	SRESET_B	SRESET#	-	USED	QVDD
6	R5	STOP_BS	STOP_BS	-	USED	QVDD
7	P5	INT_OUT_B	INT_OUT#	-	USED	QVDD
8	P2	NMI_B	NMI#	-	USED	QVDD
9	P3	NMI_OUT_B	NMI_OUT#	-	USED	QVDD
10	L26	RC21	GND	-	UNUSED	NVDD
11	K21	RCW_LSEL_B_0_RC17	GND	RCW_LSEL_0#	UNUSED	NVDD
12	L25	RCW_LSEL_B_1_RC18	GND	RCW_LSEL_1#	UNUSED	NVDD
13	L22	RCW_LSEL_B_2_RC19	GND	RCW_LSEL_2#	UNUSED	NVDD
14	L21	RCW_LSEL_B_3_RC20	GND	RCW_LSEL_3#	UNUSED	NVDD
15	G28	GPIO0/IRQ0_B/RC0	NC	RCW[0,16,32,48]	UNUSED	NVDD
16	H28	GPIO1/IRQ1_B/RC1	NC	RCW[1,17,33,49]	UNUSED	NVDD
17	K28	GPIO2/IRQ2_B/RC2	NC	RCW[2,18,34,50]	UNUSED	NVDD
18	K26	GPIO3/DRQ1/IRQ3_B/RC3	NC	RCW[3,19,35,51]	UNUSED	NVDD
19	H25	GPIO4/DDN1/IRQ4_B/RC4	NC	RCW[4,20,36,52]	UNUSED	NVDD
20	G27	GPIO5/IRQ5_B/RC5	NC	RCW[5,21,37,53]	UNUSED	NVDD
21	H27	GPIO6/IRQ6_B/RC6	NC	RCW[6,22,38,54]	UNUSED	NVDD
22	K27	GPIO7/IRQ7_B/RC7	NC	RCW[7,23,39,55]	UNUSED	NVDD
23	J26	GPIO8/IRQ8_B/RC8	NC	RCW[8,24,40,56]	UNUSED	NVDD
24	H26	GPIO9/IRQ9_B/RC9	NC	RCW[9,25,41,57]	UNUSED	NVDD
25	G26	GPIO10/IRQ10_B/RC10	NC	RCW[10,26,42,58]	UNUSED	NVDD
26	K25	GPIO11/IRQ11_B/RC11	NC	RCW[11,27,43,59]	UNUSED	NVDD
27	J25	GPIO12/IRQ12_B/RC12	NC	RCW[12,28,44,60]	UNUSED	NVDD
28	E24	GPIO13/IRQ13_B/RC13	NC	RCW[13,29,45,61]	UNUSED	NVDD

Figure 8. Pin Mapping worksheet in the Pin Multiplexing Tool

9 Identifying the Device ID and Revision Number

The MSC815x/MSC825x devices have several places that carry the Device ID and Revision Number information. **Table 3** summarize all the locations where software can explore the Device ID and Revision Number and identify the device type and mask set accordingly.

Table 3. MSC815x/MSC825x Rev 2.1 Device ID and Revision Number sources (Mask set number: 0M52Y)

Device	SRIO		PEX		GCR		JTAG
	DIDCAR[DI]	DICAR[DR]	Device ID [1]	Rev. ID [2]	SPRIDR[PARTID][3]	SPRIDR[REVID]	JTAGID [4]
MSC8151	1810	1	1810	1	8304	1	1189_001D
MSC8152	1810	1	1810	1	8304	1	1189_001D
MSC8154	1810	1	1810	1	8304	1	1189_001D
MSC8154E	1812	1	1812	1	830C	1	1189_101D
MSC8156	1818	1	1818	1	8302	1	1189_401D
MSC8156E	181A	1	181A	1	830A	1	1189_501D
MSC8251	1810	1	1810	1	8304	1	1189_001D
MSC8252	1810	1	1810	1	8304	1	1189_001D
MSC8254	1810	1	1810	1	8304	1	1189_001D
MSC8256	1818	1	1818	1	8302	1	1189_401D

1 PCI Express Device ID is accessed at offset 0x02 for common PCI configuration registers.

2 PCI Express Revision ID is accessed at offset 0x08 for common PCI configuration registers.

3 SPRIDR reside at address 0xFFF2_8028.

4 JTAGID is accessed by JTAG initiator through the Test Access Port (TAP).

10 DDR External Memory Use

Careful consideration must be given to the design and implementation of the external memory subsystem. The DDR memory supported by MSC815x/MSC825x devices is a high-frequency memory interface and the printed circuit board (PCB) design must be done carefully and verified with a simulation tool. The following list highlights the main issues to consider in such a design:

- Perform simulation for board layout to select proper termination. Use simulation output for AC timing calculation.
- Perform detailed timing analysis for AC spec between MSC815x/MSC825x and DDR-SDRAM device, include signal propagation delay, coupling, termination mismatch, trace mismatch, and clock skew.

10.1 SSTL-1.5/1.8 V Interface and Board Design Guideline

DDR memory adopts the SSTL-1.5/1.8 V interface shown in **Figure 9**. V_{TT} and V_{REF} mean half voltage of V_{DDQ} in DDR memory. V_{DDQ} in DDR memory and V_{DDDDR} in MSC815x/MSC825x device share a power supply of 1.8 V for DDR2 or 1.5 V for DDR3. V_{REF} in DDR memory and MV_{REF} in MSC815x/MSC825x device share a half voltage of power supply of 1.8 V for DDR2 or 1.5 V for DDR3.

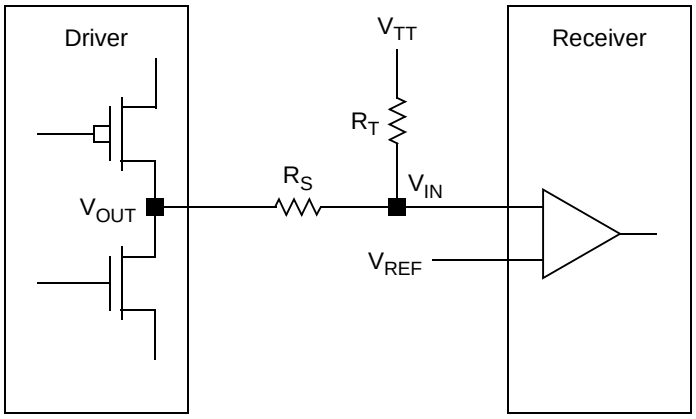


Figure 9. Typical Memory Interface Using Class II Option

- V_{TT} and V_{REF} should have DC values as close as possible (VREF should track VTT and GVDD) VTT, VREF = 1/2 GVDD. VTT should be generated from IC and VREF can be either generated from the same IC or resistor's divider of 100 OHM with tolerance better than 1% from GVDD. Refer to the MSC8156 ADS schematics for reference.
- V_{REF} should be isolated from noise by space and three decoupling capacitors of 0.1 µF, 0.01 µF, and 4.7µF. Refer to the MSC8156 ADS schematics for reference.
- Use on-die termination for data, strobe and mask pins. Use Rt termination for address and control pins.Values of termination depends on board implementation; therefore, all termination values are determined from waveform simulation

- Use the following DDR routing order:
  1. Power (VTT, VREF).
  2. Data
  3. Address / command. DDR3 Address and Command signals should be routed according to flyby topology - refer to DDR3 JEDEC standard.
  4. Control
  5. Clocks.- Clock termination should be implemented close to the memory component
- Select appropriate power supply level for design and simulation.
- If multiple MSC815x/MSC825x DSP devices reside closely on a board, route adjacent DDR data groups on alternating critical board layers to reduce crosstalk.
- In DSP farms, simultaneous switching draws more power if the DDR clocks on DSPs are synchronized. MSC815x/MSC825x PLL outputs are synchronized to a relevant CLKIN. Using a clock tree on the board that provides a phase-shifted CLKIN to each MSC815x/MSC825x on the board prevents simultaneous switching.
- MxODT[0–1] and MxCKE[0–1] pins work with each chip select $\overline{\text{MxCS[0–1]}}$. Tie MxODT[0–1] and MxCKE[0–1] on DDR controller to ODT and CKE on individual SDRAM corresponding to $\overline{\text{MxCS[0–1]}}$.
- User may swap any data bit 0 (DQ0) within a certain byte (at the memory component) to any data bit of same the same byte in the DDR component. For example DSP DQ0 can connect to any bit from DQ0 to DQ7 in the memory component.
- User may swap between any data byte between the DSP and the memory component. For example DSP DQ0 can connect to any bit from DQ0 to DQ7 in the memory component. Note that the corresponding DQS and DM should follow the data connection.For example DQ0 to DQ7, DQS0,$\overline{\text{DQS0}}$ and DM0 (byte 0) can be connected to DQ8 to DQ15, DQS1,$\overline{\text{DQS1}}$ and DM1 (byte 1) in the memory component
- The DDR3 controller supports the ZQ calibration commands ZQCL, ZQCS by DDR_ZQ_CNTL. To use the ZQ calibration function, a 240 Ω ± 1% tolerance resistor must be connected between the ZQ pin of the DDR3 memory and ground.

Use the following guidelines for the DDR3 memory connectivity:

- bRESET needs to be asserted low at power up.
- VREFCA needs to be routed to V_{REF} for address/command.
- VREFDQ needs to be routed to V_{REF} for data.
- TDQS/TDQS# are not supported by the MSC815x/MSC825x DDR3 controller.

10.2 Memory Signal Termination

The DDR controller supports both DDR2 and DDR3 SDRAM. Each memory type requires different signal termination combinations:

- If the DDR controller is configured for DDR2:
  - Connect MxMDIC0 to GND through an 18-Ω precision 1% resistor.
  - Connect MxMDIC1 to V_{DDDDR} through an 18-Ω precision 1% resistor.
- If the DDR controller is configured for DDR3:
  - Connect MxMDIC0 to GND through an 36-Ω precision 1% resistor.
  - Connect MxMDIC1 to V_{DDDDR} through an 36-Ω precision 1% resistor.

NOTE

MxMDIC[0–1] are used for the automatic impedance calibration.
The drive calibration is independently enabled/disabled while in full strength mode. There is no drive calibration while in half strength mode.

For guidelines to terminate unused memory signal lines please refer to the Pin Mux Tool and data sheet.

The following documents (available at www.freescale.com) provide additional detailed design guidelines:

- *MSC8154/6 Hardware and Layout Design Considerations for DDR2 and DDR3 SDRAM Memory Interfaces* (AN3658).
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582).
- *Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces* (AN2910)

11 Interface Connections

The following sections provide general guidelines for the various communication interfaces supported by MSC815x/MSC825x devices.

11.1 SPI

The MSC815x/MSC825x SPI can be programmed to work in a single- or multiple-master environment.

11.1.1 SPI as a Master Device

In master mode, the SPI sends a message to the slave peripheral, which sends back a simultaneous reply. A single-master device with multiple slaves can use general-purpose parallel I/O signals to selectively enable slaves, as shown in **Figure 10**. To eliminate the multi-master error in a single-master environment, the master $\overline{\text{SPI\_SL}}$ input can be forced inactive by clearing PAR[DD20] in the GPIO registers to 0 forcing the GPIO20/$\overline{\text{SPI\_SL}}$ signal to function as GPIO.

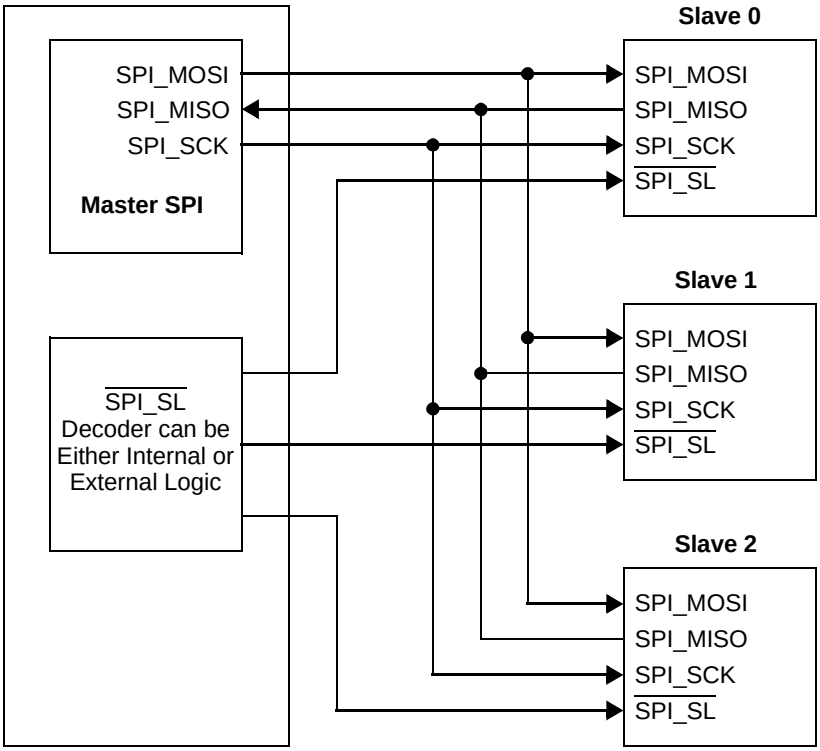
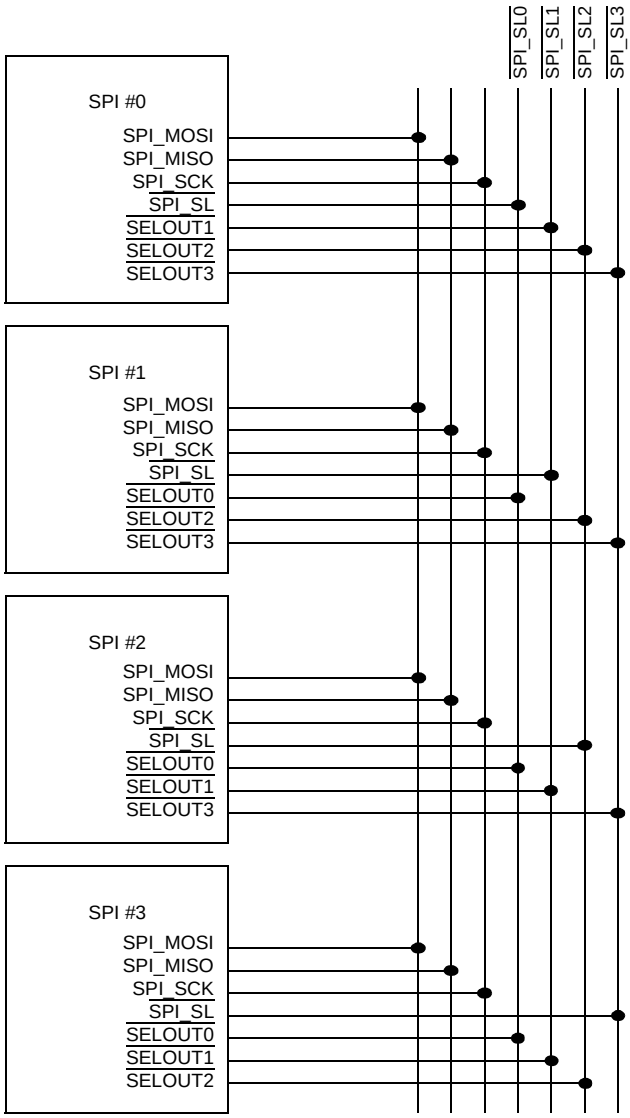


Figure 10. Single-Master/Multi-Slave Configuration

11.1.2 SPI in Multi-Master Operation

The SPI can operate in a multi-master environment in which SPI devices are connected to the same bus. In this configuration, the SPI_MOSI, SPI_MISO, and SPI_SCK signals of all SPIs are shared; the SPI_SL inputs are connected separately, as shown in **Figure 11**. Only one SPI device at a time can act as a master—all others must be slaves.



Notes:
- All signals are open-drain
- For a multi-master system with more than 2 masters, SPI_SL and SPIE[MME] do not detect all possible conflicts.
- It is the responsibility of the software to arbitrate for the SPI bus (with token passing, for example).
- SELOUTx signals are implemented in the software using general-purpose I/O signals.

Figure 11. Multimaster Configuration

11.1.3 General SPI Guidelines

Use the following guidelines for SPI connections:

- Connect the device as shown in **Figure 10** or **Figure 11** as appropriate for your system.
- A 4.7 to 10 KΩ pull-up resistor is recommended for SPI_MISO.
- If MSC815x/MSC825x SPI pins are not in use please follow the recommendation in PINMUX tool and data sheet
- Route SPI_SCK, SPI_MOSI, and SPI_MISO in a daisy chain fashion, keeping stubs as minimal as possible.
- Refer to the device specific data sheet from timing specifications. The maximum distance between the MSC815x/MSC825x and other SPI devices on the SPI bus is limited by desired operating frequency.

11.2 Ethernet

The MSC815x/MSC825x has two Ethernet controllers supported by the QUICC Engine subsystem. Each controller supports two standard MAC-PHY interfaces to connect to an external Ethernet transceiver. Supported interfaces include:

- 1000/100 Mbps RGMII interface (multiplexed with TDM)
- 1000 Mbps SGMII interface (connected externally using SerDes lines via the HSSI)

11.2.1 General Ethernet Guidelines

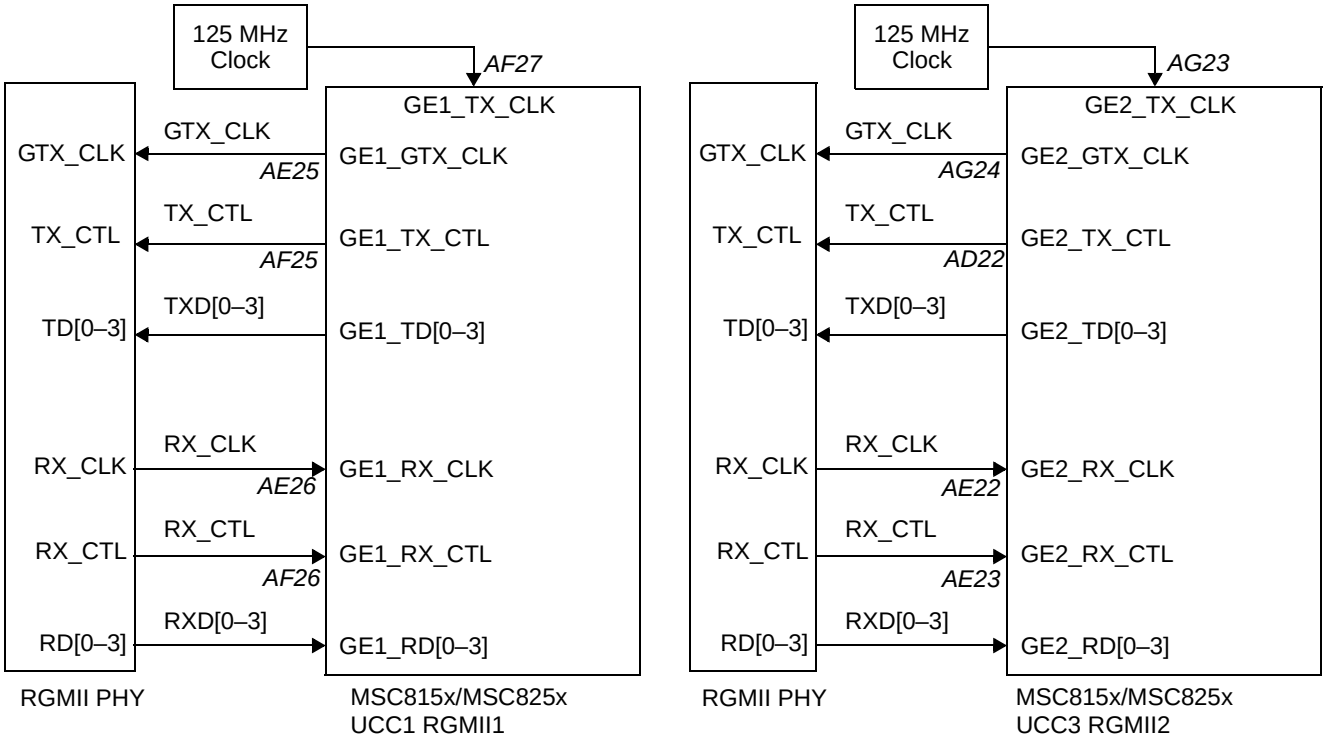
Use the following guidelines for designing an Ethernet interface into a system:

- **Chapter 3** of the reference manual identifies the correct signals to use for each Ethernet controller and interface type.
- The signal list in the technical data sheet identifies the signal by ball location. Use this list to check your schematic for proper connectivity.
- The SGMII mode uses a SerDes interface with differential pair signals. Refer to the technical data sheet for detailed specifications and operating descriptions. The RCW selects the SerDes interface for SGMII, see description in Section 5.3.1 *Reset Configuration Word Low Register (RCWLR)* of the device reference manual.
- For using the GE_MDIO and GE_MDC signals consider whether an external host processor can manage Ethernet PHY instead of MSC815x/MSC825x device. If GE_MDIO and GE_MDC are not used, terminate the signals as described in **Table 47** in the MSC815x/MSC825x device specific data sheet.
- Terminate any unused Ethernet signal lines (that are also not multiplexed for any other use) as described in **Table 46** of the MSC815x/MSC825x device specific data sheet.
- The general rules for connecting the RGMII output lines to the RGMII PHY are:
  - If the trace is long (>2 inches) and the line impedance is not 50 Ω, you should add a 22 Ω termination resistor near the MSC815x/MSC825x output transmit lines.

— If the trace that exists between the MSC815x/MSC825x and the PHY is very short, you can just use a direct connection without the additional termination resistor

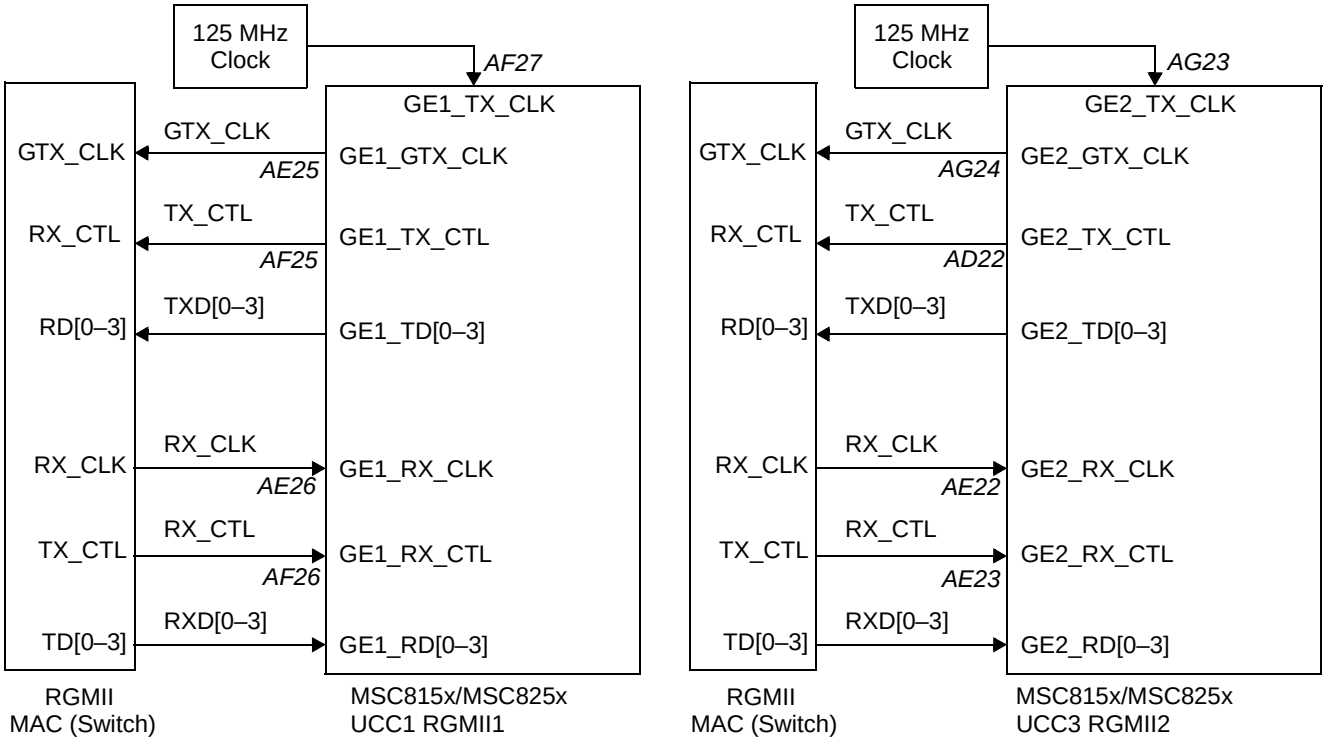
11.2.2 RGMII Considerations

- Unlike MSC814x, RGMII related pin naming for the 2 Ethernet controllers, carry the same naming convention. **Figure 12** shows an example of connecting each of the controllers to an RGMII PHY and **Figure 13** shows an example of connecting each of the controllers to an RGMII MAC or switch.
- Board designers must pay special attention to the clock-to-data skew for RGMII signals. Refer to the application note *RGMII Ethernet Timing in StarCore Based MSC8156 DSPs (AN4101)* for details on adjusting the Ethernet clock and delay timing using the General Configuration Register 4 (GCR4).
- For a MAC-to-MAC connection, the GCR4 must be programmed to compensate for the clock-to-data skew.
- For a MAC-to-PHY connection, most PHYs already include delay logic that can compensate for this delay.



Note: The letter-number combinations next to the MSC815x/MSC825x indicate the ball grid array location for the signal connection.

Figure 12. RGMII MAC-to-PHY Connection Example



Note: The letter-number combinations next to the MSC815x/MSC825x indicate the ball grid array location for the signal connection.

Figure 13. RGMII MAC-to-MAC Connection Example

11.3 HSSI-SerDes Interface for Serial RapidIO, PCI Express and SGMII Connections

The MSC815x/MSC825x supports Serial Rapid IO, PCI Express and SGMII interfaces in many combinations over the 2 HSSI (High Speed Serial Interface) ports. Use the following considerations when implementing these interfaces in your design:

- Use the Pin Mux Tool to confirm all pin availability based on application requirements.
- The signal list in the technical data sheet identifies the signals by ball location. Use this list to check your schematic for proper connectivity.
- If choosing a configuration in which Serial RapidIO is working in x1 mode, the Serial RapidIO functional lane is lane 0 only. Working in x1 mode on lane 2 is not supported by the MSC815x/MSC825x devices.
- For HSSI port 1, lanes 2 and 3 are multiplexed between the Serial RapidIO x4 and the SGMII Ethernet interface. When using the Serial RapidIO interface with one or both SGMII Ethernet interfaces, you can only operate the RapidIO interface in x1 mode. Refer to **Chapters 15** *High Speed Serial Interface (HSSI) Subsystem* **and 16** *Serial RapidIO® Controller* in the reference manual for operating details.
- For HSSI port 2, lanes 0, 1, 2 and 3 are multiplexed between the Serial RapidIO x4, the PCI Express and the SGMII Ethernet interface. When using the Serial RapidIO interface with one or both

SGMII Ethernet interfaces or with the PCI Express interface, you can only operate the RapidIO interface in x1 mode. Refer to **Chapters 15** *High Speed Serial Interface (HSSI) Subsystem* **and 16** *Serial RapidIO® Controller* in the reference manual for operating details.

- There are limitations when using the SGMII or the PCI Express and the RapidIO interface simultaneously on the same HSSI port. Because the SGMII has a fixed 1.25 Gbaud rate and the PCI Express has a fixed 2.5 Gbaud rate, it restricts the serial RapidIO interface operation to 1.25 or 2.5 Gbaud only. That is, you cannot use a 3.125 Gbaud serial RapidIO interface in parallel with the SGMII at 1.25 Gbaud or the PCI Express at 2.5 Gbaud. The possible combinations are controlled by RCWLR[S1P] and RCWLR[S2P]. See the *Reset* chapter in the device specific reference manual for details.
- There are two options for the HSSI power supply source:
  - The same power supply as the core power supply with an LC filter
  - A dedicated power supply
- Connect proper supply levels according to the specifications defined in the technical data sheet and in the PINMUX spreadsheet.
- Because it is a high frequency interface, perform detailed signal integrity analysis for the HSSI using simulations. Check that the eye opening fit system definition for your system and baud rate. See 2.6.2.3 *Serial RapidIO AC Timing Specifications* for the interface in the device specific technical data sheet. Base all simulations on the device IBIS models, available from you local Freescale sales office or representative.
- The HSSI differential output voltage comply with the RapidIO protocol for both “short” and “long” run without any change in the device supply levels (unlike the MSC814x devices in which different voltages were used for “short” and “long” run configurations). Make sure your system fits the transmitter supply output voltages of the device as defined in the device specific technical data sheet.

11.3.1 HSSI Signals Termination

11.3.1.1 Impedance Calibration Signals

There are two inputs (per port) used for automatic impedance calibration by the SerDes initialization when the RCW activates SerDes interface during the reset sequence. These pins must be terminated as follows.

- SR[1–2]_IMP_CAL_RX is pulled down to GND with 200 Ω (±1%) resistor.
- SR[1–2]_IMP_CAL_TX is pulled down to GND with 100 Ω (±1%) resistor.

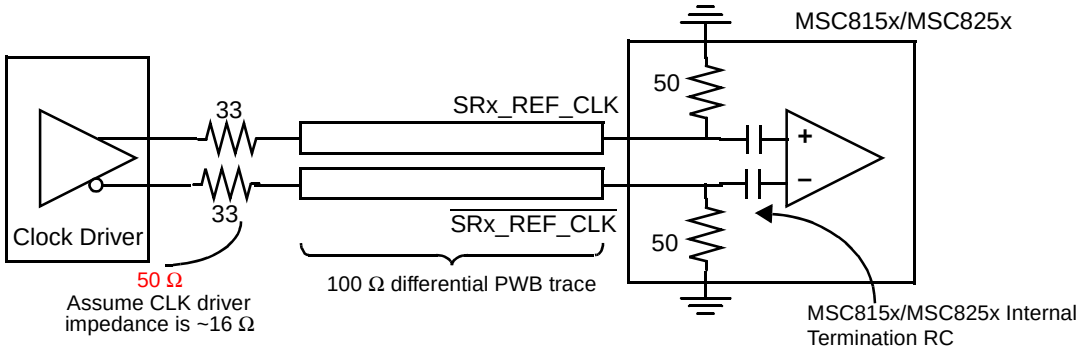
11.3.1.2 Unused Port or Lanes

In the event that one of the HSSI ports is not used, or that some lanes in a port are not used due to a specific port configuration (for example in case RCWLR[S2P] = “01010” meaning that the functional signals are those for PCI Express x1 with SGMII1 and with SGMII2, so Port 2 signals SR2_<RXD1/TXD1>/PE_<RXD1/TXD1> (lane 1) are not used), terminate the unused lanes as described in **Section 3.5.2** *HSSI Related Pins* in the MSC815x/MSC825x device specific data sheet.

11.3.2 Reference Clock Guideline

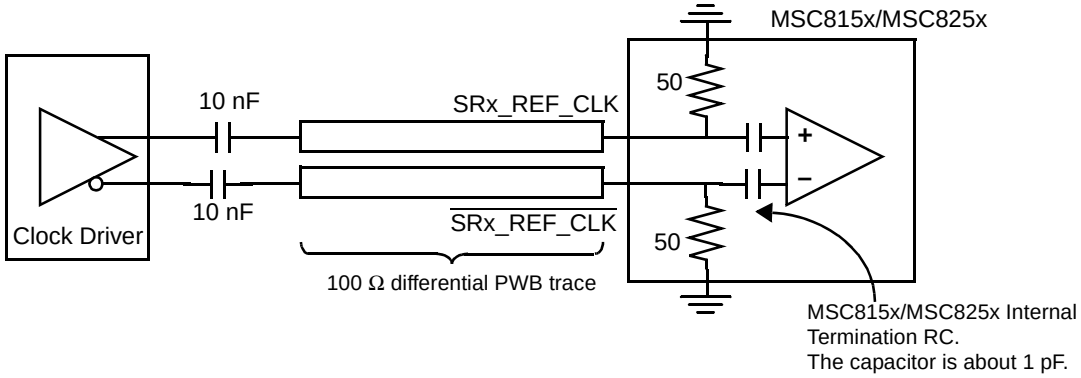
The SerDes reference clock inputs are SR<1/2>_REF_CLK and $\overline{\text{SR<1/2>\_REF\_CLK}}$. The design guidelines are written in **Section 2.5.2.2** in the data sheet.

- The MSC815x/MSC825x reference clock input (SRx_REF_CLK/$\overline{\text{SRx\_REF\_CLK}}$) input is CML type.
- The following examples shows MSC815x/MSC825x differential reference clock input (CML) connection to HCSL or LVDS drivers (see **Figure 14** and **Figure 15**).



Note: This design assumes that the CLK driver levels are compatible with the MSC81x/MSC825x clock input.

Figure 14. HCSL-Compatible Differential Clock



Note: This design assumes that the LVDS output has the driver with a 50 Ω termination resistor and that the transmitter establishes its own common mode level and does not rely on the receiver or external components for this.

Figure 15. LVDS-Compatible Differential Clock

11.3.3 SerDes Data Lane Guideline

Use the following guidelines for designing data lanes into a system:

- The board must have an AC coupling capacitor on each one of the MSC815x/MSC825x receive or transmit connections depending on the protocol used. DC coupling connection is not supported. These capacitors ensure proper conditions for the RapidIO receivers independent of the driving device, as long as the driving device complies with the RapidIO standard. To clarify, two capacitors are required for each lane. Therefore, for a x4 connection, 8 capacitors are required. The recommended capacitor values are:
  - SRIO/SGMII connection. Place a 0.01 µF capacitor on the receiver side near the DSP. Part number ECJ0EB1C103K (10 nF) is recommended as shown in **Figure 16**.
  - PCI Express connection. Place a 0.1 µF capacitor on the transmitter side near the DSP as shown in **Figure 17**.
- The on chip AC coupling must be enabled together with the on board AC coupling capacitor, resulting 2 series capacitors.

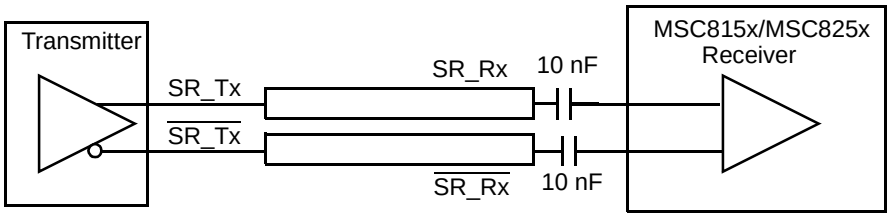


Figure 16. SRIO/SGMII SerDes Transmitter to Receiver Connection

- Figure 16 is an example for SRIO blocking capacitor connection
- For PCI Express, blocking capacitors should be placed on the MSC815x/MSC825x transmitter side as shown in Figure 17. In PCI Express blocking capacitors should be 100 nf.

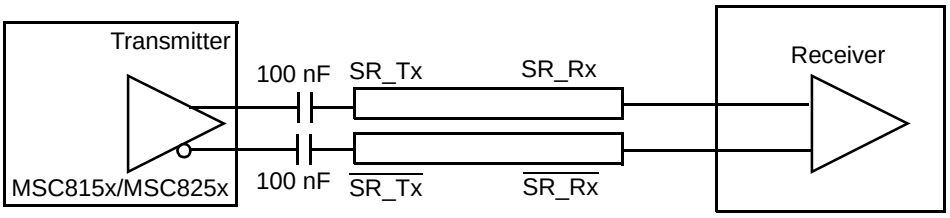


Figure 17. PCI Express SerDes Transmitter Connection

- Refer to the device specific data sheet for all SerDes clock specifications.

11.4 UART

The MSC815x/MSC825x devices support a UART interface that can be operated in half duplex (single wire) or full duplex mode (**Chapter 22** *UART* in the reference manual for more details). The UART is multiplexed on the GPIO signals (GPIO28/UART_RXD and GPIO29/UART_TXD) and must be selected by configuring its functionality through the GPIO configuration (see **Chapter 24** *GPIO* in the reference manual for programming details). Use the following guidelines when designing the UART signal interface:

- Select the connection type (half duplex single wire or full duplex) and identify the proper signal connection locations (only UART_TXD for half duplex) using the signal list in the technical data sheet.
- MSC815x/MSC825x UART_TXD is driven only when data is transmitted, so connect a pull-up resistor to this connection to avoid a floating signal.
- If UART_RXD is not connected to a full drive initiator, connect a pull-up resistor to avoid a floating signal.

11.5 I^2C

The MSC815x/MSC825x devices support an I^2C interface that is supported in all I/O modes, but must be selected by configuring its functionality through the GPIO configuration (see **Chapter 24** *GPIO* in the reference manual for programming details). Typically, this interface is used for loading the Reset Configuration Word (RCW) and booting the device from an EEPROM. The I^2C is also used to load boot patches from the EEPROM.

The I^2C guidelines are as follows:

- You must use at least as large as 64 Kbit I^2C EEPROM for booting from Ethernet or SRIO.
- The I^2C standard specification requires a pull up resistor on I2C_SDA and I2C_SCL depends on the capacitance of the lines but should not be less than 1 KΩ. The I2C_SDA pull up resistor should be three times the size of the I2C_SCL resistor, and should be at least 3 KΩ.
- The I^2C port on the MSC815x/MSC825x devices supports a maximum 400 kHz frequency, also known as I^2C fast mode. The I^2C access frequency varies depending on the following two conditions:
  - The rise time, which is determined by the time constant formed by the pull up resistor and bus load capacitance.
  - The low assertion duration on I2C_SCL, which is determined by the device with the longest low period. See **Section 26.4.6** *Clock Synchronization* and **Section 26.4.8** *Clock Stretching* in the reference manual for details.
- The I^2C standard specification defines the maximum rise time (tr) as 300 ns and the maximum load capacitance on the bus line (Cb) as 400 pF. In order to avoid violating the specification, make sure your design follow these guidelines:
  - Use a minimum 1 kΩ load pull-up resistor on SCL.
  - Make sure that the SCL line rise time does not violate the I^2C specification.

11.6 JTAG

MSC815x/MSC825x devices provide a JTAG interface for debugging designed to conform to the **IEEE 1149.1** specification. The interface supports the boundary scan architecture and provides access to the standard Test Access Port (TAP) controller that performs the standard JTAG tasks and provides access to the internal OCE blocks in the SC3850 cores. See the MSC815x/MSC825x device specific Reference Manual **Table 3-16**. *JTAG TAP Signals* for signal descriptions.

- For debugging using the CodeWarrior USB TAP controller to connect to CodeWarrior for StarCore DSP, you must use the JTAG 14-pin connector. If using more than one MSC815x/MSC825x DSP, consider using a single JTAG connector with the DSPs connected in a JTAG chain, as shown in **Figure 18**.

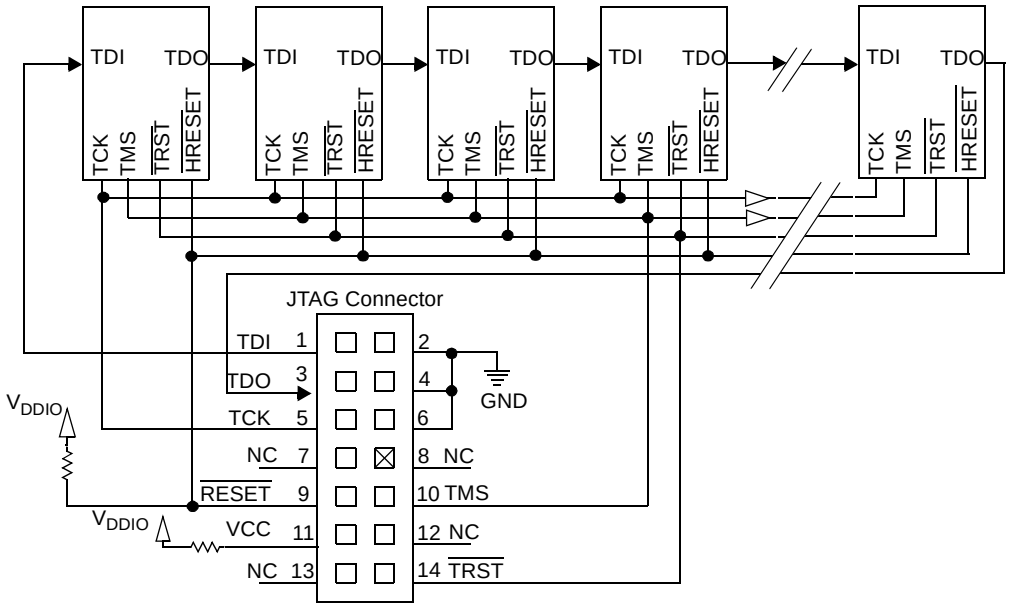


Figure 18. Multiple Target DSP Connection - Reset to All DSPs

- Special consideration must be given to the assertion/deassertion of the $\overline{\text{TRST}}$ signal. **Section 4**, *Power-Up Sequence and Start-Up Timing* in this document mentions that the $\overline{\text{TRST}}$ signal must be asserted during power up. Detailed connectivity guidelines for $\overline{\text{TRST}}$ pin are described in the device data sheet, section 3.1.3 “Reset Guidelines”.
- To meet the AC timing requirements of the JTAG pins, a buffer should be placed on TCK and TMS to maintain signal integrity when there are more than four DSPs in the chain. Each buffer should drive no more than four loads. The CodeWarrior tool can change TCK frequency and the default setting for TCK frequency is 8 MHz which is slower than maximum TCK frequency specification on an MSC815x/MSC825x device.

- The V_{CC} pin (11) on the JTAG connector is sensed by the USB TAP to determine if power is applied to the target. This signal is also used as a voltage reference for the signals driven by the USB TAP probe (TDI, TCK, TMS, $\overline{\text{RESET}}$, and $\overline{\text{TRST}}$). On the MSC8156ADS, the V_{CC} pin 11 is pulled up to V_{DDIO} using a 22 Ω current limited resistor.
- MSC815x/MSC825x JTAG devices run at 2.5 V. Because the USB TAP probe automatically supports target signal levels from 1.8 V to 3.3 V, you can connect the USB TAP directly to JTAG of MSC815x/MSC825x. Refer to the *CodeWarrior™ USB TAP User's Guide* included with the CodeWarrior for StarCore DSP IDE for additional details.
- In **Figure 18**, all $\overline{\text{HRESET}}$ pins of the DSPs are connected to the $\overline{\text{RESET}}$ pin 9 of JTAG connector so that the debugger tool can assert $\overline{\text{HRESET}}$ to all DSPs at a time. In order to reset an individual DSP in a multiple DSP connection, the connection shown in **Figure 19** can be implemented. This connection scheme buffers the reset signals of the DSPs to allow an individual DSP to be reset without affecting the reset of the other DSPs.

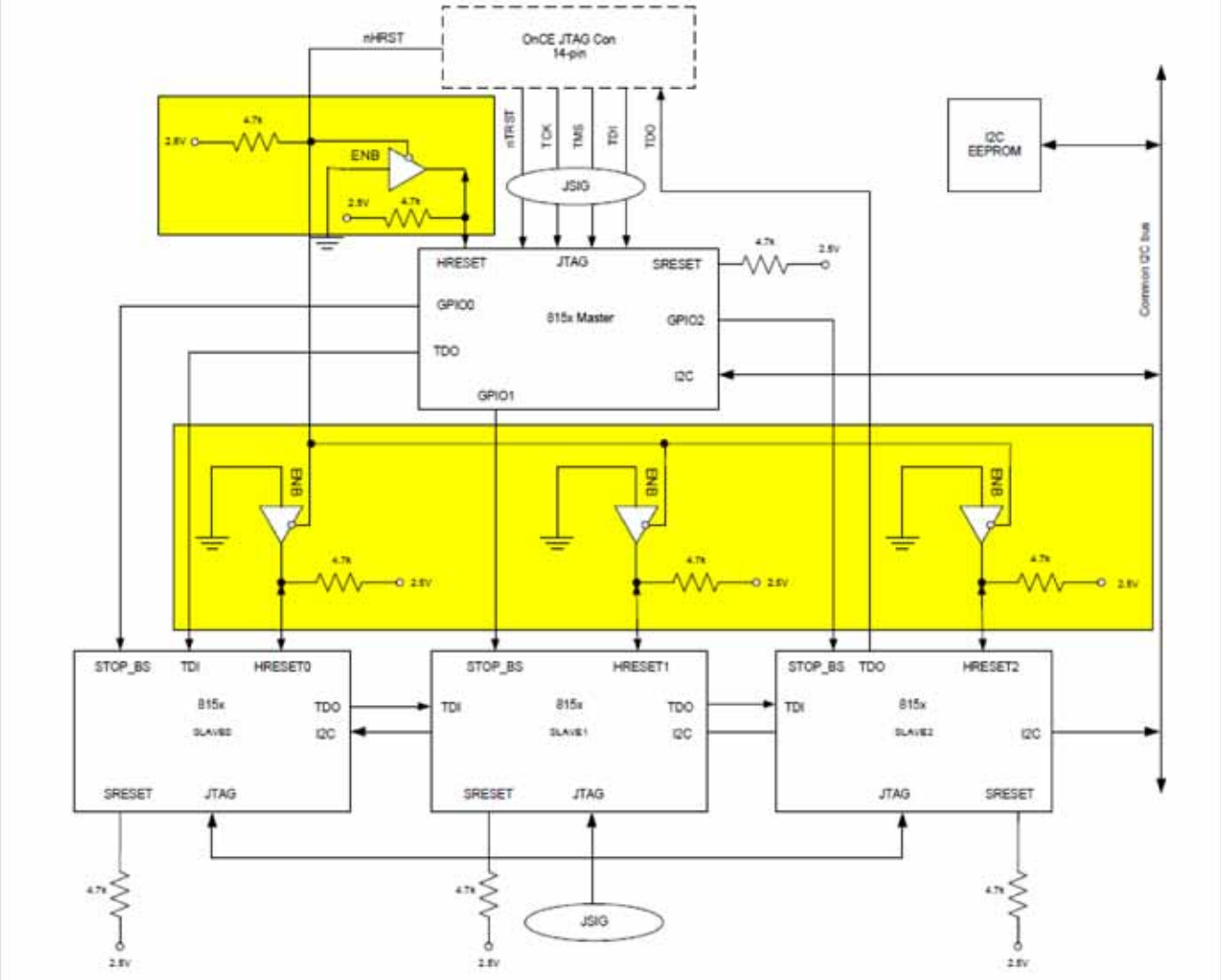


Figure 19. Multiple Target DSP Connection - Reset to Individual DSP

- The Code Warrior for StarCore DSP tool can work on a single JTAG chain that can include multiple MSC815x/MSC825x devices and also other type of devices, both Freescale and non-Freescale. For additional information, see *CodeWarrior USB TAP Users Guide*. Further information can also be found from the CodeWarrior “Help” option:
  - Help -> Help Contents -> Targeting StarCore DSPs > Multi-Core Debugging > Debugging Multi-Core Projects

11.7 Boundary Scan

- The user must make sure that if any device interface is removed (not used for functional application), the patterns generated do not compare the expected values for these pins. The BSDL supplied by Freescale includes all of the device pins.
- The BSDL file sets PORESET to 0 during boundary scan.
- In the BSDL file, DFT_TEST must be set 0.

12 Open Drain Pins

The following signals use open drain pins and must have appropriate pull up resistor attached to them on the board: $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$.

The GPIO signals can be configured as open drain (by PODR register), and in that case they also need a pull up resistor.

When GPIO signals are configured as I^2C, UART or SPI, the signals are configured as open drain in some cases. See the relevant chapters in the reference manual for additional details, and also the following sections in this document: **Section 11.4**, *UART* and **Section 11.5**, *I^2C*.

13 Disposition of Unused Signal Lines

Some applications may not use all available MSC815x/MSC825x interfaces. Refer to the Pin Mux Tool and the device technical data sheet for connectivity of unused signals.

14 Signals Connection Summary

Refer to the technical data sheet for a s summary of the recommended signals connection.

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