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SDRAM Support on the StarCore™-Based MSC8122 DSP

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The limitations of an SDRAM machine are not on the total memory it can support but rather on the type and size of the SDRAM device. This application note describes how to support various sizes of SDRAM on the Freescale MSC8122 DSP. It also describes the SDRAM settings required for the MSC8122 to access external memory at 133 MHz and 166 MHz on the MSC8122ADS board.[1]

CONTENTS

1. See the section on the SDRAM machine in the Memory Controller chapter of the *MSC8122 Reference Manual*.

1 MSC8122 SDRAM Capabilities

The MSC8122 provides only one SDRAM machine for the 60x system bus. However, multiple chip selects ($\overline{CS}$) can be programmed to support multiple SDRAM devices. There is no limitation on the number of chip selects that can be programmed for SDRAM. The $\overline{CS[1–7]}$ signal pins can be programmed to support SDRAM, assuming $\overline{CS0}$ is reserved for the general-purpose chip-select machine (GPCM) to connect to Flash memory. The *MSC8122 Reference Manual* shows an example of a multiple chip-select SDRAM configuration. If multiple chip-selects are configured to support SDRAM on a single bus, each SDRAM device should have the same port size and timing parameters. All option registers (OR*x*) for the SDRAM chip selects should be programmed exactly the same way. All the chip selects on the 60x system bus share the same 60x SDRAM mode register (PSDMR) for initialization, the 60x bus-assigned SDRAM refresh timer register (PSRT), and the memory refresh timer prescaler register (MPTPR) for refresh. The memory controller supplies auto refresh (CBR) to SDRAM according to the time interval specified in PSRT and MPTPR as follows:

Equation 1

$$Refresh\ Period = \frac{(PSRT + 1) \times (MPTPR[PTP] + 1)}{Bus\ Frequency}$$

Equation 1 represents the time period between refreshes. When the refresh timer expires, the memory controller requests the bus. If the request is granted, it issues a CBR to each chip select. Each CBR is separated by one clock. **Figure 1** shows a refresh timing diagram for multiple chip selects.

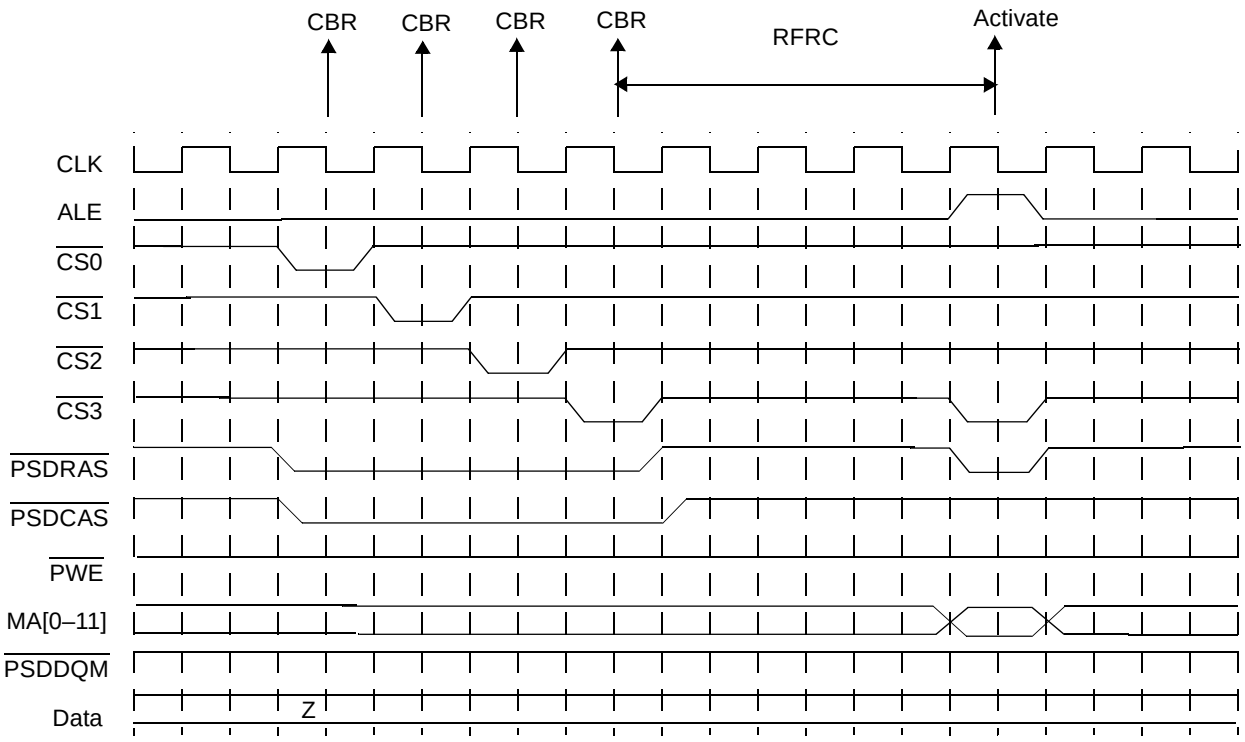

Figure 1. SDRAM Bank-Staggered CBR Refresh Timing

During a memory transaction on the bus, the memory controller compares the memory address with the address information of each memory bank, which is programmed through the BR*x* and OR*x* registers. If there is a match with a memory bank dedicated to SDRAM, the memory controller requests service from the 60x system bus SDRAM machine. Although multiple chip selects (memory banks) can be programmed for SDRAM, only one chip select is active at any time, so multiple chip selects can share the same SDRAM machine.

Table 1 is based on the SDRAM data sheet supplied by Micron. The maximum amount of SDRAM supported by the MSC8122 SDRAM controller varies, depending on how the memory device is connected to the MSC8122.

Table 1. Micron SDRAM Devices

SDRAM Device	64 Mb			128 Mb			256 Mb			512 Mb		
I/O Port Size	8 Bits	16 Bits	32 Bits	8 Bits	16 Bits	32 Bits	8 Bits	16 Bits	32 Bits	8 Bits	16 Bits	32 Bits
Bank	4	4	4	4	4	4	4	4	4	4	4	4
Row	12	12	11	12	12	12	13	13	12	13	13	13
Column	9	8	8	10	9	8	10	9	9	11	10	9

The data port size is programmable, but the examples in this application note use all 64 bits of the 60x bus. The 64-bit port size requires eight SDRAM devices (with 8-bit I/O ports) connected in parallel to a single chip select. If 128 Mbit devices are used, one chip select provides 128 Mb device × 8 devices = 128 MB. If eight chip selects are programmed for SDRAM use, the result is 128 MB × 8 = 1 GB. If 256 Mb SDRAM devices are used (page-based interleaving), the total available memory is 2 GB.

Although there is no technical difficulty in supporting multiple chip-select configurations, in practice you can choose to maximize the amount of SDRAM assigned to each chip select. For example, you can connect eight x8 SDRAM devices to the MSC8122. When maximizing the amount of SDRAM assigned to each chip select, you must consider the output load (capacitance) on the MSC8122 pins. The AC timing specifications for the memory interface in the *MSC8122 Data Sheet* are defined for a specific load. The frequency of the interface is affected if there are high loads on the pins.

2 MSC8122 SDRAM Machine Limitations

The limitations of the MSC8122 SDRAM machine are due to constraints on the interleaving modes and the inflexibility of bank select signal multiplexing.

2.1 Interleaving Modes

In bank-based interleaving mode, the maximum size of one chip select is 128 MB. In page-based interleaving mode during the address bus partition, the address lines for bank selects cannot be less than A21 (in relation to big endianness). For example, in **Example 12-1 o**f the *MSC8122 Reference Manual*, the address lines A[22–24] cannot be used for the bank select signal.

2.2 Maximum Row Number

PSDMR[BSMA] is used to multiplex the bank select address. The BSMA field and corresponding multiplexed address are as follows:

```
000 A12-A14
001 A13-A15
...
111 A19-A21
```

The highest address pins with which the bank selects can be multiplexed are A[12–14], which limits the pins for the row address to A[15–31]. For a 64-bit port, A[29–31] are not connected. The maximum row is A[15–28] (14 rows). For smaller port sizes, the row number can be greater. For example, in a 32-bit port, only A[30–31] are not connected, so A[15–29] can be used for the row address (15 rows). The Micron 256 Mb device has only 13 rows. The SDRAM machine is not used with the local bus of the MSC8122.

2.2.1 Inflexible Multiplexing Bank Select Signals

Normally, bank selects are multiplexed to the address pins immediately above the row address. For page-based interleaving, the bank signals can be multiplexed to the higher-order address pins to leave room for future upgrades. For example, you can multiplex the bank select signals to A[15–16], leaving A17 to connect to the address pin for a larger memory size. Bank-based interleaving has no such flexibility. If you attempt to multiplex the bank select signals to A[14–15], an incorrect value is multiplexed. Namely, the logical address A[5–6] is multiplexed instead of the correct A[6–7] value.

You can also use dedicated BNKSEL pins instead of multiplexing bank select signals to the higher-order address pins. For page-based interleaving, the value of SDMR[BSMA] has no effect. The correct bank select signals are always output to the BNKSEL*x*. However, for bank-based interleaving, BNKSEL*x* are correct only if BSMA is programmed so that the bank select signals are multiplexed to the address pins immediately above the row address.

2.2.2 Analysis of Row Address Multiplexing

The PSDMR[SDAM] field is used to multiplex the row address during an ACTIVATE command. It applies to both page- and bank-based interleaving. For two banks, one address pin is assigned for bank select, two address pins are assigned for four banks, and three address pins are assigned for eight banks. The following analysis is based on four banks (because all Micron SDRAMs have four banks) and a 60x system bus. The analysis uses PSDMR[SDAM] = 101 See **Table 2**.

Table 2. SDRAM Address Multiplexing when PSDMR[SDAM] = 101

Physical Address	A12	A13	A14	A15	…	A28	A29	A30	A31
Logical Address	—	A0	A1	A2	…	A15	A16	A17	A18

For both page-based and bank-based interleaving modes, the row address is determined as follows. For a port size of 64 bits, A[29–31] are not connected. If the bank-select signals are multiplexed to the highest possible physical address A[12–14] (to maximize the row number), the physical row address is A[15–28], which corresponds to logical address A[2–15]. Thus, the maximum row number is 14.

For page-based interleaving, the logical address can only be partitioned as shown in **Table 3** because the logical row address is determined to be A[2–15]. The logical address A[16–17] partition is for bank selects. The logical address partition for the column address is A[18–31]. Because the port size is 64 bits, A[29–31] are not connected. Thus, only A[18–28] are used for the logical column address.

Table 3. Logical Address Partition for Page-Based Interleaving

Address Partition	Row			Bank		Column			NC
Logical Address	A2	…	A15	A16	A17	A18	…	A28	A[29–31]

For bank-based interleaving, the bank selects are of a higher order than the row address and are partitioned as shown in **Table 4**. The logical address partition for the column address is A[16–31], but because the port size is 64 bits, only A[16–28] are used for the logical column address. A[29–31] are not connected.

Table 4. Logical Address Partition for Bank-based Interleaving

Address Partition	Bank		Row			Column			NC
Logical Address	A0	A1	A2	…	A15	A16	…	A28	A[29–31]

Table 5 summarizes the port size and column and row number for each SDAM configuration. The row number is the maximum allowed for that configuration. The column number is exact for that SDAM configuration. Note that **Table 5** and **Table 6** refer only to 4-bank SDRAM devices. When SDAM = 101 for page-based interleaving and when SDAM = 011, 100, 101 for bank-based interleaving, the column number is more than 10. The MSC8122 can use these values but requires an external multiplexer.

Table 5. Page-Based Interleaving (60x Bus, 4 Banks)

SDAM	Port Size in Bits			
	64	32	16	8
000	6 col × 14 row	6 col × 15 row	6 col × 16 row	6 col × 17 row
001	7 col × 14 row	7 col × 15 row	7 col × 16 row	7 col × 17 row
010	8 col × 14 row	8 col × 15 row	8 col × 16 row	8 col × 17 row
011	9 col × 14 row	9 col × 15 row	9 col × 16 row	9 col × 17 row
100	10 col× 14 row	10 col × 15 row	10 col × 16 row	10 col × 17 row
101	11 col × 14 row	11 col × 15 row	11 col × 16 row	11 col × 17 row

Table 6. Bank-Based Interleaving (60x Bus, 4 Banks)

SDAM	Port Size in Bits			
	64	32	16	8
000	8 col × 14 row	8 col × 15 row	8 col × 16 row	8 col × 17 row
001	9 col × 14 row	9 col × 15 row	9 col × 16 row	9 col × 17 row
010	10 col × 14 row	10 col × 15 row	10 col × 16 row	10 col × 17 row
011	11 col × 14 row	11 col × 15 row	11 col × 16 row	11 col × 17 row
100	12 col × 14 row	12 col × 15 row	12 col × 16 row	12 col × 17 row
101	13 col × 14 row	13 col × 15 row	13 col × 16 row	13 col × 17 row

3 Example SDRAM Sizes

This section shows examples of specific modules.

3.1 256 MB SDRAM

Figure 2 shows an SDRAM of 256 MB.

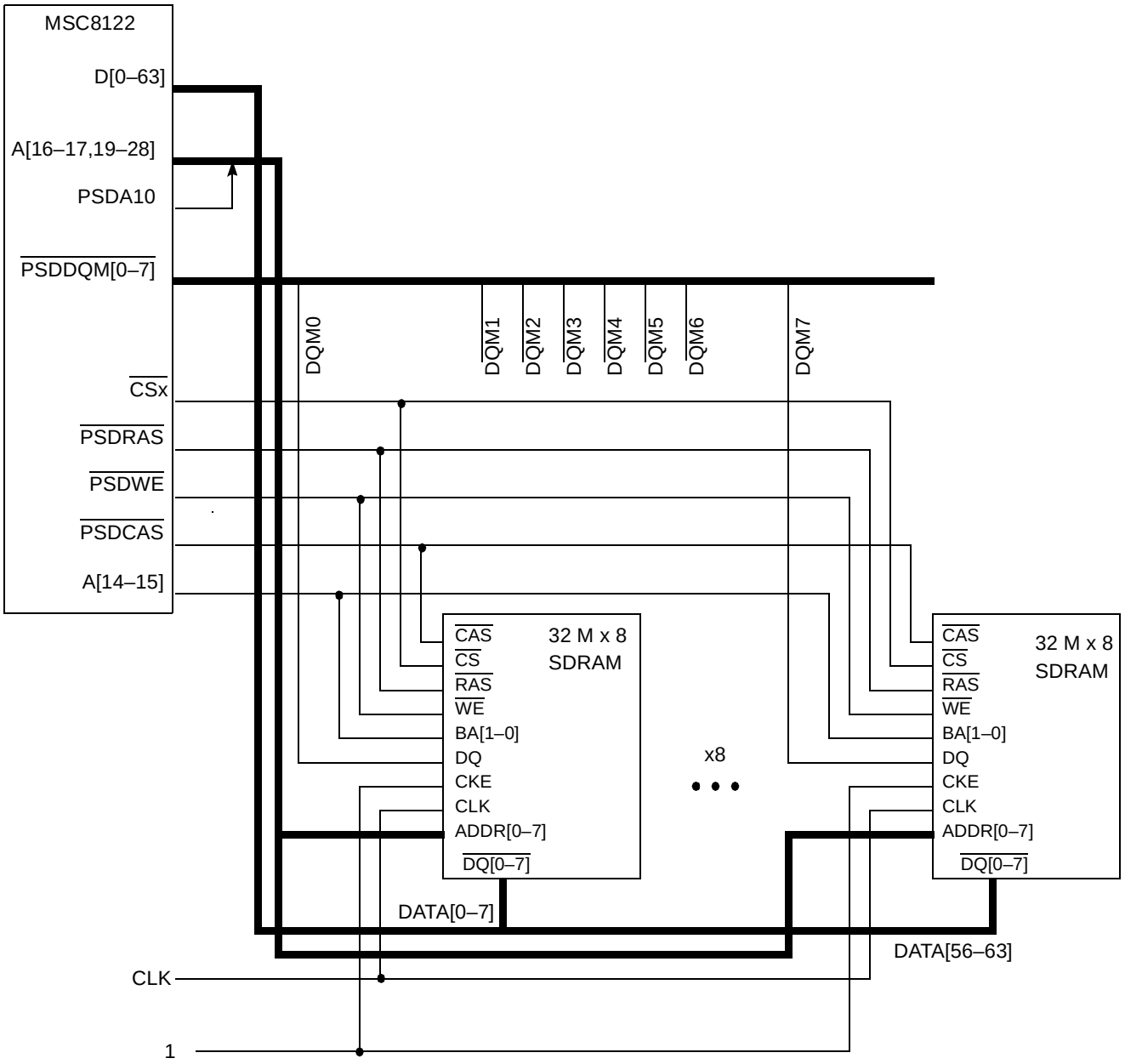

Figure 2. 256 MB SDRAM

Consider the following SDRAM organization:

- The 64-bit port size is organized as $8 \times 8 \times 32$ Mbit.
- Each device has four internal banks, 13 row address lines, and 10 column address lines.

The address bus is partitioned as shown in **Table 7**.

Table 7. 60x Address Bus Partition

A[0–3]	A[4–16]	A[17–18]	A[19–28]	A[29–31]
MSB of start address	Row	Bank select	Column	LSB

The following parameters are extracted:

- PSDMR[PBI] = 1, page-based interleaving
- BPD = 01, four internal banks
- ROWST = 100, row starts at A4
- NUMR = 100, 13 row lines

During an ACTIVATE command, the SDRAM address port is set as in **Table 8**.

Table 8. SDRAM Device Address Port During ACTIVATE Command

A[0–13]	A[14–15]	A[16–28]	A[29–31]
—	Internal bank-select A[17–18]	Row A[4–16]	No connect

To multiplex A[4–16] over A[16–28], set PSDMR[SDAM] to 100. Because the internal bank selects are multiplexed over A[14–15], PSDMR[BSMA] must be set to 001. Only the lower two bank select lines are used. Refer to the example of SDRAM address multiplexing in the Memory Controller chapter of the *MSC8122 Reference Manual*. **Table 9** shows the address port configuration during a READ/WRITE command.

Table 9. SDRAM Device Address Port During READ/WRITE Command

A[0–13]	A[14–15]	A16, A17	A18	A[19–28]	A[29–31]
—	Internal bank select	Any	AP	Column	No connect

Because AP alternates with row line A6, set PSDMR[SDA10] to 100 to output A6 on the SDA10 line during the ACTIVATE command and AP during READ/WRITE and CBR commands. SDA10 connects to the appropriate SDRAM address bit, A10. **Table 10** shows the register configuration. PSRT and MPTPR, which should be programmed according to the specific refresh requirements of the device, are not shown here.

Table 10. Register Setting for 256 MB SDRAMs

Register	Field	Value
BR*x*	BA	Base address
	PS	00 = 64-bit port size
	MS	010 = SDRAM-60x bus
	V	1
OR*x*	SDAM	0b1111 00000000
	LSDAM	0b00000
	BPD	0b01
	ROWST	0b0100
	NUMR	0b100

Table 10. Register Setting for 256 MB SDRAMs (Continued)

Register	Field	Value
PSDMR	PBI	0b1
	RFEN	0b1
	OP	0b000
	SDAM	0b100
	BSMA	0b001
	SDA10	0b100
	RFRC	From device data sheet
	PRETOACT	From device data sheet
	ACTTOROW	From device data sheet
	BL	0b0
	LDOTOPRE	From device data sheet
	WRC	From device data sheet
	CL	From device data sheet

3.2 512 MB SDRAM Module

Figure 3 is from Micron. The configuration shown here matches the previous example but uses two chip selects.

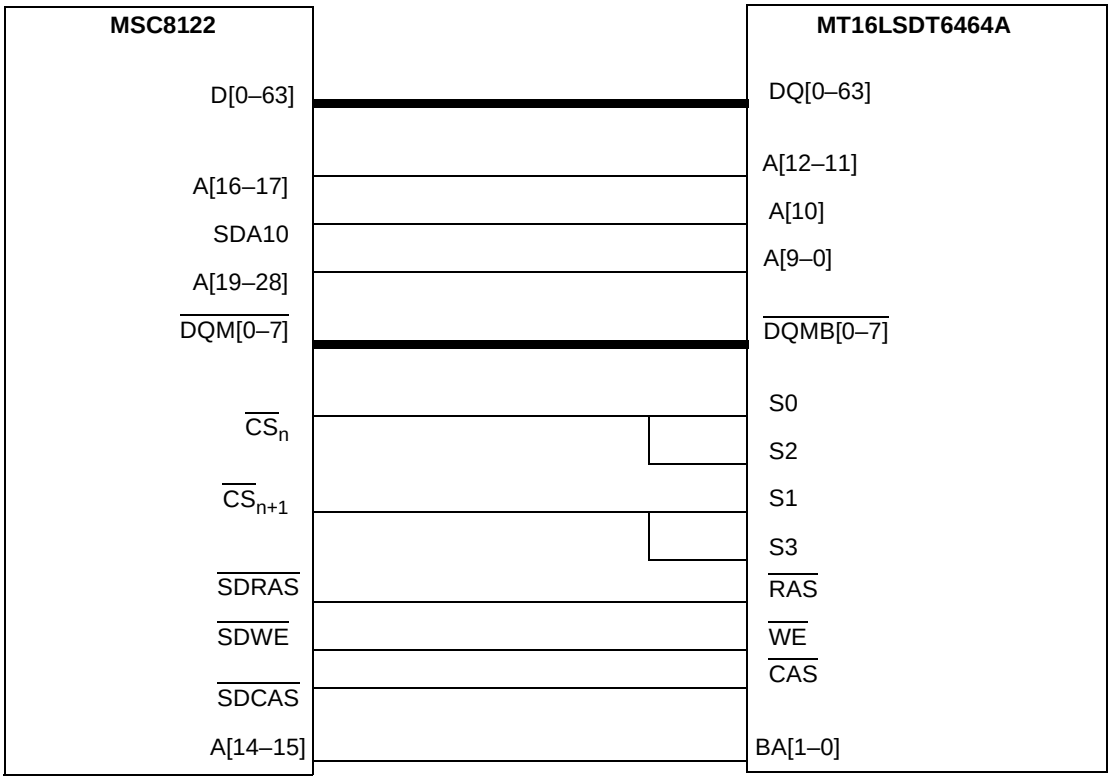

Figure 3. 512 MB SDRAM Configuration Using an MT16LSDT6464A

3.3 1 GB SDRAM Memory Module

This example shown in **Figure 4** uses an MT36LSDF12872G from Micron.

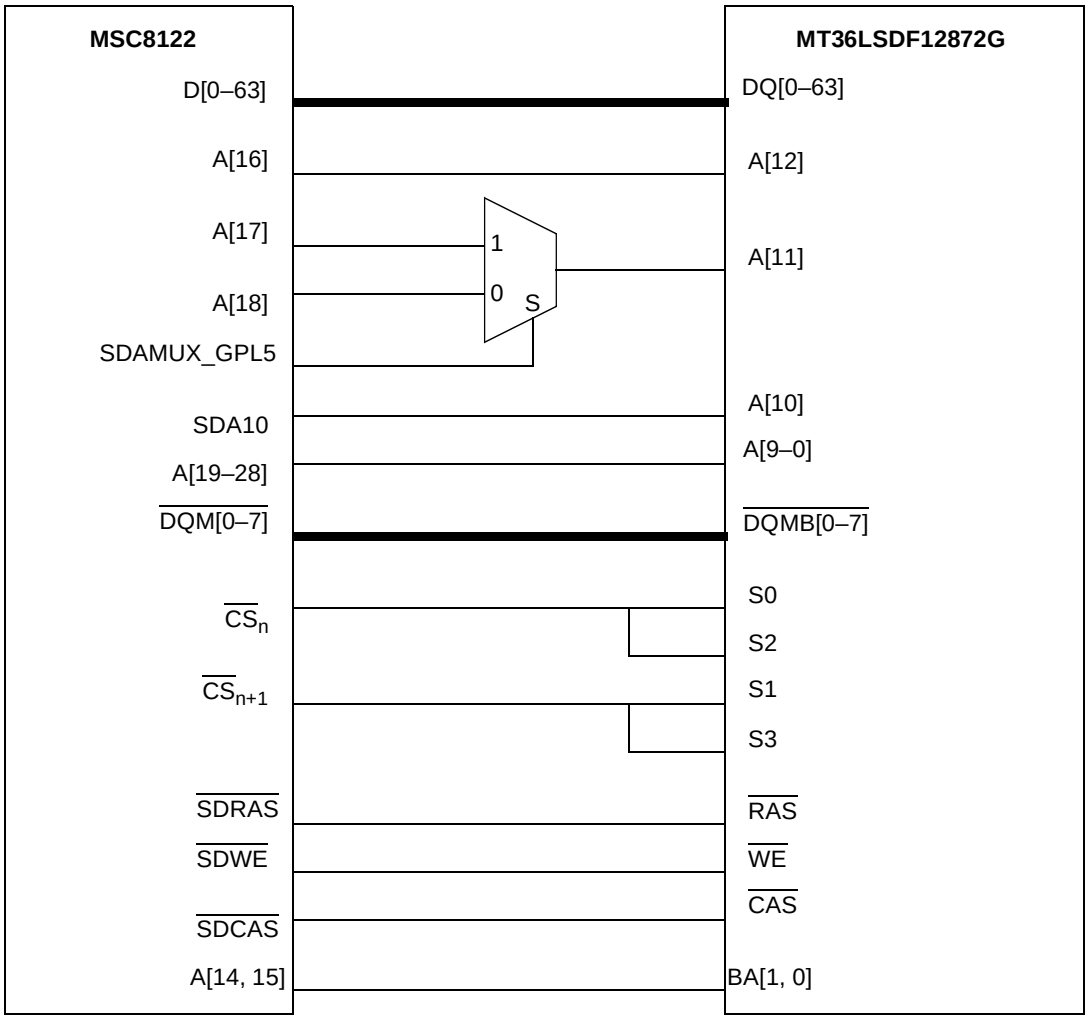

Figure 4. MT36LSDF12872G Example

In this SDRAM organization:

- The 64-bit port size is 16 × 4 × 64 Mb × 2 chip select lines.
- Each device has 4 internal banks, 13 row address lines, and 11 column address lines.

The address bus is partitioned as shown in **Table 11**.

Table 11. 60x Address Bus Partition

A[0–2]	A[3–15]	A[16–17]	A[18–28]	A[29–31]
MSB of start address	Row	Bank select	Column	LSB

The following parameters can be extracted:

- PSDMR[PBI] = 1, page-based interleaving
- BPD = 01, four internal banks
- ROWST = 011, row starts at A3
- NUMR = 100, 13 row lines

For an ACTIVATE command, the SDRAM address port is set as shown in **Table 12**.

Table 12. SDRAM Device Address Port During ACTIVATE Command

A[0–13]	A[14–15]	A[16–28]	A[29–31]
—	Internal bank select (A[16–17])	Row (A[3–15])	No connect

To multiplex A[3–15] over A[16–28], set PSDMR[SDAM] to 101. Because the internal bank selects are multiplexed over A[14–15], PSDMR[BSMA] must be set to 001. Only the lower two bank select lines are used. For details on SDRAM address multiplexing, refer to the *MSC8122 Reference Manual*. **Table 13** shows the address port settings for a READ/WRITE command.

Table 13. SDRAM Device Address Port During READ/WRITE Command

A[0–13]	A[14–15]	A16	A17	A18	A[19–28]	A[29–31]
—	Internal bank select	Any	Column	AP	Column	No connect

Because AP alternates with the MSB of the row line A5, set PSDMR[SDA10] to 101. This outputs A5 on the SDA10 line during the ACTIVATE command and on AP during the READ/WRITE and CBR commands. SDA10 connects to the appropriate SDRAM address bit, A10. An external multiplex is needed for proper generation of A11. **Table 14** shows the register configuration. PSRT and MPTPR, which should be programmed according to the refresh requirements of the specific device, are not shown here.

Table 14. Register Settings for 1 GB SDRAMs

Register	Field	Value
BR*x*	BA	Base address
	PS	00 = 64-bit port size
	MS	010 = SDRAM-60x bus
	V	0b1
OR*x*	SDAM	0b111000000000
	LSDAM	0b00000
	BPD	0b01
	ROWST	0b0011
	NUMR	0b100

Table 14. Register Settings for 1 GB SDRAMs (Continued)

Register	Field	Value
PSDMR	PBI	0b1
	RFEN	0b1
	OP	0b000
	SDAM	0b101
	BSMA	0b001
	SDA10	0b101
	RFRC	From device data sheet
	PRETOACT	From device data sheet
	ACTTOROW	From device data sheet
	BL	0b0
	LDOTOPRE	From device data sheet
	WRC	From device data sheet
	CL	From device data sheet

4 MSC8122ADS Settings for Selected Frequencies

The MSC8122 device can operate in various frequency configurations, ranging from a maximum core frequency of 300 MHz with a 100 MHz system bus to a 500 MHz core frequency with a 166 MHz system bus.

CodeWarrior for StarCore 2.6 includes configuration files for the MSC8122 DSP to initialize its memory controller and control registers immediately after reset. For the default board configuration, which specifies a 32-bit DSI and boots via the DSI, the configuration files reside at the following location:

`C:\Program Files\Metrowerks\CodeWarrior\StarCore_Support\Initialization_Files\RegisterConfigFiles\MSC8122ADS\Dsi32_DsiBoot.`

Core 0 runs the `8122ADS_DSI32_Slave_Init.cfg` file after the MSC8101 host resets it. The file contains a `bank2_init` SDRAM section in which the SDRAM interface is programmed. This section of the configuration file must be changed when the bus operates at 133 MHz or 166 MHz. The default bus operating speed is 100 MHz.

Section 4.1 describes the physical connection to SDRAM on the MSC8122ADS for a 64-bit port size. **Section 4.3-Section 4.5** include the changes required in the ADS configuration files to operate the interface at 100 MHz, 133 MHz, and 166 MHz.

4.1 MSC8122ADS Connections

Figure 5 is from Micron. The multiplex on the address lines enables the SDRAMs for 32-bit or 64-bit port sizes. Refer to the *MSC8122/26ADS Reference Manual* for details on the connections.

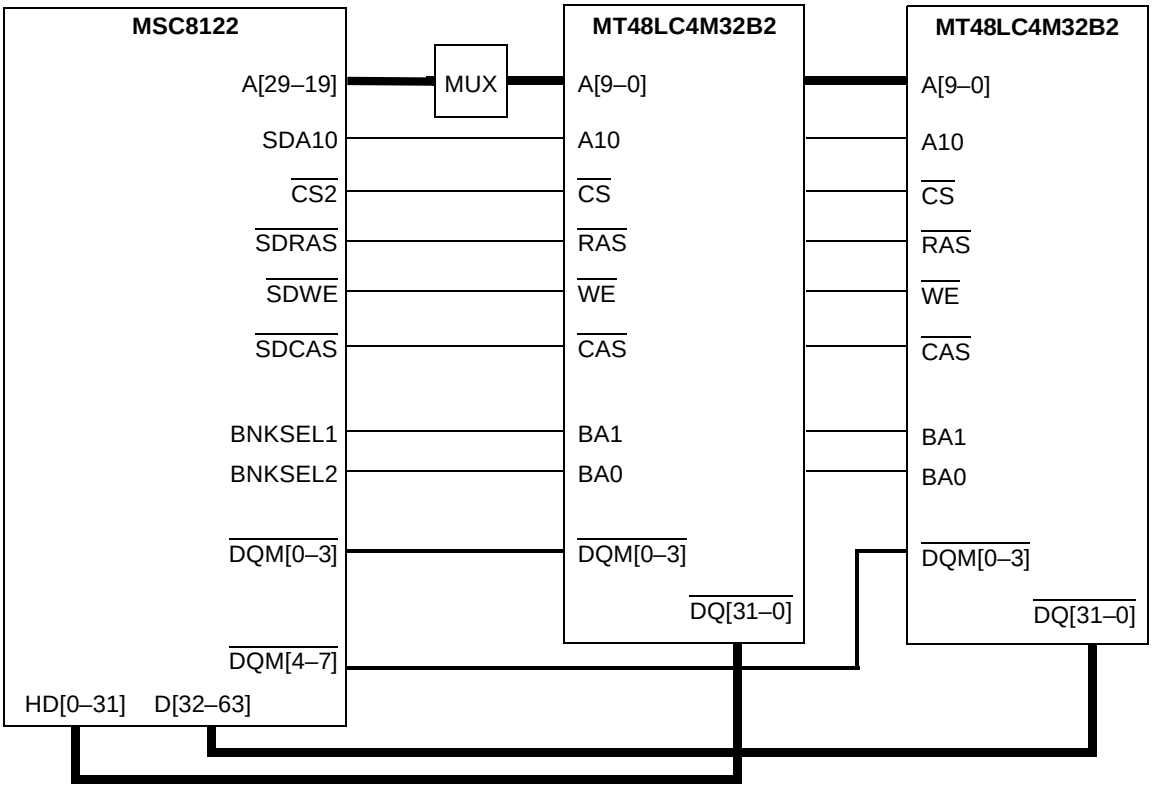

Figure 5. 16 MB SDRAM Configuration with MT48LC4M32B2 on the MSC8122ADS

Consider the following SDRAM organization:

- The 64-bit port size is organized as $2 \times 32 \times 4$Mbit.
- Each device has four internal banks, 12 row address lines, and 8 column address lines.

The address bus is partitioned as shown in **Table 15**.

Table 15. 60x Address Bus Partition

A[0–6]	A[7–8]	A[9–20]	A[21–28]	A[29–31]
MSB of start address	Bank select	Row	Column	LSB

The following parameters are extracted:

- PSDMR[PBI] = 0, bank-based interleaving
- BPD = 01, four internal banks
- ROWST = 0110, row starts at A9
- NUMR = 011, 12 row lines

During an ACTIVATE command, the SDRAM address port is set as shown in **Table 16**.

Table 16. SDRAM Device Address Port During ACTIVATE Command

A[0–15]	A[15–16]	A[17–28]	A[29–31]
—	Internal bank-select A[7–8]	Row A[9–20]	No connect

To multiplex A[9–20] over A[16–28], set PSDMR[SDAM] to 000. Because the internal bank selects are multiplexed over A[15–16], PSDMR[BSMA] must be set to 010. Only the lower two bank select lines are used. **Table 17** shows the address port configuration during a READ/WRITE command.

Table 17. SDRAM Device Address Port During READ/WRITE Command

A[0–13]	A[15–16]	A17	A18	A19, A20	A[21–28]	A[29–31]
—	Internal bank select	Any	AP	Any	Column	No connect

Because AP alternates with row line A10, set PSDMR[SDA10] to 010., which outputs A10 on the SDA10 line during the ACTIVATE command and on AP during the READ/WRITE and CBR commands. SDA10 connects to the appropriate SDRAM address bit, A10. **Table 18** shows the register configuration for the default configuration file included with the CodeWarrior tools. The PSDMR settings for the 133 MHz and 166 MHz configurations are different. For refresh, the memory controller must supply auto refresh (CBR) to SDRAM within each 15.625 µs. The refresh period is calculated according to the interval specified in PSRT and MPTPR, as follows, when the bus runs at 100 MHz (see **Equation 1**):

Equation 2

$$Refresh\ Period = \frac{(24 + 1)\ x\ (61 + 1)}{100MHz} = 15.500ms$$

Table 18. Register Setting for 32 MB SDRAM on the MSC8122ADS

Register	Field	Value
BR*x*	BA	0b00100000000000000
	PS	0b00 = 64-bit port size
	MS	0b010 = SDRAM-60x bus
	DR	0b1
	V	0b1
OR*x*	SDAM	0b11111110000
	LSDAM	0b00000
	BPD	0b01
	ROWST	0b0110
	NUMR	0b011

Table 18. Register Setting for 32 MB SDRAM on the MSC8122ADS (Continued)

Register	Field	Value
PSDMR	PBI	0 = bank-based
	RFEN	1 = refresh enabled
	OP	0b000
	SDAM	0b000
	BSMA	0b010
	SDA10	0b010
	RFRC	0b110 = 8 clock recovery
	PRETOACT	0b010
	ACTTOROW	0b010
	BL	0b0 = burst length 4
	LDOTOPRE	0b01 = –1 clock cycle
	WRC	0b10 = 2 clock cycles
	CL	0b11 = 3

4.2 Types of MSC8122ADS Boards

There are three types of MSC8122ADS boards:

- *Type 1*. Standard MSC8122ADS for up to 133 MHz operation (most common).
- *Type 2*. Updated MSC8122ADS for 166 MHz 60x bus operation (low availability).
- *Type 3*. New MSC8122ADS specifically for 166 MHz operation. This board is in the design phase.

For MSC8122ADS boards operating with a 500 MHz MSC8122 device (Type 2 and Type 3 boards), different SDRAM devices are used: MT48LC2M32B2-5. They are half the size (16 MB total) and operate at a higher speed grade than the default SDRAM devices on the Type 1 boards described in **Section 4.1**. With the higher speed grade, they can operate with the MSC8122 166 MHz 60x bus. Since the size is smaller, the OR2 mask has a value of 0xFF00 for the 133 MHz and 166 MHz configuration settings.

To verify which SDRAM configuration is used on your board, you can check the reference manual for your board or look on the bottom side of your MSC8122ADS and check the part number for the SDRAM bank closest to the MSC8122 socket. If the part number ends in -6, you should use the default configuration settings in **Section 4.3**. These settings are also the default settings used in *CodeWarrior 2.6 for StarCore* stationaries. Otherwise, use the SDRAM initialization settings in **Section 4.4** or **Section 4.5**, depending on the clock mode of the MSC8122 device.

4.3 Default SDRAM Configuration File Settings

```
################################################
######### bank2_init SDRAM ####################
################################################
#OR2
writemem32 0x14710114 0xff002ce0
#BR2
writemem32 0x14710110 0x20000041
# PSDMR
writemem32 0x14710190 0x284b2463
writemem32 0x20000020 0x0
```

```
writememl32 0x14710190 0x084b2463
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x14710190 0x184b2463
writememl32 0x20000190 0x0
# PSDMR
writememl32 0x14710190 0x404b2463
# PSRT
writemem8 0x1471019c 0x18
# MPTPR
writemem16 0x14710184 0x3d00
```

4.4 133 MHz Configuration File SDRAM Settings

```
################################################
######### bank2_init SDRAM ####################
################################################
#OR2
writememl32 0x14710114 0xff0030a0
#BR2
writememl32 0x14710110 0x20000043
# PSDMR
writememl32 0x14710190 0x286b24a3
writememl32 0x20000020 0x0
writememl32 0x14710190 0x086b24a3
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x20000000 0x0
writememl32 0x14710190 0x186b24a3
writememl32 0x20000190 0x0
# PSDMR
writememl32 0x14710190 0x404b24a3
# PSRT
writemem8 0x1471019c 0xff
# MPTPR
writemem16 0x14710184 0x0700
```

4.5 166 MHz Configuration File SDRAM Settings

```
################################################
######### bank2_init SDRAM ####################
################################################
#OR2
writememl32 0x14710114 0xff0030a0
```

```
#BR2
writememm32 0x14710110 0x20000043
# PSDMR
writememm32 0x14710190 0x286bb6a3
writememm32 0x20000020 0x0
writememm32 0x14710190 0x086bb6a3
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x20000000 0x0
writememm32 0x14710190 0x186bb6a3
writememm32 0x20000190 0x0
# PSDMR
writememm32 0x14710190 0x404bb6a3
# PSRT
writememm8 0x1471019c 0xff
# MPTPR
writememm16 0x14710184 0x0700
```

4.5.1 Differences Between Configuration File Settings

The only difference between the 133 MHz and 166 MHz SDRAM interface settings is the value of the MSC8122 PSDMR register bits 14–25. They differ from the default configuration file settings in the PSDMR bits for LDOTOPRE and CL. **Table 19** shows the register setting differences and their meanings.

Table 19. Configuration File Differences

	100 MHz	Meaning	133 MHz	Meaning	166 MHz	Meaning
PSDMR[RFRC]	110	8 clock refresh recovery	110	8 clock refresh recovery	111	16 clock refresh recovery
PSDMR[PRETOACT]	010	2 wait states for refresh after precharge	010	2 wait states for refresh after precharge	011	3 wait states for refresh after precharge
PSDMR[ACTTORW]	010	2 clock cycle interval between ACTIVATE and READ/WRITE	010	2 clock cycle interval between ACTIVATE and READ/WRITE	011	3 clock cycle interval between ACTIVATE and READ/WRITE
PSDMR[LDOTOPRE]	01	–1 clock cycles	10	–2 clock cycles	10	–2 clock cycles

5 SDRAM Interface Throughput With DMA

The configuration file settings in **Section 4**, *MSC8122ADS Settings for Selected Frequencies*, on page 11 were used to measure throughput performance of a dual-access DMA operation on the MSC8122. In addition, the technique of DMA-interleaving combined with SDRAM bank-based interleaving was used as described in AN2704, *Using DMA-SDRAM to Optimize Bandwidth on the StarCore MSC8102 and MSC812x Devices*. **Table 20** shows the results. The 150 MHz bus throughput is included for reference.

Table 20. DMA Throughput from M1 Memory to SDRAM

	Throughput (MB/s)				
	Transfer Size (Bytes)	**100 MHz**	**133 MHz**	**150 MHz**	**166 MHz**
Read	2048	479	601	676	751
Write	2048	605	817	919	1021

NOTES:

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