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Application Note

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Migration from MPC8540 or MPC8541E to MPC8548E

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The MPC8548E family of microprocessors is part of the Freescale PowerQUICC™ III family of quad integrated communications controller (PowerQUICC) devices. The MPC8548E microprocessor is based on the Freescale 90 nanometer (nm) silicon-on-insulator (SOI) copper interconnect process technology and delivers higher performance with lower power dissipation. The MPC8548E offers several more higher specification system blocks than the MPC8540 or MPC8541E:

- 1.33 GHz core
- 512 KB L2 cache
- integrated security engine
- 4 Gigabit Ethernet interfaces
- 64-bit DDR1/2 scaling to 533 MHz data rate
- dual 32-bit PCI/64-bit PCI-X
- 4-bit Serial RapidIO and 4-bit PCI Express (or single 8-bit PCI Express 1.0a), and local bus I/O interfaces.

This document compares the MPC8548E and MPC8540 or MPC8541E and examines how the additional functionality of the MPC8541E affects the migration from the MPC8540 or MPC8541E to MPC8548E.

Contents

1 Feature Comparisons

Table 1 summarizes the features of the MPC8548E, MPC8540, and MPC8541E, and the remainder of this section considers each feature in more detail.

Table 1. Feature Comparisons

Features	MPC8548E	MPC8540	MPC8541E
CPU	e500v2	e500v1	
The size of L2 look-aside cache/SDRAM	512K	256K	
DDR controller	Refer to Section 1.2, “DDR Controller”		
TSEC	Refer to Section 1.3, “Enhanced Three-Speed Ethernet Controllers”		
Power supply voltages	Refer to Section 1.7, “Power Supply Voltages”		
Clocking and clocking ratio	Refer to Section 1.8, “Clock and Clock Ratio”		
Pin migration	Refer to Section 1.9, “Pin Migration”		
Software migration	Refer to Section 2, “Software Migration”		
PCI/PCI-X	2 × 3-bit PCI(X) or 1 × 64-bit PCI(X)	One 32-/64-bit PCI/PCI-X	2 × 32-bit PCI or 1 × 64-bit PCI
Security engine	One integrated security engine (SEC 2.1), XOR acceleration	None	One integrated security engine (SEC 2.0)
High-speed interfaces	x8 PCI Express or x4 serial RapidIO and x4 PCI Express	One 8-bit parallel RapidIO	None
Communications processor module (CPM)	None	None	Yes. With dual 10/100 fast Ethernet controllers, I^2C controller and a serial peripheral interface (SPI)
I^2C	2	1	2

1.1 e500v2 Versus e500v1

The most significant enhancements to the MPC8548E e500v2 core are the 36-bit real addressing and the double-precision floating-point (DPFP) APU. For details, refer to the section titled, “e500v2 Differences,” in the *MPC8548 PowerQUICC™ III Integrated Communications Processor Family Reference Manual.* For details on the e500v2 core, refer to the *PowerPC™ e500 Core Family Reference Manual* (supports e500v1 and e500v2), which is available at the web site listed on the back cover of this manual.

1.2 DDR Controller

Table 2 lists the major feature differences between the MPC8548E DDR controller and the MPC8540 or MPC8541E DDR controller.

Table 2. DDR Controller Feature Differences

Features	MPC8548E DDR Controller	MPC8540 or MPC8541E DDR Controller
DDR and DDR2 support	Supports both DDR and DDR2 SDRAM with ECC	Supports DDR SDRAM with ECC
FCRAM1, FCRAM2 and low power DDR supports	Yes	No
Data rate	Up to 400 MHz data rate for DDR and 533 MHz data rate for DDR2	Up to 333 MHz data rate for DDR
Memory bank support	Four banks of memory supported, each up to 4 Gbytes, to a maximum of 16 Gbytes	Four banks of memory supported, each up to 1 Gbytes, to a maximum of 4 Gbytes
DRAM chip configurations	64 Mbits to 4 Gbits with x8/x16 data ports	64 Mbits to 1 Gbit with x8/x16 data ports
Page mode support	Up to 16 simultaneous open pages for DDR and up to 32 simultaneous open pages for DDR2	Up to 16 simultaneous open pages for DDR
On-die termination	Supported for DDR2	No
I/O voltage	2.5-V SSTL_2 compatible I/O for DDR; 1.8-V SSTL_1.8 for DDR2	2.5-V SSTL_2 compatible I/O for DDR
DDR clock control configuration	Source synchronous mode	Source synchronous mode and DLL mode (DLL mode applies to MPC8540 only)

The MPC8548E DDR controller supports automatic or software-based driver calibration which requires external precision resistors. It is source clocked, and there is no PLL or DLL. It allows better tracking across process variations in I/O drivers. The DDR controller also supports chip select interleaving, which effectively yields the performance of eight sub-banks in a single bank of memory. The MPC8548E DDR controller supports emergency self-refresh battery backup for storage applications. The IRQ_OUT signal can be enabled to put memories into self-refresh mode. External interrupt connected to power failure circuitry is routed to IRQ_OUT in PIC to trigger this mode.

1.3 Enhanced Three-Speed Ethernet Controllers

Table 3 compares the features of the enhanced three-speed Ethernet controllers (eTSECs) of the MPC8548E and the three-speed Ethernet controllers (TSECs) of the MPC8540 or MPC8541E.

Table 3. eTSEC and TSEC Comparisons

Features	eTSEC	TSEC
Number of TSECs	4 eTSEC controllers	2 TSEC controllers
Ethernet physical interface supports	GMII, RGMII, MII, TBI, RTBI	
	RMII	—
Full-duplex FIFO interface bypassing the Ethernet MAC	Yes	No
TCP/IP off-load	Yes	No
Quality of service support	Yes. Transmission up to eight queues; reception to up to eight physical queues	No

Table 3. eTSEC and TSEC Comparisons (continued)

Features	eTSEC	TSEC
Interrupt coalescing	Yes	Yes
VLAN tags and priority, VLAN insertion and deletion	Yes	No
Hash table	256 unicast/multicast or 512 multicast-only address	256 unicast/multicast address
Backward-compatibility with MPC8540/ MPC8560 (PowerQUICC III) TSEC	Yes	—

1.4 PCI/PCI-X

The MPC8548E has a 64-bit PCI/PCI-X controller and a second 32-bit PCI controller. Both are compatible with the *PCI Local Bus Specification*, Revision 2.2. The PCI-X interface is compatible with the PCI-X Addendum, Revision 1.0. Each controller can function as a host or agent bridge interface in either PCI mode. Due to pin multiplexing limitations, the PCI/PCI-X controller can operate in 64-bit mode or both interfaces can operate simultaneously in 32-bit mode. Both interfaces support 32- and 64-bit addressing.

The MPC8548E PCI1/PCI-X controller is the same as the PCI/X interface on the MPC8540, except that it may be asynchronous with respect to the SYSCLK. The PCI2 controller is mutually exclusive with the serial RapidIO interface. It is essentially the same as that of the MPC8541E and shares pins with the 64-bit PCI1. It may be asynchronous with respect to SYSCLK as well. Note that the PCI2 controller supports host mode and 32-bit mode only.

1.5 Security Engine

The MPC8548E integrated security engine (SEC 2.1) doubles the performance of the MPC8541E security engine (SEC 2.0). Following is a list of SEC 2.1 enhancements. Refer to the *MPC8548 PowerQUICC III™ Integrated Communications Processor Family Reference Manual* for details on these enhancements:

- Improved SSL support:
  - Single-pass SSL processing with four new descriptor types to support SSL with stream or block cipher, with or without HW HMAC checking.
  - SSL 3.0 MAC (message authentication code) through new bits in the MDEU mode register.
- Hardware ICV checking, which applies to AESU, MDEU, and KEU:
  - New bits in the mode registers to enable ICV checking.
  - New interrupt mask, status, and clear bits to control EU behavior on ICV mismatch.
  - New bits in the crypto channel to enable header write-back with ICV checking.
- XOR acceleration for RAID:
  - New mode bits in AESU to enable XOR processing.
  - New descriptor type to support XOR processing.
- Kasumi acceleration:
  - New to the SEC, but very similar to the KEU in the MPC185.
  - New mode bits in the KEU to support GEA-3, A5/3, and ICV checking.

- 36-bit addressing:
  - All pointers can be written as 36 bits.
  - Must enable 36-bit addresses in each channel via CCCR.

1.6 Global Utilities

In the MPC8548E, software can set $\overline{\text{HRESET\_REQ}}$ to implement reset control. For general-purpose I/O, eight dedicated general-purpose outputs (GPOUT[24:31]) are defined.

1.7 Power Supply Voltages

Table 4 compares the power supplies of the MPC8548E and MPC8540 or MPC8541E.

Table 4. Power Supply Voltage Comparisons

	MPC8548E	MPC8540 or MPC8541E
Core supply voltage	V_{DD} = 1.1 V	V_{DD} = 1.2 V
PLL supply voltage	AV_{DD} = 1.1 V	AVDD = 1.2 V
Power supply for the high-speed SerDes interface	XV_{DD} = 1.1 V SV_{DD} = 1.1 V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD} = 2.5 V for DDR GV_{DD} = 1.8 V for DDR2	GV_{DD} = 2.5 V
Three-speed Ethernet I/O voltage	LV_{DD} = 3.3 or 2.5 V for eTSEC1 and eTSEC2 TV_{DD} = 3.3 or 2.5 V for eTSEC3 and eTSEC4	LV_{DD} = 3.3 or 2.5 V for TSEC1 and TSEC2
PCI/PCI-X, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD} = 3.3 V	OV_{DD} = 3.3 V
Local bus I/O voltage	BV_{DD} = 3.3, 2.5, or 1.8 V	OV_{DD} = 3.3 V

1.8 Clock and Clock Ratio

Table 5 provides the clock range and clock ratio comparisons between the MPC8548E and MPC8540 or MPC8541E.

Table 5. Clock Range and the Clock Ratio Comparisons

	MPC8548E	MPC8540 or MPC8541E
Core frequency	533–1333 MHz	400–833 MHz
CCB frequency	266–533 MHz	200–333 MHz
DDR data rate	266–533 MHz	200–333 MHz
Local bus frequency	16.6–133 MHz	25–166 MHz
New clock ratio for e500v2 core to CCB added in MPC8548E	4:1, 9:2, 1:1, 3:2	—
New clock ratio for CCB to SYSCLK added in MPC8548E	20:1	—

1.9 Pin Migration

The MPC8540, MPC8541E, and MPC8548E microprocessors use the same 783-pin FC-PBGA package. There is no difference in the package type. However, there are differences in the signal pins.

1.9.1 Pin Compatibility

Because the MPC8548 has DDR2, PCI Express, serial Rapid I/O high-speed interfaces, and two additional eTSECs (eTSEC3/4), it is not pin-compatible with the MPC8540 or MPC8541E. The customer must redesign the PCB board when migrating from the MPC8540 or MPC8541E to MPC8540

1.9.2 PCI Pin Changes

The PCI interface on the MPC8548E and MPC8541E differs slightly from that on the MPC8540 because it can be configured as either one 64-bit interface or two 32-bit interfaces. On the MPC8540, there is only one PCI interface, which can be configured as either 32- or 64-bit. Table 6 illustrates these pin differences.

Table 6. MPC8540 or MPC8541E to MPC8548E PCI Pin Changes

Pin Assignment	MPC8540 Pin	MPC8541E Pin	MPC8548E Pin
PCI_AD[63:32] [1]	AA14, AB14, AC14, AD14, AE14, AF14, AG14, AH14, V15, W15, Y15, AA15, AB15, AC15, AD15, AG15, AH15, V16, W16, AB16, AC16, AD16, AE16, AF16, V17, W17, Y17, AA17, AB17, AE17, AF17, AF18	Same as MPC8540	AB14, AC15, AA15, Y16, W16, AB16, AC16, AA16, AE17, AA18, W18, AC17, AD16, AE16, Y17, AC18, AB18, AA19, AB19, AB21, AA20, AC20, AB20, AB22, AC22, AD21, AB23, AF23, AD23, AE23, AC23, AC24
PCI_AD[31:0]	AH6, AD7, AE7, AH7, AB8, AC8, AF8, AG8, AD9, AE9, AF9, AG9, AH9, W10, Y10, AA10, AE11, AF11, AG11, AH11, V12, W12, Y12, AB12, AD12, AE12, AG12, AH12, V13, Y13, AB13, AC13	Same as MPC8540	AH6, AE7, AF7, AG7, AH7, AF8, AH8, AE9, AH9,AC10, AB10, AD10, AG10, AA10, AH10, AA11, AB12, AE12, AG12, AH12, AB13, AA12, AC13, AE13, Y14, W13, AG13, V14, AH13, AC14, Y15, AB15
PCI_C_$\overline{\text{BE}}$[7:4] [2]	AG13, AH13, V14, W14	Same as MPC8540	AF15, AD14, AE15, AD15
PCI_C_$\overline{\text{BE}}$[3:0]	AH8, AB10, AD11, AC12	Same as MPC8540	AF9, AD11, Y12, Y13
PCI_PAR	AA11	AA11	AD12
PCI_PAR64 [3]	Y14	Y14	W15
$\overline{\text{PCI\_FRAME}}$	AC10	AC10	AE11
$\overline{\text{PCI\_TRDY}}$	AG10	AG10	AG11
$\overline{\text{PCI2\_TRDY}}$	—	AC19	AD27
$\overline{\text{PCI\_IRDY}}$	AD10	AD10	AF11
$\overline{\text{PCI2\_IRDY}}$	—	AD20	AD26
$\overline{\text{PCI\_STOP}}$	V11	V11	W12
$\overline{\text{PCI2\_STOP}}$	—	AC23	AF24

Table 6. MPC8540 or MPC8541E to MPC8548E PCI Pin Changes (continued)

Pin Assignment	MPC8540 Pin	MPC8541E Pin	MPC8548E Pin
PCI_DEVSEL	AH10	AH10	AH11
PCI_IDSEL	AA9	AA9	AG9
PCI_REQ64 [4]	AE13	AE13	AF14
PCI_ACK64 [5]	AD13	AD13	V15
PCI_PERR	W11	W11	AC12
PCI2_PERR	—	AC20	AD25
PCI_SERR	Y11	Y11	V13
PCI2_SERR	—	AE20	AD24
PCI_REQ[4:0]	AE5, AG4, AE4, AF3, AF5	AE5, AG4, AE4, AF3, AF5	AH2, AG4, AG3, AH4, AH3
PCI2_REQ[4:0]	—	AC21, AE22, AD22,AE21,AD21	AD28, AE27, W17, AF26, AH25
PCI_GNT[4:0]	AG6, AF6, AH5, AG5, AE6	AG6, AF6, AH5, AG5, AE6	AG6, AE6, AF5, AH5, AG5
PCI2_GNT[4:0]	—	AD19, AE19, AE18, AD18, AC18	AE26, AG24, AF25, AE25, AG25
PCI_IRDY	AD10	AD10	AF11
PCI1_CLK	—	AH25	AH26
PCI2_CLK	—	AH27	AE28

1 On the MPC8541E and MPC8548E, these pins are multiplexed with the functionality of PCI2 pins, PCI2_AD[31:0].
2 On the MPC8541E and MPC8548E, these pins are multiplexed with the functionality of PCI2 pins, PCI2_C_BE[3:0].
3 On the MPC8541E and MPC8548E, this pin is multiplexed with the functionality of the PCI2 pin, PCI2_PAR.
4 On the MPC8541E and MPC8548E, this pin is multiplexed with the functionality of the PCI2 pin, PCI2_FRAME.
5 On the MPC8541E and MPC8548E, this pin is multiplexed with the functionality of the PCI2 pin, PCI2_DEVSEL.

1.9.3 Enhanced Three-Speed Ethernet Controllers Pin Changes

Table 7 shows the differences between eTSEC1 on the MPC8548E and TSEC1 on the MPC8540 or MPC8541E.

Table 7. MPC8540 or MPC8541E to MPC8548E eTSEC1 Pin Changes

Signal	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC1_RXD[7:0]	D4, B4, D3, D5, B5, A5, F6, E6	R5, U1, R3, U2, V3, V1, T3, T2
TSEC1_TXD[7:0]	A6, F7, D7, C7, B7, A7, G8, E8	T10, V7, U10, U5, U4, V6, T5, T8
TSEC1_COL	G7	R4
TSEC1_CRS	C3	V5
TSEC1_GTX_CLK	B6	U7
TSEC1_RX_CLK	D6	U3
TSEC1_RX_DV	D2	V2
TSEC1_RX_ER	E5	T1

Table 7. MPC8540 or MPC8541E to MPC8548E eTSEC1 Pin Changes (continued)

Signal	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC1_TX_CLK	C6	T6
TSEC1_TX_EN	C8	U9
TSEC1_TX_ER	B8	T7

Table 8 highlights the pin differences between eTSEC2 on the MPC8548E and TSEC2 on the MPC8540 or MPC8541E.

Table 8. MPC8540 or MPC8541E to MPC8548E eTSEC2 Pin Changes

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC2_RXD[7:0]	F9, E9, C9, B9, A9, H9, G10, F10	P2, R2, N1, N2, P3, M2, M1, N3
TSEC2_TXD[7:0]	B10, A10, J10, K11, J11, H11, G11, E11	N9, N10, P8, N7, R9, N5, R8, N6
TSEC2_COL	F8	P1
TSEC2_CRS	D9	R6
TSEC2_GTX_CLK	C10	P6
TSEC2_RX_CLK	E10	N4
TSEC2_RX_DV	H8	P5
TSEC2_RX_ER	A8	R1
TSEC2_TX_CLK	D10	P10
TSEC2_TX_EN	B11	P7
TSEC2_TX_ER	D11	R10

Table 9 highlights the pin differences between eTSEC3 on the MPC8548E and TSEC3 on the MPC8540 or MPC8541E. As the MPC8540 or MPC8541E only has two TSECs, the eTSEC3 pins on the MPC8548E are no connects on the MPC8540 or MPC8541E.

Table 9. MPC8540 or MPC8541E TO MPC8548E eTSEC3 Pin Changes

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC3_RXD[7:0] [1]	—	AA1, Y3, AA2, AA4, Y1, W3, W5, W4
TSEC3_TXD[7:0] [1]	—	AB8, Y7, AA7, Y8, V8, W10, Y10, W7
TSEC3_COL [2]	—	Y5
TSEC3_CRS [2]	—	AA3
TSEC3_GTX_CLK	—	W8
TSEC3_RX_CLK	—	W2
TSEC3_RX_DV	—	W1
TSEC3_RX_ER	—	Y2
TSEC3_TX_CLK	—	V10

Table 9. MPC8540 or MPC8541E TO MPC8548E eTSEC3 Pin Changes (continued)

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC3_TX_EN	—	V9
TSEC3_TX_ER [2]	—	AB6

[1] The upper portion of this byte (that is, eTSEC4 xXD[7:4]) is multiplexed with the lower portion (that is, xXD[3:0]) of eTSEC4.

[2] Multiplexed signal with eTSEC4.

Table 10 highlights the pin differences between TSEC on the MPC8540 or MPC8541E and eTSEC on the MPC8548E. As the MPC8540 or MPC8541E only has two TSECs, the TSEC4 pins on the MPC8548E are no connects on the MPC8540 or MPC8541E.

Table 10. MPC8540 or MPC8541E to MPC8548E eTSEC4 Pin Changes

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
TSEC4_RXD[3:0] [1]	—	AB8, Y7, AA7, Y8
TSEC4_TXD[7:0] [1]	—	AA1, Y3, AA2, AA4
TSEC4_GTX_CLK	—	AA5
TSEC4_RX_CLK [1]	—	Y5
TSEC4_RX_DV [1]	—	AA3
TSEC4_TX_EN [1]	—	AB6

[1] Multiplexed signal with TSEC3.

Table 11 highlights the pin differences between the MPC8540 or MPC8541E and the MPC8548E on the Ethernet management pins and also the Gigabit reference clock.

Table 11. MPC8540 or MPC8541E to MPC8548E Ethernet Management Pin Changes

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
EC_MDC	F1	AB9
EC_MDIO	E1	AC8
EC_GTX_CLK125	E2	V11

1.9.4 DDR Pin Changes

The MPC8548E microprocessor contains a DDR2 controller as well as the DDR1 controller that is present on the MPC8540. This section discusses the pin differences in the DDR controller between the MPC8540 or MPC8541E and MPC8548E devices.

Table 12. DDR Pin Changes

Pin Assignment	MPC8540 or MPC8541E Pin	MPC8548E Pin
MDQ[0:63]	M26, L27, L22, K24, M24, M23, K27, K26, K22, J28, F26, E27, J26, J23, H26, G26, C26, E25, C24, E23, D26, C25, A24, D23, B23, F22, J21, G21, G22, D22, H21, E21, N18, J18, D18, L17, M18, L18, C18, A18, K17, K16, C16, B16, G17, L16, A16, L15, G15, E15, C14, K13, C15, D15, E14, D14, D13, E13, D12, A11, F13, H13, A13, B12	L18, J18, K14, L13, L19, M18, L15, L14, A17, B17, A13, B12, C18, B18, B13, A12, H18, F18, J14, F15, K19, J19, H16, K15, D17, G16, K13, D14, D18, F17, F14, E14, A7, A6, D5, A4, C8, D7, B5, B4, A2, B1, D1, E4, A3, B2, D2, E3, F3, G4, J5, K5, F6, G5, J6, K4, J1, K2, M5, M3, J3, J2, L1, M6
MECC[0:7]	N20, M20, L19, E19, C21, A21, G19, A19	H13, F13, F11, C11, J13, G13, D12, M12
MDM[0:8]	L24, H28, F24, L21, E18, E16, G14, B13, M19	M17, C16, K17, E16, B6, C4, H4, K1, E13
MDQS[0:8]	L26, J25, D25, A22, H18, F16, F14, C13, C20	M15, A16, G17, G14, A5, D3, H1, L2, C13
$\overline{\text{MDQS}}$[0:8]	—	L17, B16, J16, H14, C6, C2, H3, L4, D13
MA[0:15]	N19, B21, F21, K21, M21, C23, A23, B24, H23, G24, K19, B25, D27, J14, J13	A8, F9, D9, B9, A9, L10, M10, H10, K10, G10, B8, E10, B10, G6, A10, L11
MBA[0:2] [1]	B18, B19	F7, J7, M11
$\overline{\text{MWE}}$	D17	E7
$\overline{\text{MCAS}}$	J16	H7
$\overline{\text{MRAS}}$	F17	L8
MCKE[0:3] [2]	E26, E28	F10, C10, J11, H11
$\overline{\text{MCS}}$[0:3]	H16, G16, J15, H15	K8, J8, G8, F8
MCK[0:5]	J20, H25, A15, D20, F28, K14	H9, B15, G2, M9, A14, F1
$\overline{\text{MCK}}$[0:5]	F20, G27, B15, E20, F27, L14	J9, A15, G1, L9, B14, F2
MSYNC_IN	M28	—
MSYNC_OUT	N28	—
MODT[0:3]	—	E6, K6, L7, M7
MDIC[0:1]	—	A19, B19

1 Only two bank address (MBA) pins exist on the MPC8540 or MPC8541E.

2 Only two clock enable (MCKE) pins exist on the MPC8540 or MPC8541E.

1.9.5 Power-On Configuration Pin Changes

Table 13 summarizes the power-on pin changes.

Table 13. Power-On Configuration Pin Changes

Pin Assignment	MPC8540 POR Configuration Pins	MPC8541 POR Configuration Pins	MPC8548E POR Configuration Pins
$\overline{\text{PCI1\_REQ64}}$/$\overline{\text{PCI2\_FRAME}}$	cfg_pci_width	cfg_pci1_width	cfg_pci1_width
$\overline{\text{PCI1\_GNT}}$[1]	cfg_pci_impd	cfg_pci1_impd	cfg_pci1_impd

Table 13. Power-On Configuration Pin Changes (continued)

Pin Assignment	MPC8540 POR Configuration Pins	MPC8541 POR Configuration Pins	MPC8548E POR Configuration Pins
$\overline{\text{PCI1\_GNT}}$[2]	cfg_pci_arb	cfg_pci1_arb	cfg_pci1_arb
$\overline{\text{PCI1\_GNT}}$[3]	cfg_pci_debug	cfg_pci_debug	cfg_pci1_debug
$\overline{\text{PCI1\_GNT}}$[4]	cfg_pci_mode	cfg_pci1_hold	cfg_pci1_mode
$\overline{\text{PCI2\_GNT}}$[1]	—	cfg_pci2_impd	cfg_pci2_impd
$\overline{\text{PCI2\_GNT}}$[2]	—	cfg_pci2_arb	cfg_pci2_arb
$\overline{\text{PCI2\_GNT}}$[3]	—	—	cfg_pci1_clk
$\overline{\text{PCI2\_GNT}}$[4]	—	cfg_pci2_hold	cfg_pci2_clk
EC_MDC	cfg_tsec_reduce	cfg_tsec_reduce	cfg_tsec_1_2_reduce
TSEC1_TXD[7]	cfg_tsec1	—	cfg_tsec1_prtcl[1]
TSEC1_TXD[6]	cfg_rom_loc[0]	—	cfg_rom_loc[0]
TSEC1_TXD[5]	cfg_rom_loc[1]	—	cfg_rom_loc[1]
TSEC1_TXD[4]	cfg_rom_loc[2]	—	cfg_rom_loc[2]
TSEC1_TXD[3]	—	—	cfg_io_ports[0]
TSEC1_TXD[2]	—	—	cfg_io_ports[1]
TSEC1_TXD[1]	—	—	cfg_io_ports[2]
TSEC1_TXD[0]	—	—	cfg_tsec1_prtcl[0]
TSEC2_TXD[7]	cfg_tsec2	—	cfg_tsec2_prtcl[1]
TSEC2_TXD[6]	cfg_lb_hold_en[0]	—	—
TSEC2_TXD[5]	cfg_lb_hold_en[1]	—	—
TSEC2_TXD[4]	Device_ID[7]	—	cfg_device_ID[7]
TSEC2_TXD[3]	Device_ID[6]	cfg_tsec1	cfg_device_ID[6]
TSEC2_TXD[2]	Device_ID[5]	cfg_tsec2	cfg_device_ID[5]
TSEC2_TXD[1]	—	cfg_pci1_clk	cfg_dram_type[0]
TSEC2_TXD[0]	—	cfg_pci2_clk	cfg_tsec2_prtcl[0]
TSEC2_TX_ER	—	—	cfg_dram_type[1]
TSEC3_TXD[2]	—	—	cfg_tsec_3_reduce
TSEC3_TXD[1]	—	—	cfg_tsec3_prtcl[1]
TSEC3_TXD[0]	—	—	cfg_tsec3_prtcl[0]
TSEC4_TXD[3]/TSEC3_TXD[5]	—	—	cfg_tsec4_prtcl[1]
TSEC4_TXD[2]/TSEC3_TXD[4]	—	—	cfg_tsec4_prtcl[0]
LAD[0:19]	cfg_gpinput[0:19]	cfg_gpinput[0:19]	cfg_gpinput[0:19]
LAD[20:31]	cfg_gpinput[20:31]	cfg_gpinput[20:31]	cfg_gpinput[20:31]
LA[27]	cfg_cpu_boot	cfg_cpu_boot	cfg_cpu_boot

Table 13. Power-On Configuration Pin Changes (continued)

Pin Assignment	MPC8540 POR Configuration Pins	MPC8541 POR Configuration Pins	MPC8548E POR Configuration Pins
LA[28:31]	cfg_sys_pll[0:3]	cfg_sys_pll[0:3]	cfg_sys_pll[0:3]
LWE_B[0] / LBS_B[0]	cfg_pci_hold_en[0]	cfg_lb_hold_en[0]	cfg_pci1_speed
LWE_B[1] / LBS_B[1]	cfg_pci_hold_en[1]	cfg_lb_hold_en[1]	cfg_host_agt[0]
LWE_B[2] / LBS_B[2]	cfg_host_agt[0]	cfg_host_agt	cfg_host_agt[1]
LWE_B[3] / LBS_B[3]	cfg_host_agt[1]	cfg_rom_loc[2]	cfg_host_agt[2]
LBCTL	—	—	cfg_core_pll[0]
LALE	cfg_core_pll[0]	cfg_core_pll[0]	cfg_core_pll[1]
LGPL0 / LSDA10	cfg_rio_clk[0]	cfg_rom_loc[0]	cfg_rio_sys_size
LGPL1/$\overline{\text{LSDWE}}$	cfg_rio_clk[1]	cfg_rom_loc[1]	cfg_pci2_speed
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	cfg_core_pll[1]	cfg_core_pll[1]	cfg_core_pll[2]
LGPL3/$\overline{\text{LSDCAS}}$	cfg_boot_seq[0]	cfg_boot_seq[0]	cfg_boot_seq[0]
LGPL5	cfg_boot_seq[1]	cfg_boot_seq[1]	cfg_boot_seq[1]
MSRCID[0]	cfg_mem_debug	cfg_mem_debug	cfg_mem_debug
MSRCID[1]	cfg_ddr_debug	cfg_ddr_debug	cfg_ddr_debug

2 Software Migration

This section considers software issues on a module-by-module basis.

2.1 36-Bit Addressing

All MPC8548E IPs support a 36-bit internal address space, except for the local bus, which supports only 34 bits and aliases based on the two highest-order address bits. Care must be taken during local access window (LAW) initialization to avoid aliasing. Refer to Section 2.2, “Local Bus Controller,” for details.

In the e500v2 core, the default boot page uses the same vector as e500v1: 0x0_FFFF_FFFC. The upper 4 bits of the real page number (RPN) are taken from MAS7 when a **tlbwe** instruction is executed. By default, these bits are all zero. The MAS7 is one of the MMU assist registers defined in the e500 core. MAS7 is available for the e500v2 core only. It contains the high-order address bits of the RPN for implementations with more than 32 bits of physical address. For details, refer to the *PowerPC™ e500 Core Family Reference Manual* (supports e500v1 e500v2). An HID bit enables MAS7 updates when a **tlbre** instruction is executed. By default, this HID bit does not allow MAS7 to be updated by a **tlbre** instruction. Therefore, unless the user explicitly enables MAS7 updates or performs a move to MAS7, the value in MAS7 is always zero. This default mode is fully backward-compatible with the e500v1 core.

To keep the software backward-compatible, keep the upper 4 address bits default to zeros and always stay in the low 32-bit address space. These restrictions apply to the MMU, local access windows, DDR chip selects and LBIU chip selects, and the DMA controller.

2.2 Local Bus Controller

The local bus controller (LBC) can decode a 34-bit address with a mask through the option register (OR). BR[XBA] provides the extra 2 MSBs for the 34-bit addressing comparison. When the LBC decodes the address, the 34-bit address becomes the rightmost 34 bits of the 36-bit physical address space. LAWs should not route two address ranges to LBIU that differ only in the top 2 bits. To maintain the same external frequencies for the higher MPC8548 internal clock frequencies, divide ratios are increased from /2, /4, /8 to /4, /8, /16 through LCRR[CLKDIV]. Therefore, the same software settings as MPC8548E may result in the same external local bus frequency in MPC8548E. Other than that, the local bus controller is backward-compatible with MPC8540 or MPC8541E.

2.3 Enhanced Three-Speed Ethernet Controllers

The enhanced three-speed Ethernet controller (eTSEC) is compatible with a subset of the TSEC configuration register set as specified in the *MPC8540 PowerQUICC III™ Integrated Communications Processor Reference Manual*. For registers outside this subset, if the software driver does not alter their POR defaults, the driver should work on eTSEC without modification.

For eTSEC, the following MPC8540 or MPC8541E register should be left as defaults in the MPC8548E: MINFLR, FIFO_PAUSE_CTRL, TBDLEN, RBDLEN, CTBPTR, CRBPTR, OSTBD, OSTBDP.

If the previous versions of the software do not configure these registers, it runs without modification on the MPC8548E. If the software configures these registers, writes to these registers have no effect and reads from these register locations result in undefined data responses.

- MINFLR: Minimum frame length. Defaults to 64 bytes in TSEC. eTSEC assumes this value permanently.
- FIFO_PAUSE_CTRL: This functionality is also offered by MACCFG1[Tx_Flow] in both TSEC and eTSEC. Use MACCFG1[Tx_Flow] to enable Tx flow control instead. The FIFO_PAUSE_CTRL register space is marked as reserved in eTSEC.
- TBDLEN: TxBD data length register. This DMA register contains the number of bytes remaining in the current transmit buffer. It is implementation-specific to TSEC and this register space is marked as reserved in eTSEC.
- RBDLEN: RxBD data length register. This DMA register contains the number of bytes remaining in the current receive buffer. It is implementation-specific to TSEC and this register space is marked as reserved in eTSEC.
- CTBPTR: Current transmit buffer descriptor pointer. Pointer to current Tx buffer being processed. Implementation-specific to TSEC.
- CRBPTR: Current receive buffer descriptor pointer. Pointer to current Rx buffer being processed. Implementation-specific to TSEC.
- OSTBD: Out-of-sequence TxBD register. This register space is marked as reserved in eTSEC. This functionality can be reproduced in eTSEC via its supports for multiple Tx rings, with Ring0 override.
- OSTBDP: Out-of-sequence Tx data buffer pointer. This register space is marked as reserved in eTSEC. This functionality can be reproduced in eTSEC via its supports for multiple Tx rings, with Ring0 override.

NOTE

eTSEC behaves as if the RCTRL[RSF]: Receive short frames bit is permanently on in Rev. 1.0 silicon. It is an errata for Rev. 1 silicon. Rev. 2 silicon matches TSEC behavior. Refer to the MPC8548E device errata. In the POR device status register (PORDEVSR), MAC interface modes are decoded differently in the MPC8548 eTSEC and the MPC8540 TSEC.

2.4 DDR1 Controller

The DDR1 controller initialization is backward-compatible with that of the MPC8540 DDR1 controller. However, there is an errata ‘DDR 4’ in the MPC8548 Rev. 1 silicon that may affect the customers who still use DDR1 memories. For details, refer to the MPC8548 device errata document.

2.5 DDR2 Controller

This functionality is not in the MPC8540 or MPC8541E. For DDR2 controller initialization details, refer to the *MPC8548 PowerQUICC™ III Integrated Communications Processor Reference Manual*.

2.6 I^2C and DUART

The MPC8548 supports two channels of I^2C. The second I^2C controller has the same memory-mapped registers that are described for the first I^2C controller, 0x0_3000–0x0_3014, except the offsets are from 0x0_3100–0x0_3114. A single interrupt is shared between two I^2C channels. Some frequency configuration changes required because of new system frequencies. The MPC8540 or MPC8541E I^2C software is forward-compatible with that of the MPC8548E, except that the MPC8548E I^2C frequency divider registers (I2CFDR*n*) may need to be updated because of the new platform clock frequency of the MPC8548E.

The MPC8548E DUART software is backward-compatible with that of the MPC8540 or MPC8541E, except that the divisor for the baud rate may need to be updated because of the new platform clock frequency of the MPC8548E.

2.7 DMA Controller

The MPC8548E DMA controller and software configurations are the same as on the MPC8540 or MPC8541E, except that the MPC8548E DMA controller supports 36-bit addressing by placing high-order address bits in the ECLNDAR, ENLNDAR, ECLSDAR, and ENLSDAR registers. The address mapping for these registers in the MPC8548E are reserved fields in the MPC8540 or MPC8541E, and the reset value of these registers are zero. Therefore, the MPC8540 or MPC8541E DMA software is forward-compatible with MPC8548E as long as the user stays in the low 32-bit address space.

2.8 Local Access Windows

Compared to the MPC8540 or MPC8541E, the MPC8548 local access windows (LAW) increases from 8 to 10 windows, with respect to additional targets in MPC8548E. Local access windows 8 and 9 map to the reserved fields of the MPC8540 or MPC8541E memory space and are disabled by default. Thus, the MPC8540 or MPC8541E LAW software is forward-compatible with MPC8548E.

2.9 L2 Cache Controller

The MPC8548 L2 cache is 512 Kbytes with 8-way associativity; MPC8548E SRAM granularity also greater. In the MPC8540, all, half, or none of the memory array can be used as memory-mapped SRAM. In the MPC8548E, one, two, four, or all eight ‘ways’ of the cache can be used as SRAM. In the MPC8548E, stash-only regions can be defined to prevent stash data from polluting processor data and *vice versa*. One, two, or four ways of the cache can be dedicated as stash-only. Stash allocate disable mode allows updates of all resident cache lines without allocation of new lines. The MPC8540 or MPC8541E legacy software still works for MPC8548E L2 cache controller and does not take advantage of the new L2 features supported by MPC8548E.

NOTE

In MPC8548E Rev. 1.x.x silicon, the memory-mapped SRAM base address register (L2SRBAR) is not backward-compatible with MPC8540 or MPC8541E, in which L2SRBAR[0] maps to physical address MSB bit 32. In the MPC8548E, L2SRBAR[0] maps to physical address MSB bit 36. In MPC8548E Rev. 2.0 silicon, L2SRBAR is backward-compatible with MPC8540 or MPC8541E.

2.10 Interrupt Controller

Eight message shared interrupt (MSI) registers in the MPC8548E indicate which of the interrupt sources sharing the message register have pending interrupts. Up to 32 sources can share any individual message register. MSI bits are set by a PCI Express MSI packet or by a write to the MSI Index register.

NOTE

The addresses of the MSI registers change from Rev. 1.0 silicon to Rev. 2.0 silicon. Refer to the MPC8548E device errata document for the Rev. 1.0 silicon.

A new external interrupt summary register reports the status of external interrupt inputs and can be used as general purpose input. All these new registers added to the MPC8548E reside in the reserved memory space of the MPC8540 or MPC8541E. Thus, the MPC8540 or MPC8541E interrupt controller software is forward-compatible with MPC8548E.

2.11 Reset Control

In the MPC8548E, software can set $\overline{\text{HRESET\_REQ}}$ through the reset control register (RSTCR), which is in the reserved field of the MPC8540 or MPC8541E memory space. This feature is not supported in the MPC8540 or MPC8541E.

2.12 Watchpoint, Trace Buffers, PerfMon, and Debug

Essentially, watchpoint and debug facilities are unchanged from the MPC8540, but one additional performance monitor counter is added in the reserved memory space of the MPC8540 or MPC8541E. In the MPC8548E, there are nine performance monitor counters (PMC1–PMC9) in addition to the cycle counter (PMC0).

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