Freescale Semiconductor
Application Note

Document Number: AN2587
Rev. 1, 01/2007

Software Migration from the NPe405H/L to PowerQUICC™ II

by *Paul Genua*
NCSG
Freescale Semiconductor, Inc.

As embedded systems become more complex, software complexity ultimately rules and has become the deciding factor when architecting a new system. The cost of porting code can sometimes offset the benefits that come with the additional features of a new processor platform. Fortunately, software migration can be easy, especially when staying within a processor core architecture. This document details device driver and lower-level software migration from the IBM PowerNP™ (NPe405H, NPe405L) to Freescale's PowerQUICC™ II product family. As both are PowerPC™ processors (built on Power Architecture™ technology), software migration has few caveats, leaving architects with decisions based more on hardware functionality and processor feature sets.

Contents

freescale™ semiconductor

1 Feature Comparison

The IBM PowerNP processor family builds off of IBM's experience with the 405GP and 405CR families of processors. It includes a PowerPC core as well as integrated peripherals such as the following:

- Multiple fast Ethernet controllers
- SDRAM controller
- PCI bus
- HDLC controller with time-slot assigner (TSA)
- UART
- I2C
- DMA capability
- Peripheral bus

The PowerQUICC II (PQII) is the successor to the highly popular PowerQUICC (8xx) family of processors from Freescale. Over the years since its initial product launch, the PQII has grown into a whole family of devices, ranging from the fully featured MPC8280 to the ultra-low-cost MPC8270VR. The latest devices in this family were built using 0.13-µ technology, enabling very low power (~1.5 W) at high frequencies (~450 MHz).

At the heart of the PQII is the communications processor module (CPM), a RISC protocol engine capable of processing Ethernet, ATM, HDLC, and so on, without intervention from the core PowerPC processor. The PQII has the ability to be updated with new, custom, and/or enhanced, protocols through microcode updates to the CPM. For example, Freescale offers microcode for SS7 signaling, as well as microcode packages adding features such IMA (without PowerPC core intervention) in addition to the standard protocols shipped with the silicon. This flexibility eases the processing burden on the PowerPC and can increase time-in-market, with microcode updates for new protocols as they become needed in the marketplace.

Typical features available in the PQII include the following:

- Multiple fast Ethernet controllers
- ATM SARRing
- PCI bus
- SDRAM controller
- 256-channel HDLC controller
- Time-slot assigner
- I2C
- SPI
- DMA
- Multiple UARTS

Table 1 is a side-by-side comparison of features commonly available to both processors.

Table 1. Feature Comparison of PowerNP vs. PowerQUICC II

Feature	PowerNP	PowerQUICC II
PCI bus	Yes	Yes
Peripheral bus	32-bit bus	64-bit 60x-compliant bus
SDRAM controller	Yes	Yes
User programmable memory controller	No	Yes
External DMA channels	4 channels	4 channels
Cache	16K I / 8K D	16K I / 16K D
UARTs	2	Up to 5
TDM interfaces	2	Up to 8
ATM SAR engine	No	Yes
IMA functionality	No	Yes
Technology	0.25 µ	0.13 µ
Frequency	Up to 266 MHz	Up to 450 MHz
Power	2.1 W at 200 MHz	1.5 W at 450 MHz, 0.8 W at 266 MHz

The features of the NPe405 are shown to be a subset of the features found on the PQII, enabling an easy hardware migration to the PQII. Upon further investigation, the features common to the two processors are somewhat similar from a software point of view as well, enabling a reasonably easy migration from the NPe405 to the PQII from both a hardware and software prospective.

2 Software Migration Overview

High-level software such as a RTOS (real-time operating system) and any high-level applications riding on top of the RTOS (for example, a web server) should not be affected by processor selection. A RTOS typically utilizes a board support package (BSP) in order to communicate with the underlying hardware, and this BSP is subject to change with new hardware. Changes to a BSP are outside of the scope of this document, since these changes are not only RTOS dependent, but hardware dependent as well.

Device drivers are the most affected software element in migrating to a new hardware platform. The term “device driver” is concerned with communication with anything external to the processor through mechanisms internal to the processor. This includes but is not limited to: Ethernet physical layer devices (PHYs) through an internal MAC, memory devices through the memory controller, T1 framers through a time-slot interchanger (TSA), and I2C devices through an internal I2C controller. In porting code from the NPe405 to the PQII, differences in the following are explored:

- The SDRAM controller
- Buffer descriptors

- The time-slot assigner
- DMA transfers

3 SDRAM Controller

Many similarities exist between the integrated SDRAM controllers of the PQII and the NPe405. However, the PQII SDRAM controller allows for some enhanced flexibility in SDRAM configuration pertaining to memory sizing and row/column multiplexing; thus, configuration of the two SDRAM controllers differs somewhat.

3.1 NPe405

The PowerNP utilizes sixteen indirectly accessed registers for status and control of the SDRAM controller. They are accessed through the PowerNP's SDRAM0_CFGADDR and SDRAM0_CFGDATA registers. Upon system reset of the processor, software must configure and then enable the SDRAM controller. The PowerNP registers that are involved with the SDRAM controller are outlined below in Table 2 through Table 4.

Table 2. NPe405 SDRAM0_CFG

Bits	Mnemonic	Description
0	DCE	SDRAM controller enable/disable
1	SRE	Self refresh enable/disable
2	PME	Power management enable/disable
3	MEMCHK	ECC enable/disable
4	REGEN	Registered memory enable/disable
5–6	DRW	SDRAM width (must be set to 32 bits)
7–8	BRPF	Burst read prefetch
9	ECCDD	ECC driver enable/disable
10	EMDULR	Condition of bus when inactive

Table 3. NPe405 SDRAM0_TR

Bits	Mnemonic	Description
0–6	—	Reserved
7–8	CASL	CAS latency
9–11	—	Reserved
12–13	PTA	Precharge to activate minimum
14–15	CTP	Command to precharge minimum
16–17	LDF	SDRAM command leadoff
18–26	—	Reserved

Table 3. NPe405 SDRAM0_TR (continued)

27–29	RFTA	CAS before RAS refresh to activate
30–31	RCD	RAS to CAS delay

Table 4. NPe405 SDRAM0_B0CR

Bits	Mnemonic	Description
0–9	BA	Base address
10–11	—	Reserved
12–14	SZ	Size
15	—	Reserved
16–18	AM	Addressing mode
19–30	—	Reserved
31	BE	Memory bank enable

3.2 PowerQUICC II

Similarities exist between the SDRAM controller in the NPe405 and the PQII, although the exact register format differs between the two. Registers within the PQII are directly accessed by the CPU, instead of indirectly accessed as with the NPe405.

The PQII registers that are involved with the SDRAM controller are outlined below in Table 5 through Table 7.

Table 5. PowerQUICC II BRx

Bits	Mnemonic	Description
0–16	BA	Base address
17–18	—	Reserved
19–20	PS	Size
21–22	DECC	ECC enable/disable
23	WP	Write protect
24–26	MS	Machine select
27	EMEMC	External memory controller enable
28–29	ATOM	Atomic operation enable
30	DR	Data pipelining enable/disable
31	V	Valid bit

Table 6. PowerQUICC II ORx

Bits	Mnemonic	Description
0–11	SDAM	Address mask
12–16	LSDAM	Lower address mask
17–18	BPD	Banks per device
19–21	ROWST	Row start address
22	—	Reserved
23–25	NUMR	Number of row address lines
28	PMSEL	Page mode select
27	IBID	Internal bank interleaving
28–31	—	Reserved

Table 7. PowerQUICC II PSDMR

Bits	Mnemonic	Description
0	PBI	Paged based interleaving
1	RFEN	Refresh enable
2–4	OP	SDRAM operation
5–7	SDAM	Address multiplex size
8–10	BSMA	Bank select multiplexed address
11–13	SDA10	A10 control
14–16	RFRC	Refresh recovery
17–19	PRETOACT	Precharge to activate interval
20–22	ACTTORW	Activate to read/write
23	BL	Burst length
24–25	LDOTOPRE	Last data out to precharge
26–27	WRC	Write recovery time
28	EAMUX	External address mux
29	BUFCMD	External buffer timing
30–31	CL	Cas latency

3.3 Porting to PowerQUICC II

Many of the SDRAM controller registers map effortlessly from the PowerNP to the PQII.

Consider the following SDRAM organization:

- 32-bit port size (4 × 8 × 64 Mbit)
- Each device has 12 rows, 9 columns, and 4 banks.

For bank-based interleaving, the address bus should be partitioned as in Table 8.

Table 8. Address Bus Partitioning for SDRAM

A[0–6]	A[7–8]	A[9–20]	A[21–29]	A[30–31]
MSB of address	Bank select	Row	Column	N/A

Table 9 indicates that during an activate command, addresses A[7–20] are multiplexed over A[16–29].

Table 9. SDRAM During Activate

A[0–15]	A[16–17]	A[18–29]	A[30–31]
—	Bank select A[7–8]	Row A[9–20]	N/A

Table 10 indicates that during a read/write command AP alternates with A[8] of the row lines.

Table 10. SDRAM During Read/Write Command

A[0–5]	A[16–17]	A[19]	A[20]	A[21–29]	A[30–31]
—	Bank select A[6–7]	AP	N/A	Column	N/A

Using the data above and assuming AC timing information, such as CAS latency, initialization of this SDRAM would be as shown in Table 11.

Table 11. SDRAM Register Mappings NPe405 to PQII

NPe405 Register	PQII Register	Comments
SDRAM0_CFG[SRE]	PSDMR[RFEN]	Refresh enabled
SDRAM0_TR[CASL]	PSDMR[CL]	CAS latency
SDRAM0_CFG[DRW]	BRx[PS]	SDRAM width (must be 32 bits in NPE405)
SDRAM0_TR[PTA]	PSDMR[PRETOACT]	Precharge to activate timing
SDRAM0_TR[CTP]	PSDMR[LDOTOPRE]	R/W command to precharge timing
SDRAM0_TR[RFTA]	PSDMR[RFRC]	Refresh recovery timing
SDRAM0_TR[RCD]	PSDMR[ACCTORW]	Activate to read/write timing
SDRAM0_B0CR[BA]	BRx[BA]	Base address
SDRAM0_B0CR[BE]	BRx[V]	Memory valid

Unfortunately, memory size and row and column multiplexing are not as readily ported from the NPe405 to the PQII.

The NPe405 uses pre-defined “modes” (SDRAM0_B0CR[AM]), each of which defines a supported configuration of SDRAM. For the above example (12 row, 9 column, 4 banks) the NPe405 would be set to mode 2. The mode, combined with the size (SDRAM0TR[SZ]) of memory, in this case 32 Mbytes, initializes the memory controller’s multiplexing and A10 pin setting.

The PQII instead provides increased flexibility by not predefining memory configurations. For the above configuration, it would be necessary to set the following:

- ORx[BPR] to two banks per device
- ORx[ROWST] to 0b0110 to define RowStart at A9
- ORx[NUMR] to 0b011 to define 12 rows
- PSDMR[SDAM] to 0b001 to set up address multiplexing
- PSDMR[SDA10] to 0b100 to set up AP output on A8

Additionally, the PQII accommodates future memory expansion with dedicated bank select signals, instead of using address lines to select banks. This allows migration to SDRAM devices with differing numbers of rows and columns without hardware change. In order to use the dedicated bank select pins, PSDMR[BSMA] must be set to the corresponding addresses that are to be output.

4 Buffer Descriptors

Buffer descriptors (BDs) are the primary data structures used on both the NPe405 and the PQII for passing data between higher level software and on-chip serial communication peripherals. Organization of BDs differs between the NPe405 and the PQII, but the basic structure is similar, easing migration to the PQII.

As an example, the differences in BDs for the serial communication controllers (SCCs) of both the NPe405 and the PQII will be examined.

4.1 NPe405 Buffer Descriptors

The NPe405 locates buffers and buffer descriptors in external memory. The descriptors are pointers to the actual buffers organized as circular queues. Each on-chip peripheral is associated with two tables (transmit and receive) of up to 256 buffer descriptors per table.

Figure 1 shows an example of buffer descriptors and the data buffer organization.

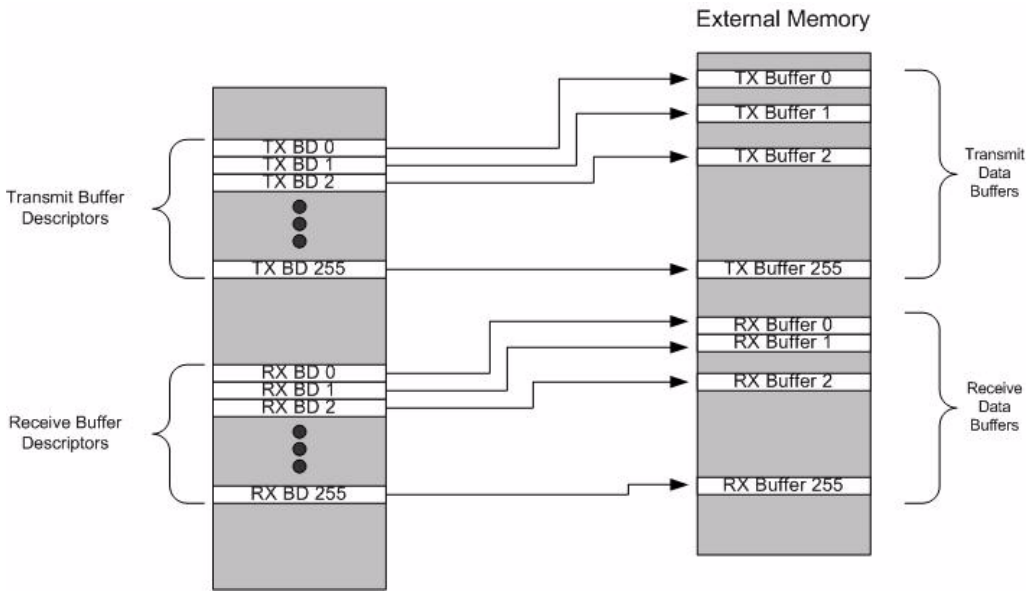

Figure 1. Example of Buffer Descriptors and Data Buffer Organization

Table 12 shows the NPe405 buffer descriptor format.

Table 12. NPe405 Buffer Descriptor Format

Offset	Bits	Field	Description
+0	0–15	Status and control	BD status and control information
+2	4–15	Data length	Number of bytes to be sent/received
+4	0–15	High buffer pointer	Define 32-bit address where BD starts
+6	0–15	Low buffer pointer	

Table 13 shows the NPe405 transmit and control field.

Table 13. NPe405 Transmit Status and Control Field

Bits	Mnemonic	Description
0	R	Ready. Indicates Tx buffer is ready for transmission.
1	W	Wrap. Last buffer in the circular BD table.
2	CM	Continuous mode. Indicates continuous transmission regardless of ‘R’ bit.
3	L	Last buffer in frame
4	—	Reserved
5	I	Specifies an interrupt to be generated upon processing of BD.
6	MS	Allows for multiple transmission of a packet.
7	A	Reports abort errors during transmission.

Table 13. NPe405 Transmit Status and Control Field (continued)

8	FU	Reports FIFO buffer underrun errors
9	U	Set to specify that the frame is an unnumbered frame.
10	D	Notifies software the corresponding frame has not been transmitted because link is disconnected.
11–15	—	Reserved

Table 14 shows the NPe405 receive and control field.

Table 14. NPe405 Receive Status and Control Field

Bits	Mnemonic	Description
0	E	Empty. Indicates that the receive data buffer is ready to receive data.
1	W	Wrap. Last buffer in the circular BD table.
2	CM	Continuous mode. Indicates continuous transmission regardless of ‘R’ bit.
3	L	Indicates last buffer in frame
4	F	Indicates first buffer in frame
5	I	Specifies an interrupt to be generated upon processing of BD
6	NBA	Reports non-byte-aligned frame errors during reception
7	TS	Reports detection of too-short frame error
8	TL	Reports detection of a too-large error
9	FE	Reports detection of a frame check sequence (FCS) error
10	A	Reports detection of an abort error
11	FO	Reports detection of a FIFO overrun
12	PE	Reports detection of a protocol error during reception
13	NSE	Reports detection of a frame-sequence error
14–15	—	Reserved

4.2 PowerQUICC II

The PQII also uses buffer descriptors (BDs) to form circular queues of buffers in order to communicate with on-chip peripherals. For the purposes of this document the PQII’s SCC will be used as an example of how BDs are organized within the PQII. The SCC is a communications controller within the PQII CPM that is capable of protocols such as UART, HDLC, AppleTalk, and 10bT Ethernet.

SCC parameter RAM, located within the PQII’s internal dual-port RAM, is used to locate BD tables in memory. For an SCC, BD tables can be located either within the internal dual-port RAM or in external memory. Other peripherals, such as fast communications controllers (FCCs) and multi-channel controllers (MCCs), require BD placement in external memory. Buffers are then pointed to by the BD tables and should also be located in external memory.

Figure 2 shows the PQII SCC buffer descriptor organization.

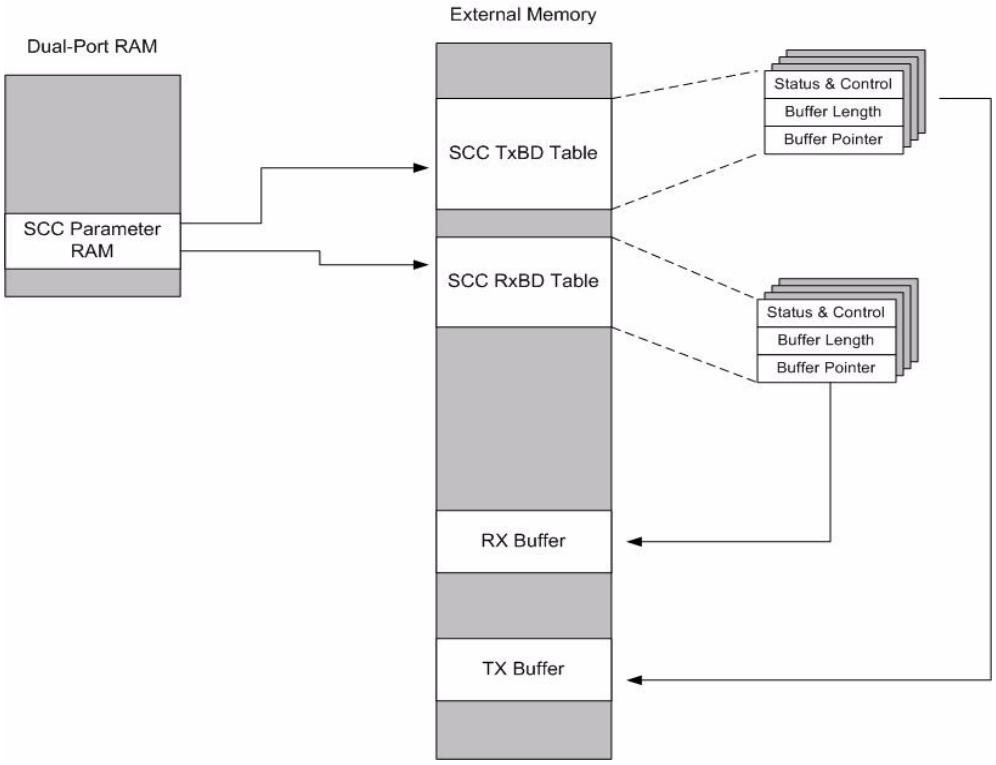

Figure 2. PQII SCC Buffer Descriptor Organization

Table 15 shows the PQII buffer descriptor format.

Table 15. PQII Buffer Descriptor Format

Offset	Bits	Field	Description
+0	0–15	Status and control	BD status and control information
+2	0–15	Data length	Number of bytes to be sent/received
+4	0–15	High buffer pointer	Defines 32-bit address where BD starts
+6	0–15	Low buffer pointer	

Table 16 shows the PQII SCC HDLC TxBD status and control field.

Table 16. PQII SCC HDLC TxBD Status and Control Field

Bits	Mnemonic	Description
0	R	Ready. Used to indicate that the transmit data buffer is ready for transmission.
1	—	Reserved
2	W	Wrap. Last buffer in the circular BD table.
3	I	Specifies if an interrupt is to be generated upon processing of buffer

Table 16. PQII SCC HDLC TxBD Status and Control Field (continued)

4	L	Indicates last buffer in frame
5	TC	Tx CRC. Specifies if a CRC should be appended to the end of the frame.
6	CM	Continuous mode. Allows for continuous transmission regardless of “R” bit status.
7–13	—	Reserved
14	UN	Underrun. Set after the SCC sends a buffer and a transmitter underrun occurs.
15	CT	CTS lost. Indicates CTS lost errors during transmission.

Table 17 shows the PQII HDLC RxBD status and control field.

Table 17. PQII SCC HDLC RxBD Status and Control Field

Bits	Mnemonic	Description
0	E	Empty. Indicates if the corresponding buffer is full or empty.
1	—	Reserved
2	W	Wrap. Last buffer in the circular BD table.
3	I	Specifies if an interrupt is to be generated upon processing of buffer
4	L	Indicates last buffer in frame
5	F	First in frame. Indicates that buffer is first in frame.
6	CM	Continuous mode. Allows for continuous reception of data, regardless of ‘E’ bit.
7	—	Reserved
8	DE	DPLL error. Set if a DPLL error occurs when buffer is being received.
9	—	Reserved
10	LG	Reports Rx frame length violation
11	NO	Reports Rx nonoctet aligned frames
12	AB	Reports an Rx abort sequence
13	CR	Reports an Rx CRC error
14	OV	Reports a receiver overrun during frame reception
15	CD	Reports loss of carrier detect

4.3 Porting to the PowerQUICC II

Since both the PQII and the NPe405 rely on circular queues of buffer descriptors, porting software applications from the NPe405 to the PQII should be relatively straightforward. Buffer descriptors

themselves seem to have a very similar format. However there may be some application-specific differences. For example, the PQII utilizes BDs for all serial communications channels, including UARTs and I2C. The NPe405 does not use BDs for either of the above mentioned peripherals.

5 Time-Slot Assignment

The mechanisms for handling time-slot assignment differ from the NPe405 to the PQII in both the actual on-chip peripherals and the registers used to initialize time slots.

5.1 NPe405 Time-Slot Assignment

The NPe405 provides two separate time-slot assigners (TSA1 and TSA2). Each time-slot assigner consists of two RAMs (transmit and receive) of 512 entries each used to assign time slots within the NPe405. Each channel can be programmed independently with 1-bit resolution at up to 4.096 Mbps or 8.192 Mbps on port A.

NOTE

At rates > 4.096 Mbps only port A is enabled, and port B must be disabled.

Table 18 shows the NPe405 Tx time-slot assignment.

Table 18. NPe405 Tx TSA

Bits	Mnemonic	Description
0–23	—	Reserved
24	A/U	Indicates that bit is assigned or unassigned to the corresponding channel
25–26	DV	Default value that the TSA places on the Tx line for a disabled channel
27–31	CN	Specifies channel number (from 0 to 31)

Table 19 shows the NPe405 Rx time-slot assignment.

Table 19. NPe405 Rx TSA

Bits	Mnemonic	Description
0–25	—	Reserved
26	A/U	Indicates that bit is assigned or unassigned to the corresponding channel
27–31	CN	Specifies channel number (from 0 to 31)

5.2 PowerQUICC II TSA

The PQII provides two separate time-slot assigners (TSA1 and TSA2) capable of connecting to four independent TDM channels at up to E1 rate each. TDMa also has the ability to be used to interface to a T3 or DS3 clear channel. External signals allow for the option of independent transmit and receive frame syncs and clocks. Figure 3 shows the PQII TSA organization.

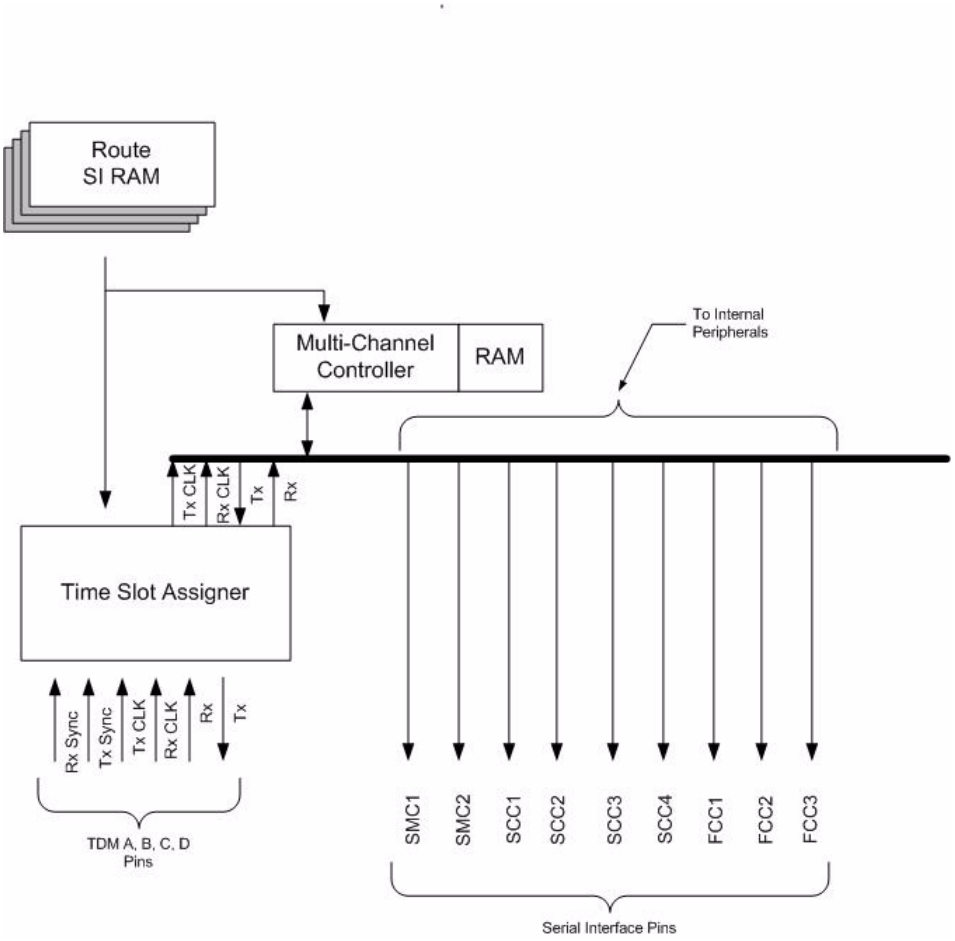

Figure 3. PowerQUICC II TSA Organization

Each serial interface (SI) has two SI RAMs associated with it, one for transmit and one for receive. Each SI RAM is composed of four banks of 64 16-bit entries (256 entries total) that enable it to control TDM channel routing to all serial devices within the CPM of the PQII. Each entry in the table defines the routing of 1–8 bits or bytes at a time.

As is evident in Figure 3, the PQII TSA has the ability to work in concert with the multi-channel controllers (MCCs). MCCs each have the ability to perform HDLC formatting/de-formatting or act as a transparent channel for up to 128 serial full-duplex data channels. There is an option in the SI RAM table to route a channel to a MCC or not; routing to a MCC changes the format of the SI RAM entry. Without the MCC enabled, software has the ability to route directly from a serial TDM interface to a serial communications channel (that is, FCC, SCC, SMC).

Table 20 shows the PQII SI RAM table with MCC not enabled.

Table 20. PQII SI RAM Table for MCC Off

Bits	Mnemonic	Description
0	MCC	Indicates if MCC is used or not

Table 20. PQII SI RAM Table for MCC Off (continued)

1	SWTR	Allows for special circumstances where its desired to receive data on the Tx pin and transmit data on the Rx pin
2–5	Slacks	Selects use of internal strobe pins
6	—	Reserved
7–10	CSEL	Channel select. Selects routing of TDM data to a specific SCC, FCC, SMC.
11–13	CNT	Indicates number of bits/bytes in this time slot
14	BYT	Byte resolution. Defines the number in CNT field as either bits or bytes.
15	LST	Indicates last entry in SI RAM table

Table 21 shows the PQII SI RAM table with MCC enabled.

Table 21. PQII SI RAM Table for MCC On

Bits	Mnemonic	Description
0	MCC	Indicates if MCC is used or not. Set to ‘1’ to enable MCC.
1	LOOP/ECHO	Channel loopback or echo mode.
2	SUPER	Current timeslot is part of a superchannel
3–10	MCSEL	Indicates MCC channel this timeslot is routed to
11–13	CNT	Indicates number of bits/bytes in this time slot
14	BYT	Byte resolution. Defines the number in CNT field as either bits or bytes.
15	LST	Indicates last entry in RAM.

5.3 Porting to the PowerQUICC II TSA

The time-slot assignment/configurations supported by the NPe405 and the PQII are very similar, so porting between the two should be straightforward. The PQII TSA allows for superchannels by combining multiple time slots into a single channel, which provides added functionality to software if the user chooses to take advantage of it. In addition, the PQII gives the user the flexibility to route directly from the TSA to a serial communications device, or to the MCC for HDLC or transparent processing. Unfortunately there is no MCC in the NPe405, so routing within the MCC would mean additional programming work.

The MCC is configured using buffer descriptors that are very similar to the PQII SCC buffer descriptors in Section 4, “Buffer Descriptors,” of this application note.

Table 22 shows the PQII MCC transmit status and control field.

Table 22. PQII MCC Transmit Status and Control Field

Bits	Mnemonic	Description
0	R	Ready
1	—	Reserved
2	W	Wrap. Indicates that this BD ends the circular BD table.
3	I	Specifies that an interrupt should be generated upon processing of this BD
4	L	Indicates this BD is the last BD in a frame
5	TC	Specifies that the MCC is to append a CRC at the end of data transmitted
6	CM	Continuous mode. Allows for continuous retransmission of data in buffer without examining ‘R’ bit.
7	—	Reserved
8	UB	User defined bit the HW does not touch
9–11	-	Reserved
12–15	PAD	Specifies the number of idle symbols to be sent after frame closing flag

Table 23 shows the PQII MCC receive status and control field.

Table 23. PQII MCC Receive Status and Control Field

Bits	Mnemonic	Description
0	E	Indicates that the Rx BD is empty and ready to receive data.
1	—	Reserved
2	W	Wrap. Indicates that this BD ends the circular BD table.
3	I	Specifies that an interrupt should be generated upon processing of this BD
4	L	Indicates this BD is the last BD in a frame
5	F	First. Indicates this BD points to the 1st buffer in frame
6	CM	Continuous mode. Allows for continuous retransmission of data in buffer without examining ‘E’ bit.
7	-	Reserved
8	UB	User defined bit the HW does not touch
9	—	Reserved

Table 23. PQII MCC Receive Status and Control Field (continued)

10	LG	Reports too-large frame error
12	AB	Reports aborted frame errors
13	CR	Reports bad CRC errors
14–15	—	Reserved

One of the major differences between the NPe405 TSA and the PQII TSA lies in the configuration of dynamic time-slot assignment.

The NPe405 allows software to dynamically change the routing of the TSA through a process consisting of the following:

- Disabling the channel through the TECR register
- Waiting for the TESR to report that the channel is inactive
- Configuring the new TSA entry
- Assigning the TSA entry (through the A/U bit)
- Setting the “Go” bit in TECR to activate the channel

The PQII utilizes two sets of TSA tables to perform dynamic time-slot assignment. One set is active, while one set shadows the active table and is updated with new routes by software. Once any updates to the TSA are made to the shadow RAM, software simply swaps the active TSA with the shadow TSA table, and the new time-slot assignment takes effect.

6 DMA

Both the NPe405 and the PowerQUICC II support a DMA function.

6.1 NPe405 DMA

The NPe405 includes a four channel (unidirectional) DMA controller on-chip. Each channel is programmable through configuration registers. The DMA controller can read and write any address accessible by the NPe405.

For each DMA transfer it is necessary to program a channel’s control, source, destination, and count registers for each transfer. The NPe405 additionally provides for “scatter/gather” DMA functionality. Scatter/gather functionality allows for software to use a descriptor table to accommodate multiple DMA transfers in place of individually programming each channel for every transfer.

The DMA implements an internal 32-byte buffer, enabled on a per-channel basis, to minimize the number of discrete memory transactions.

Each channel of the DMA is configurable for either peripheral or memory-to-memory transfers.

6.2 PowerQUICC II DMA

The PQII provides two physical serial DMA (SDMA) engines for transactions to/from serial controllers (FCC, MCC, SCC, SMC, SPI and I2C). Four additional virtual SDMA channels are provided to be used as general-purpose independent DMA (IDMA) channels.

Dual address IDMA channels transfer data from a source to its destination using an intermediate transfer buffer, located internal to the PQII (in dual-port RAM). Transfers can be memory-to-memory, memory-to-peripheral, or peripheral-to-memory. DMA requests can be made internally or can be configured to operate in external request mode using external ~DREQ pins. Figure 4 shows a PQII dual-address DMA transfer.

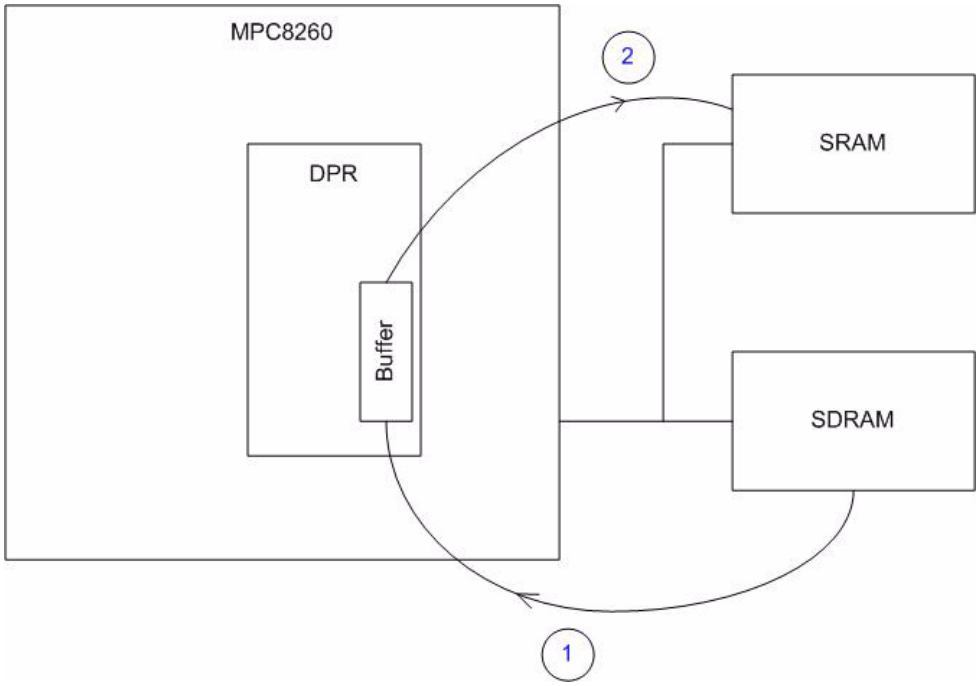

Figure 4. PQII Dual-Address DMA Transfer

For a dual-address transfer, the IDMA first reads from the source bus and fills an internal transfer buffer with data to be transferred. It then empties the data from the buffer to the destination bus by initiating a separate transfer to the destination device. Since accesses to memory are initiated by two separate transfers (in the case of Figure 4, one read from SDRAM, and one write to SRAM) two addresses would be put on the bus, hence the name “dual-address transfer”.

The internal transfer buffer is described in Section 19-5, “IDMA Transfers,” in the *MPC8260 PowerQUICC II Family Reference Manual*. The size of the buffer is determined by DMA_WRAP and must be a multiple of 32 bytes.

STS/DTS are the transfer sizes of the source and destination memory. Valid sizes are 1,2,4, and 8 bytes, or the size of data to be transferred if the memory/peripheral accepts bursts.

SS_MAX is defined as the steady-state maximum transfer size of an IDMA transfer. The transfer buffer is either filled or emptied with SS_MAX bytes. For example, if STS is initialized to SS_MAX, the buffer will be filled with one burst access from the source and written to the destination in multiple transfers.

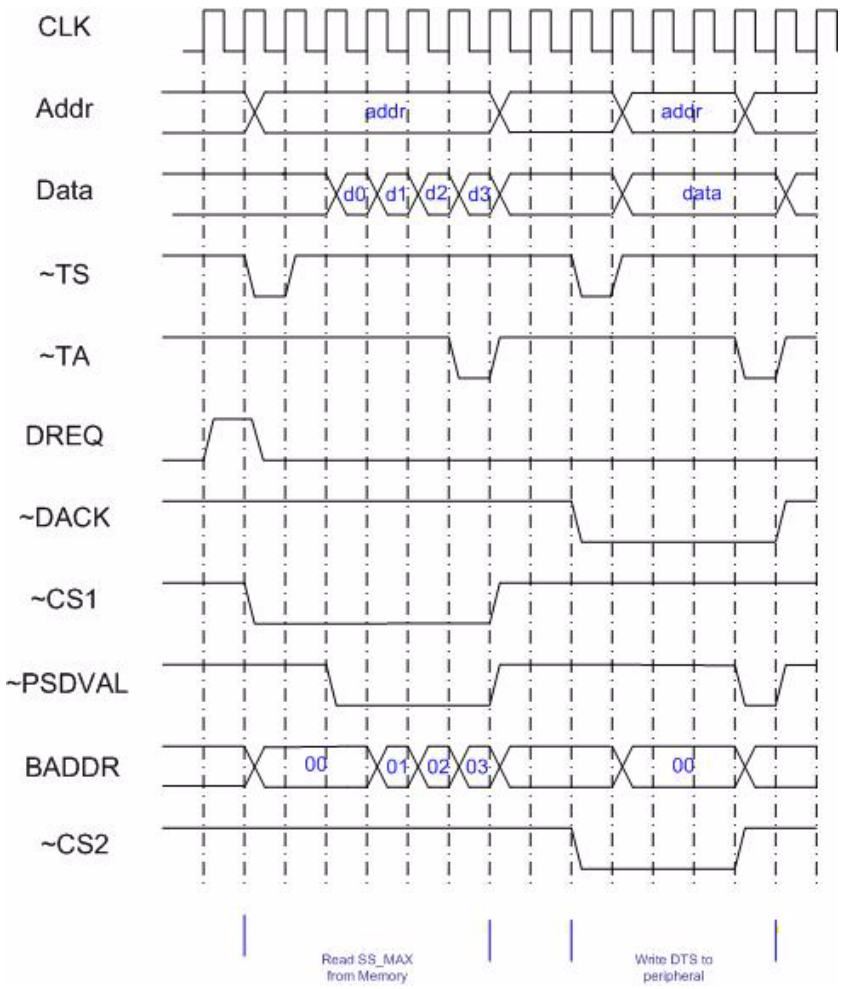

Figure 5. PQII Dual-Address DMA Timing Diagram

Figure 5 is an example of a dual-address memory-to-peripheral DMA transfer. In this case memory is on Chip Select1, and the Peripheral is on CS2. Upon a DREQ assertion by the peripheral, SS_MAX bytes are read from the memory. For the purposes of this example we can imagine that SS_MAX = STS = 4 and the port size of the memory is 32 bits wide. Thus we see four bytes transferred from the memory into the internal buffer. The peripheral port size is one byte for the purpose of this discussion, so the following write to the peripheral only empties one byte from the internal buffer. It will require three more DREQ assertions by the peripheral in order to transfer the full four bytes. When the internal transfer buffer has fewer than DTS bytes left (in this case, one) the next DREQ assertion triggers a read of SS_MAX bytes from memory automatically followed by a write to the peripheral.

Note that this case is an example of bursting, and the corresponding memory assignment must be programmed to accept bursts (that is, PQII UPM programming).

NOTE

DREQ is an active high signal. This was an errata to the original 8260 user's manual.

Single-address mode bypasses the internal transfer buffer of the 82xx and instead transfers data directly between a peripheral and memory.

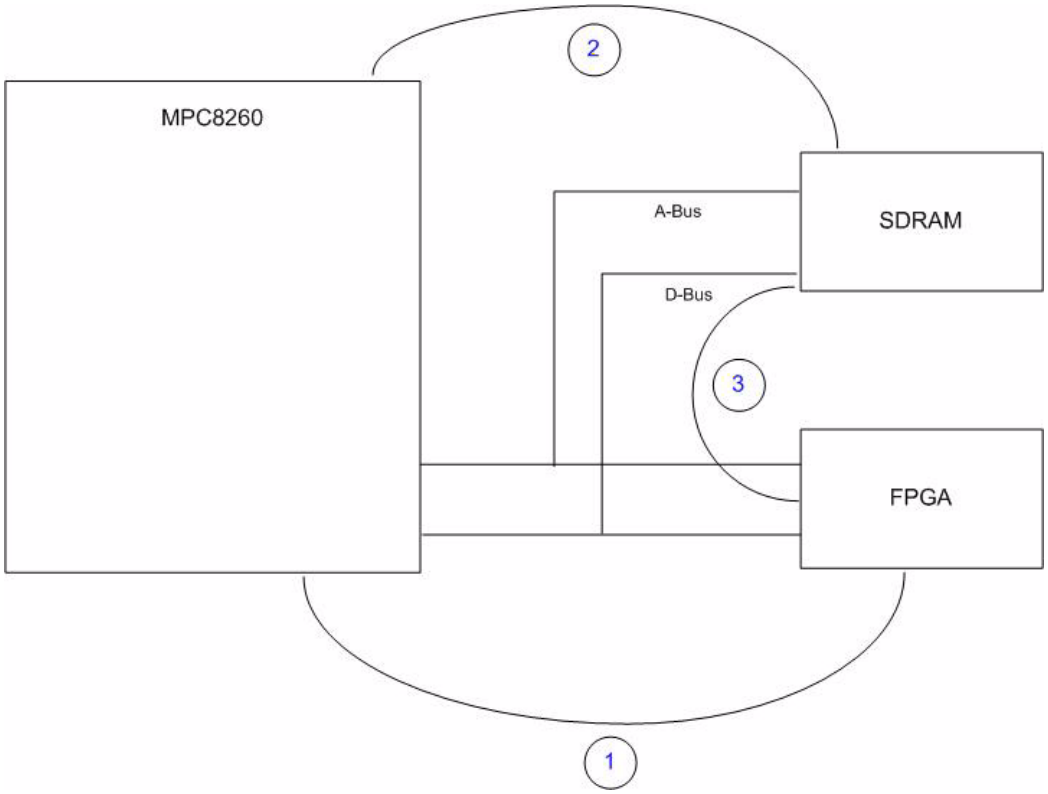

Figure 6. PowerQUICC II Single Access DMA

For the DMA example in Figure 6, steps would be as follows:

1. FPGA requests a DMA through the ~DREQ signal.
2. PQII preforms a write access to memory, with an address and write signal, while asserting ~DACK to acknowledge the DMA request.
3. Data is driven on the data bus sourced by the FPGA and input to the SRAM.

The internal intermediate transfer buffer is not used in this mode, and thus all parameters (SS_MAX, DPR_BUF, DMA_WRAP) related to the dual-port RAM are not used.

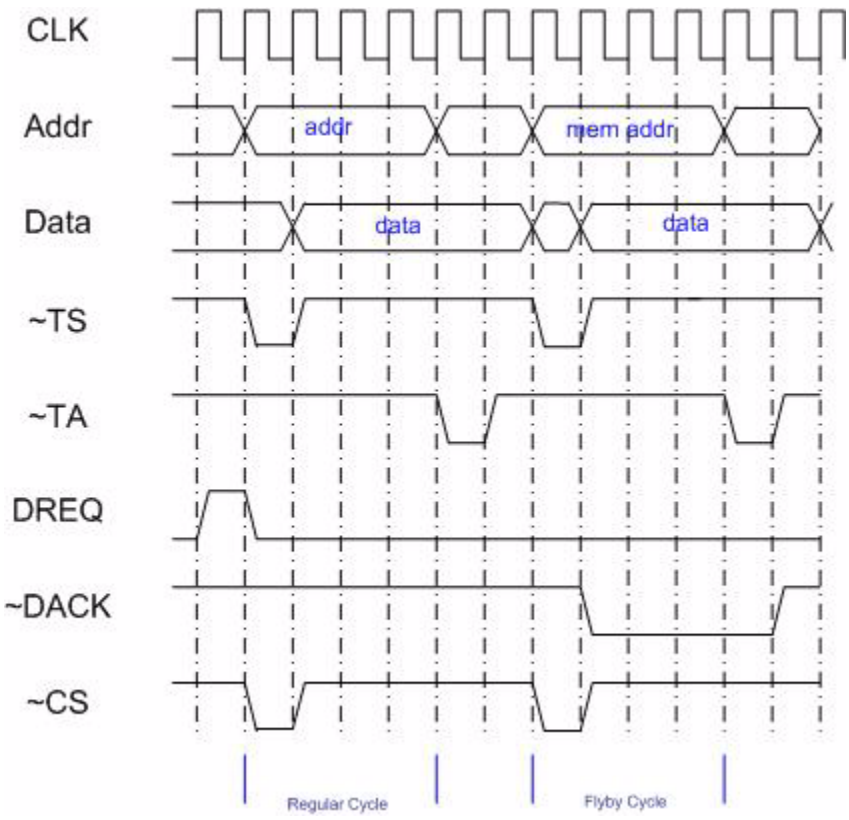

Figure 7. Fly-By Peripheral to Memory Timing

Figure 7 is an example of fly-by timing for a peripheral to memory transfer. The above example is of a regular data tenure on the bus prior to the DMA transfer. During the fly-by transfer, the address and ~CS to the memory is provided to the memory from the 82xx while the data is put on the bus directly from the peripheral.

In this case each DREQ assertion by the peripheral triggers a transfer of the full port size between the peripheral and memory. When the program transfer length is reached or ~DONE is asserted by the peripheral, the buffer descriptor is closed.

6.3 Porting to PowerQUICC II

The PQII and NPe405 provide equivalent DMA functionality to the user. The NPe405's DMA engine is similar to the PQII's dual-address mode transfers, with some basic differences:

- NPe405 has an internal 32-byte buffer, while the PQII has a programmable internal buffer
- NPe405 has the ability to implement scatter/gather through linked lists. The PQII implements similar functionality through circular buffers.

In addition the PQII allows faster transfers to peripherals through single-address mode. Since this feature is not currently available on the NPe405, any porting of DMA features should use the dual-address mode DMA functionality of the PQII. Single-address DMAs could conceivably be implemented at a later date to increase the performance of certain DMA transfers.

7 Conclusions

Migrating to a new hardware platform has inherent software implications and typically becomes a challenge engineers are unwilling to face. Fortunately, both the NPe405 and the PQII are based on the PowerPC architecture, enabling high-level software to port with minimal trouble. The low-level feature set of the NPe405 is a subset of the features available on the PQII, with many similarities between implementation in the two architectures. As shown in this document, porting low-level code is a relatively straightforward process.

With software migration no longer a deciding factor in processor selection, embedded processors can once again be decided upon by system architects. Performance, flexibility, and features become the deciding factors, and the PowerQUICC II family provides a compelling story as the processor choice for many of today's embedded systems.

8 Revision History

Table 24 provides a revision history for this application note.

Table 24. Document Revision History

Revision Number	Substantive Change(s)
1	Document template update.
0.1	Added TOC, history table, minor nontechnical corrections, changed document title from 'Software Implications of Migrating from the NPe495H/L to PowerQUICC II' to 'Software Migration from the NPe495H/L to PowerQUICC II'.
0	Initial release.

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: AN2587
Rev. 1
01/2007