AN13906

ADC Usage for LPC86x

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Document Information

Information	Content
Keywords	LPC86x, ADC, ADC accuracy
Abstract	This application note introduces and provides the usage note for the ADC module of LPC86x.

1 Introduction

LPC86x series contain a 12-bit successive approximation Analog-to-Digital Converter (ADC). This application note provides the usage note for the ADC module of LPC86x.

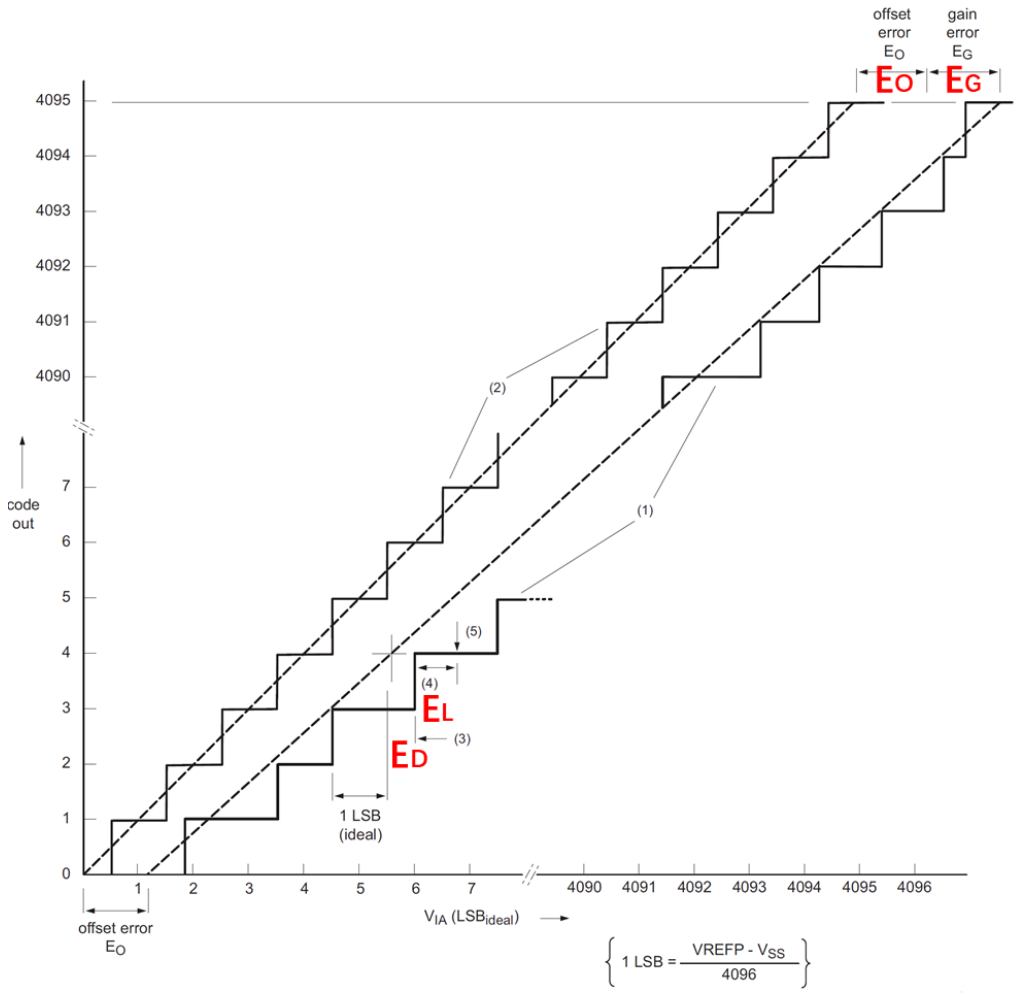
During the application design, the ADC accuracy is the most important factor which affects the design. The application note illustrates the methods for improving LPC86x ADC accuracy.

2 Main factors of ADC accuracy

To evaluate the ADC accuracy, use the below static characteristic parameters:

- Application Notes EO - offset error. Refer to Figure 1.
  The offset error (EO) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve.
- EG - gain error or the full-scale error voltage. Refer to Figure 1.
  The gain error (EG) is the difference between the straight line which fits the actual transfer curve after removing offset error and the straight line which fits the ideal transfer curve.
- EL - integral non-linearity. Refer to Figure 1.
  The integral non-linearity (EL) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors.
- ED - differential linearity error. Refer to Figure 1.
  The differential linearity error (ED) is the difference between the actual step width and the ideal step width.

To get best ADC accuracy, the application design applies methods to reduce above errors.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential linearity error (E_D).
(4) Integral non-linearity ($E_{L(adj)}$).
(5) Center of a step of the actual transfer curve.

Figure 1. LPC86x ADC static characteristic parameters

Below lists other factors affecting ADC accuracy in application:

- Power stability and noise
- Reference voltage stability
- Digital and analog part isolation in system
- ADC input impedance matching with outside circuit impedance
- PCB layout with EMI and EMC problems

3 ADC usage for LPC86x

3.1 Hardware self-calibration

The A/D converter includes a built-in, hardware self-calibration mode. To achieve the specified ADC accuracy, recalibrate the A/D converter, at a minimum, following every chip reset before initiating normal ADC operation.

A calibration cycle requires approximately 290 µs to complete. While calibration is in progress, normal ADC conversions cannot be launched, and the ADC Control Register must not be written. For detailed usage, see the LPC86x UM.

3.2 ADC design note related with ADC performance

When using LPC86x ADC, for best performance, select VREFP and VREFN at the same voltage level as VDD and VSS. When selecting VREFP and VREFN different from VDD and VSS, make sure that the voltage midpoints are the same:

$$\frac{\text{VREFP - VREFN}}{2} + \text{VREFN} = \frac{VDD}{2} \quad (1)$$

3.3 ADC pin configuration

To get accurate voltage readings on the monitored pin, select the ADC function via the switch matrix registers.

The MODE bits in the IOCON register must disable both pullup and pulldown resistors.

For a pin hosting an ADC input, it is not possible to have a digital function selected, because an inside circuit disconnects ADC hardware from the associated pin whenever a digital function is selected on that pin.

3.4 Analog source impedance match

In some applications, to control the power consumption, in the ADC sample circuit which connects to ADC pin, use resisters with value above 100 kΩ. LPC86x has minimum input impedance about 100 kΩ when ADC applies the maximum convert speed (1.9 M samples/s for LPC86x). In this case, consider the ADC pin input impedance for input voltage measurement.

Figure 2 gives an example for typical ADC sampling circuit.

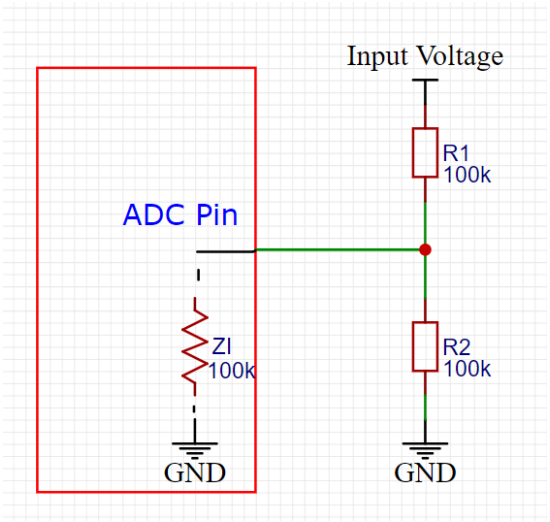


Figure 2. ADC pin analog source impedance match

In this application, when ADC apply Maximum convert speed, the voltage in ADC pin is not the half but one-third of Input voltage. Designer should take care of this effect in their sample circuit design.

The other characteristic for ADC input impedance is that the input impedance is inversely proportional to convert speed. If user application does not require high-speed ADC convert, we can slow down the ADC convert speed. For example, to get input impedance increase by 10 times, slow the ADC convert by 10 times. This can eliminate the effect caused by ADC pin input impedance mostly. Perform this operation by configuring CLKDIV bits in CTRL register for ADC module.

4 Methods to improve ADC accuracy

4.1 Software processing to improve ADC accuracy

4.1.1 Oversampling with averaging to increase ADC accuracy

During the input signal sampling, when a white noise happens to the input signal, ADC result loses its accuracy. To eliminate this white noise, over sample the input signals and give an averaging arithmetic processing to the ADC result. This method has efficient help to deal with white noise interference.

4.1.2 Zero voltage pre-sampling to deal with offset error (EO)

The offset error is same for each analog-to-digital conversion. To eliminate the offset error, perform the zero voltage pre-sampling.

Before analog-to-digital conversion, do a conversion for 0 voltage. Keep value in memory. To eliminate the offset error, in afterward conversion, minus the result of 0 voltage in memory with each conversion result.

4.2 Hardware processing to improve ADC accuracy

To make the ADC achieve the best accuracy, properly design and configure the entire system. The basic hardware processing is to separate the analog and digital layouts, including isolating the grounds by different PCB planes, avoiding analog/digital tracks crossing each other, and using different power supply. In some case, to eliminate the high-frequent noise, add an external RC filter in ADC circuit.

The following section provides some suggestions on PCB layout, system power decoupling, and analog/digital grounding.

4.2.1 ADC pins processing

PCB trace length for ADC pins must be as short as possible. In practical application design, fully consider the influence of parasitic parameters on PCB traces for ADC pins.

Some digital signal lines locate among the analog pins. If possible, do not select these digital pins.

Input filters connected to the ADC have a significant impact on the noise immunity of the analog parts. The type of the filters to be used depends on the input signal frequency. The location of the filter capacitors is also very important. Place the filter capacitors onto the same (analog) subground plane.

4.2.2 Decoupling system power supply

Using electrolytic capacitors near the power source input of PCB and ceramic capacitors next to the power pins of the microcontroller, put a 0.1 µF to filter high frequency noise and a 100 µF to filter low frequency noise. The capacitors must as close as possible to the power pins and place the two capacitors between each pair of power pins.

By using thicker traces to the power supply of the microcontroller, its inductive impedance is lowered, thus effectively reducing noise emissions. Due to the power line emissions, to decrease crosstalk, separate power lines from signal lines.

Figure 3 shows an example for decoupling capacitors placement. C4 is for filtering low frequency noise. C5, C6, C7, C8, and C9 are for filtering high frequency noise.

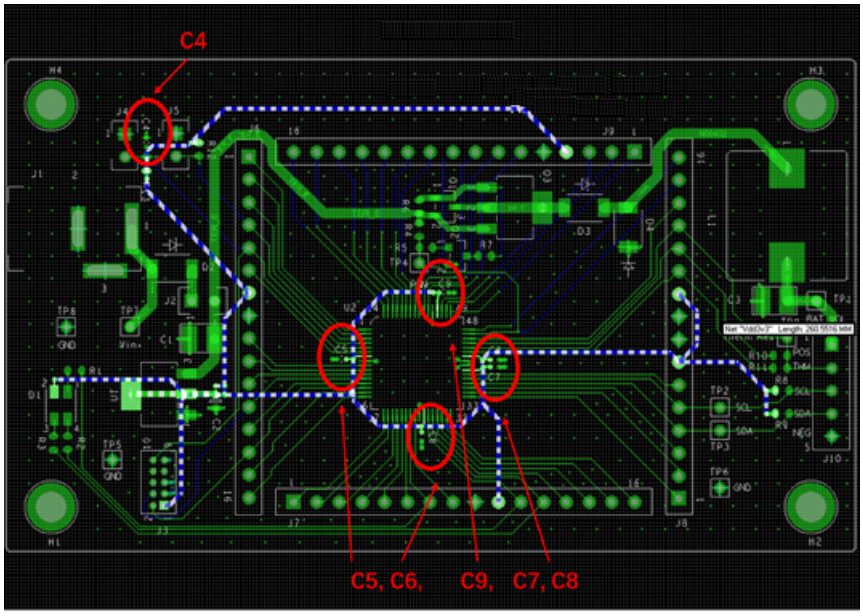


Figure 3. An example for decoupling capacitors placement

4.2.3 Analog/digital grounding

Reduce the noise on the power and ground lines as much as possible. To decrease the noise, segment the ground plane into the digital and analog domains. These planes are physically separated by a small gap and connected only at one point that is a few millimeters in size.

LPC86x contains some package for LPC86x, such as, LPC86x 48/64 LQFP package. The VDDA/VSSA is separated from VDD/VSS. To connect the digital part and the analog part to the same power supply, use a small inductor or magnetic bead.

Use a ground plane to isolate noisy digital components from analog components, and analog ground to surround analog signals when routing.

5 Revision history

Table 1 summarizes the revisions to this document.

Table 1. Revision history

Revision number	Date	Substantive changes
0	08 May 2023	Initial release

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