

AN13905

ACMP Usage for LPC86x

Rev. 0 — 8 May 2023

Application note

Document Information

| Information | Content |
|-------------|---|
| Keywords | LPC86x, ACMP, Voltage monitor, Pulse-width measurement |
| Abstract | This application note introduces and provides the usage note for the ACMP module of LPC86x. |



1 Introduction

LPC86x series contain an ACMP (Analog Comparator) module. This application note introduces and provides the usage note for the ACMP module of LPC86x.

2 General function of ACMP

ACMP is a module that compares two analog input voltages and outputs a signal level indicating which of the inputs is greater or lesser.

Typically an analog comparator compares voltage levels on two inputs and gives digital output based on the comparison. When the voltage on the positive input (V_A) is greater than the voltage on the negative input (V_B), the output voltage (V_{OUT}) is same as its positive supply (V_+). Otherwise, the output is as its negative supply (V_-). Usually, the ACMP module uses VDD as its positive supply, while GND as its negative supply.

Figure 1 shows an ideal behavior of ACMP.

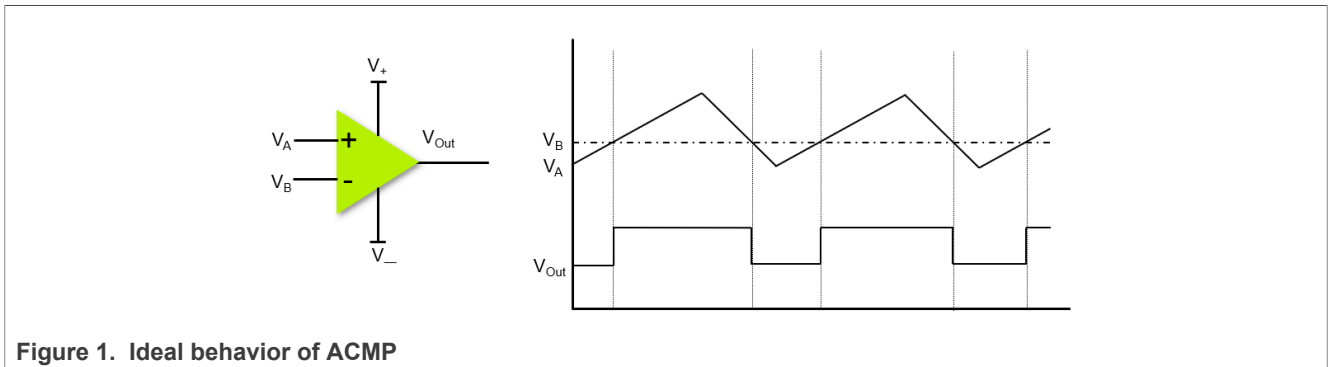


Figure 1. Ideal behavior of ACMP

3 LPC86x ACMP introduction and diagram

3.1 LPC86x ACMP introduction

LPC86x ACMP consists of four parts:

- Voltage ladder
- Input mux
- Analog comparator
- Output mux

3.1.1 ACMP voltage ladder

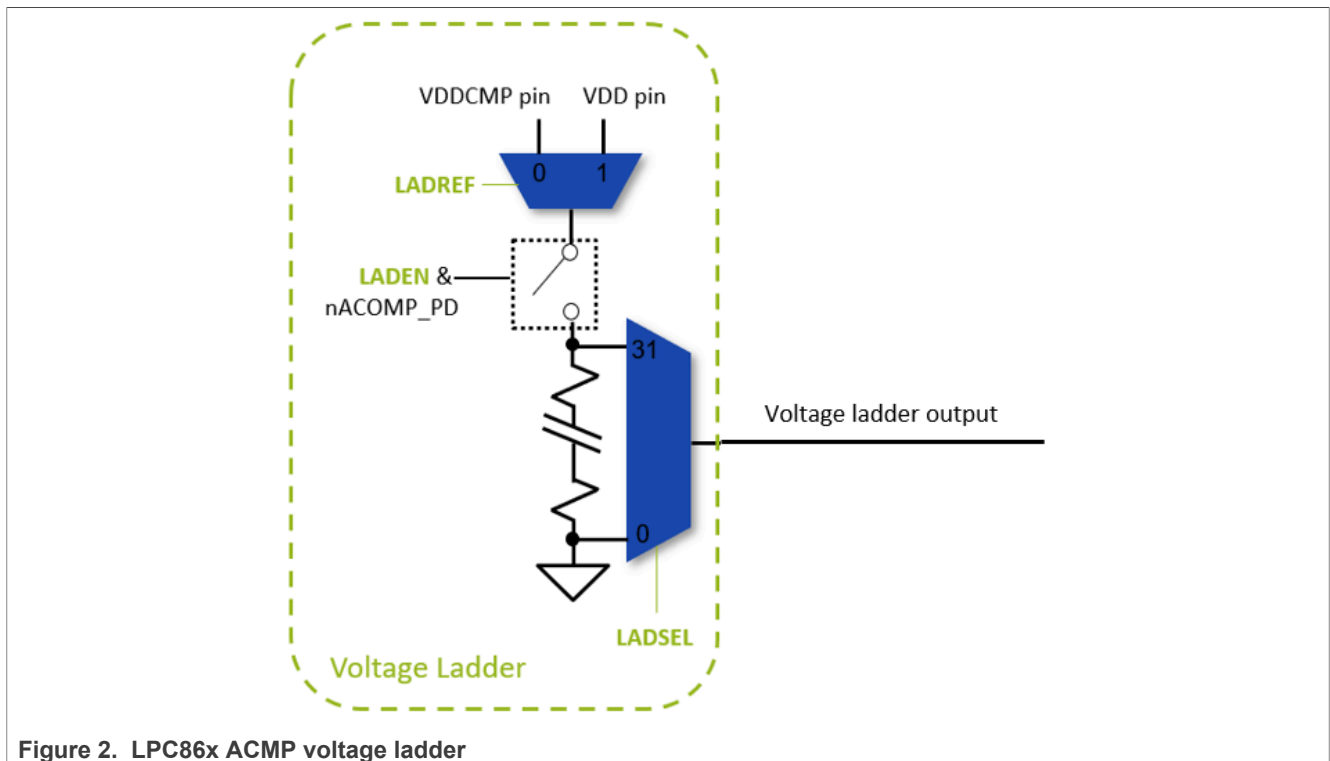


Figure 2. LPC86x ACMP voltage ladder

The ACMP voltage ladder can use two reference voltages, from the VDDCMP pin or the VDD pin. The voltage ladder selects one of 32 steps between the reference voltage and VSS inclusive. The voltage on VDDCMP must not exceed that on VDD.

Voltage ladder can be separately powered down for applications only requiring the comparator function to save the chip power consumption.

3.1.2 ACMP input mux

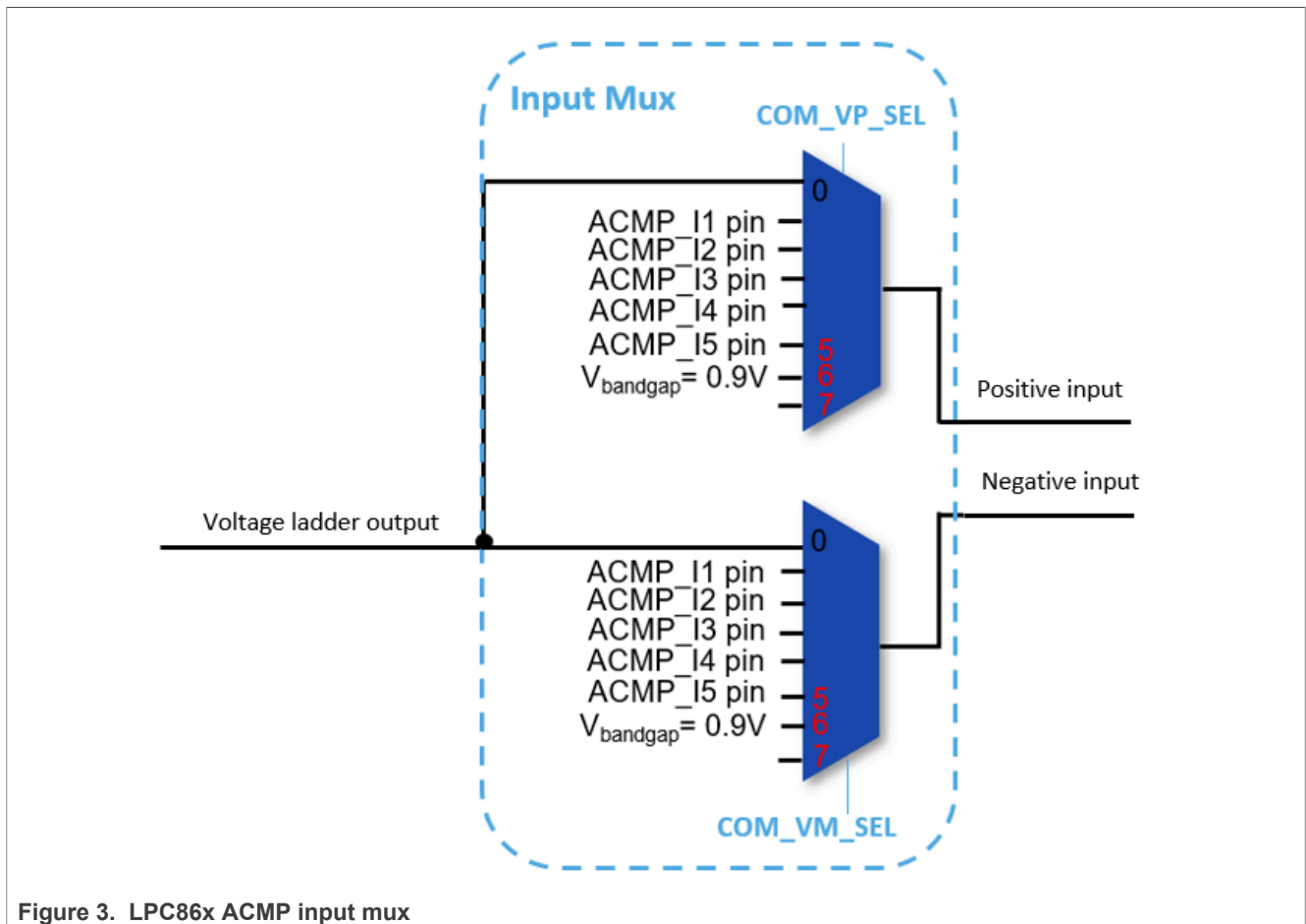


Figure 3. LPC86x ACMP input mux

LPC86x ACMP positive input and negative input can use seven input sources:

- Voltage ladder output
- ACMP_{Ix} (1 - 5)
- Band gap (Internal reference voltage 0.9 V)

3.1.3 ACMP analog comparator

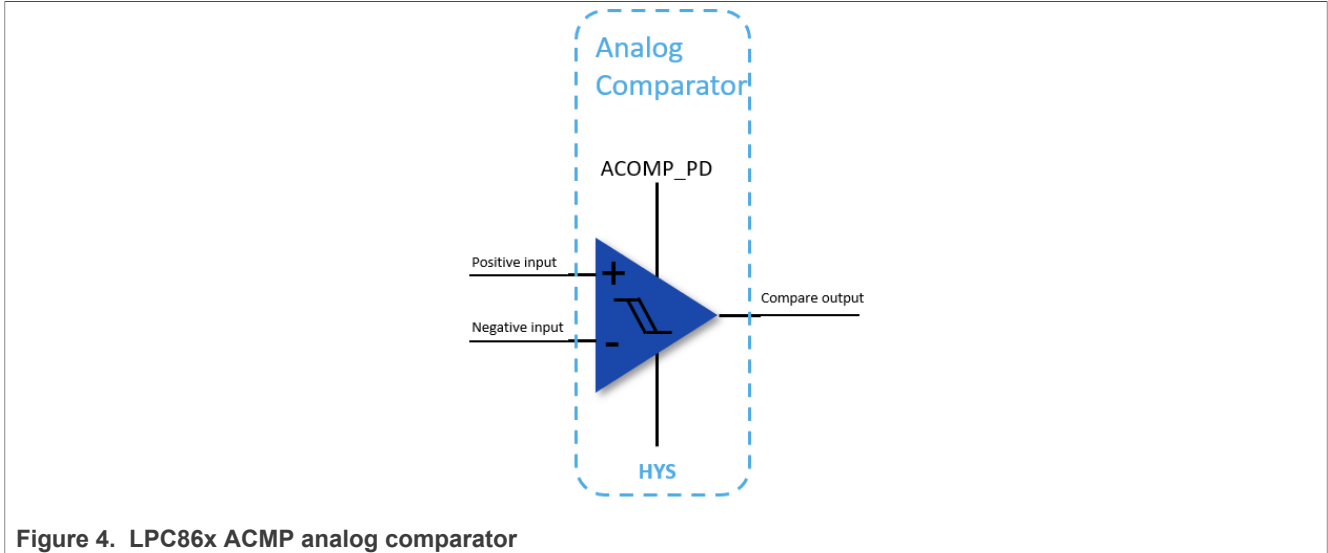


Figure 4. LPC86x ACMP analog comparator

The analog comparator compares the positive input and negative input, and gets the compare output.

User can enable or disable ACMP by controlling the PDRUNCFG register ACOMP bit, and setting the different hysteresis voltage here.

3.1.4 ACMP output mux

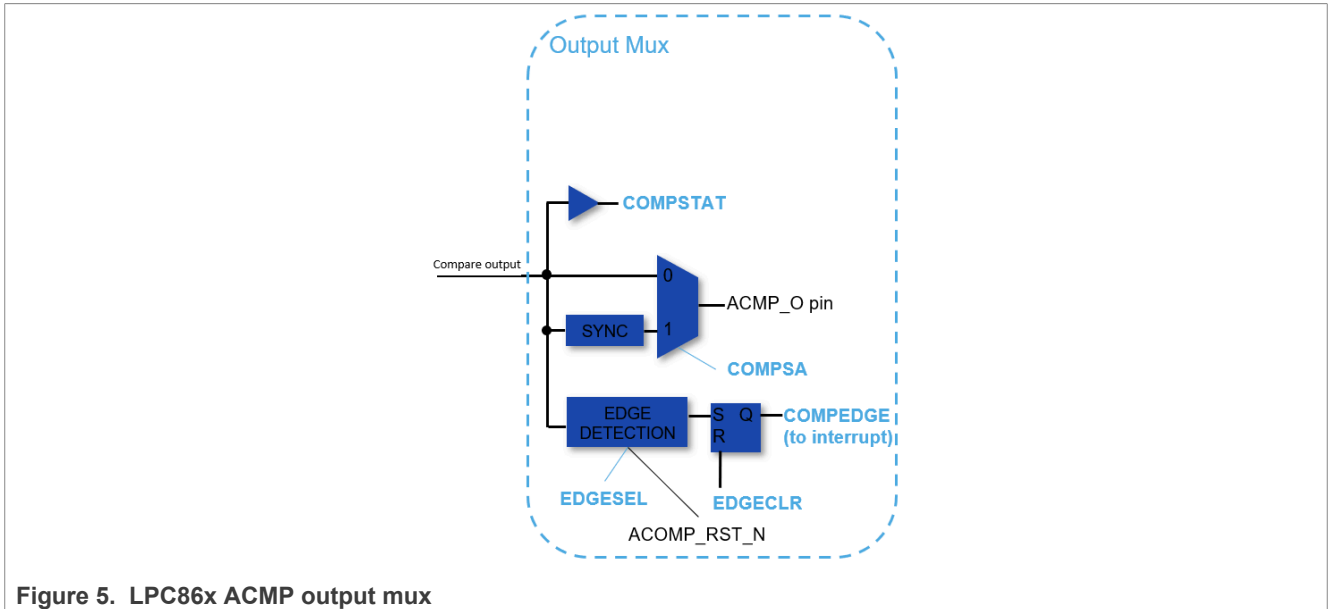


Figure 5. LPC86x ACMP output mux

The ACMP analog comparator output goes to a selected pin and causes an edge detected interrupt. The interrupt output is connected to NVIC.

One comparator output is internally collected to the ADC trigger input multiplexer.

Compare completed indicates that the ACMP status is completed.

3.2 LPC86x ACMP diagram

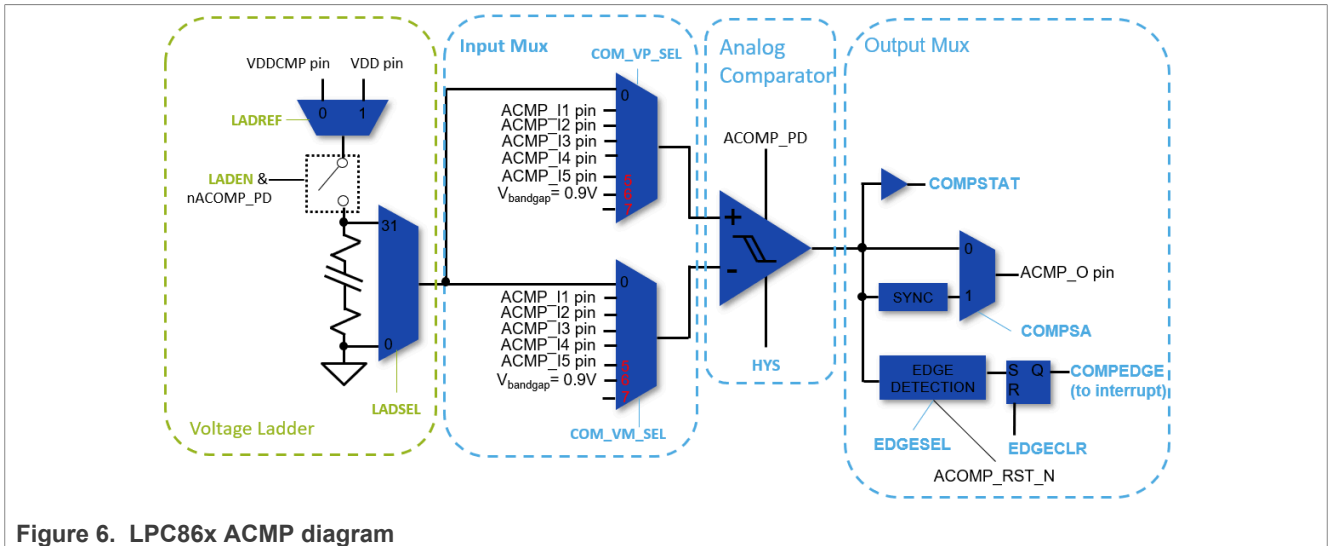


Figure 6. LPC86x ACMP diagram

The above four parts form the entire LPC86x ACMP diagram.

4 LPC86x ACMP pin description

LPC86x ACMP contains three kinds of pins:

- Input – ACMP_Ix
- Output – ACMP_O
- Reference voltage – VDDCMP

The input pins and reference voltage pins are fixed-pins. They must be enabled through the switch matrix and can only be assigned to special pins on the package.

The output pins are movable-pins. It can be assigned to any pin on the LPC86x package through the switch matrix.

[Table 1](#) describes the ACMP pins.

Table 1. LPC86x ACMP pins description

| Function | Type | Pin | Description | SWM register |
|----------|------|---------|--|--------------|
| ACMP_I1 | I | PIO0_0 | Comparator input 1 | PINENABLE0 |
| ACMP_I2 | I | PIO0_1 | Comparator input 2 | PINENABLE0 |
| ACMP_I3 | I | PIO0_14 | Comparator input 3 | PINENABLE0 |
| ACMP_I4 | I | PIO0_23 | Comparator input 4 | PINENABLE0 |
| ACMP_I5 | I | PIO0_30 | Comparator input 5 | PINENABLE0 |
| ACMP_O | O | any | Comparator output | PINASSIGN11 |
| VDDCMP | I | PIO0_6 | External reference voltage source for 32-stage Voltage Ladder. | PINENABLE0 |

5 LPC86x ACMP non-ideal behavior characteristics

LPC86x ACMP has below non-ideal behavior characteristics:

- Offset voltage
- Propagation delay
- Hysteresis offset

5.1 Offset voltage

Offset voltage is the output voltage offset when both inputs are equal. The ideal behavior must be 0 when both inputs are equal. [Figure 7](#) shows the LPC86x ACMP offset voltage.

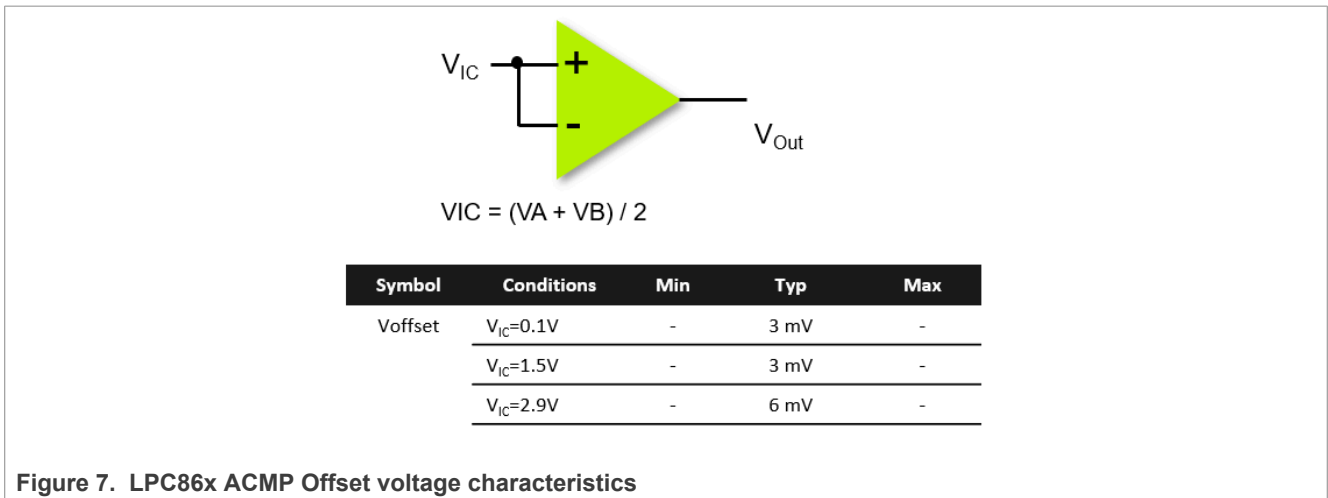


Figure 7. LPC86x ACMP Offset voltage characteristics

5.2 Propagation delay

Propagation delay is the time needed to establish the output. This delay is defined as the duration between the moment that the input signal crosses the threshold and the moment that the output state changes (usually when the output reaches 50 % of VDD). [Figure 8](#) shows the example for the propagation delay.

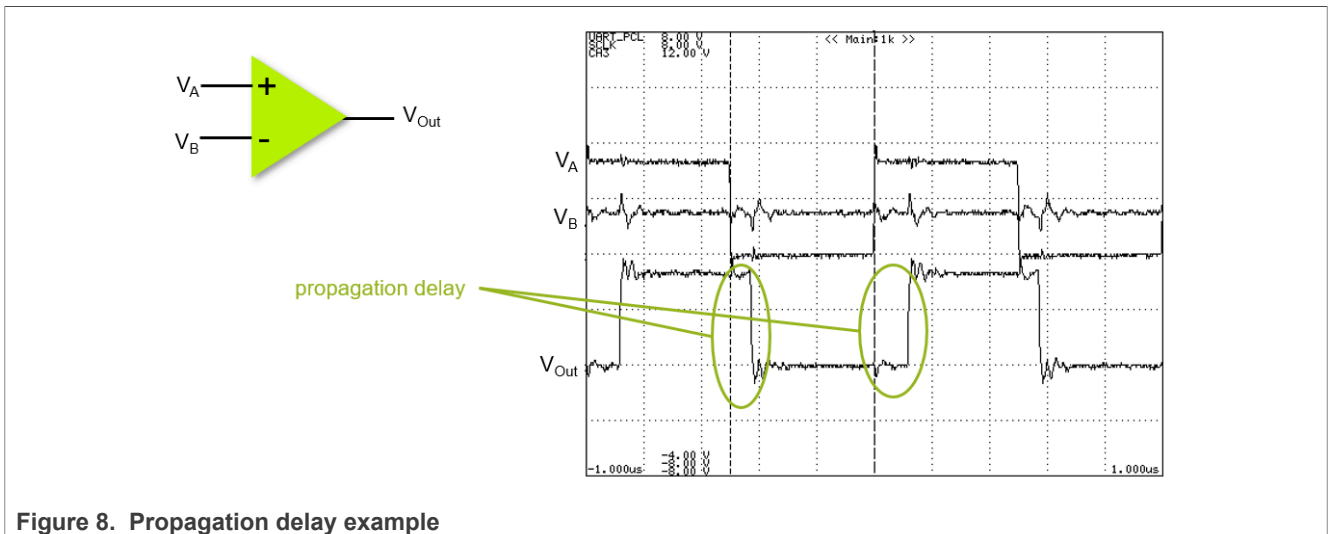


Figure 8. Propagation delay example

The Propagation delay time between rising and falling edge is unsymmetrical.

Figure 9 shows the LPC86x ACMP propagation delay characteristics.

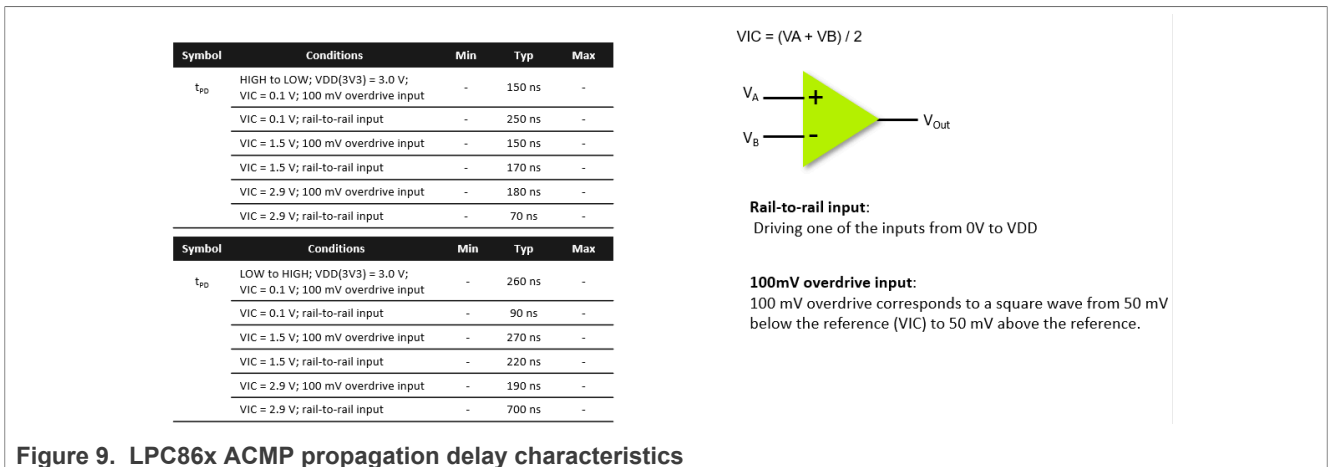


Figure 9. LPC86x ACMP propagation delay characteristics

5.3 Hysteresis offset

In ideal status, when the voltage on the positive input (VA) is greater or lesser than the voltage on the negative input (VB), the output voltage (VOUT) changes. In this case, the input signal crosses threshold cannot be set or the cross threshold equals to zero. While in some applications, the zero threshold causes system unstable, for example, the vibration existing around the zero threshold. Therefore, introducing hysteresis offset is an often-effective solution to these situations.

Figure 10 shows the example for the Hysteresis offset.

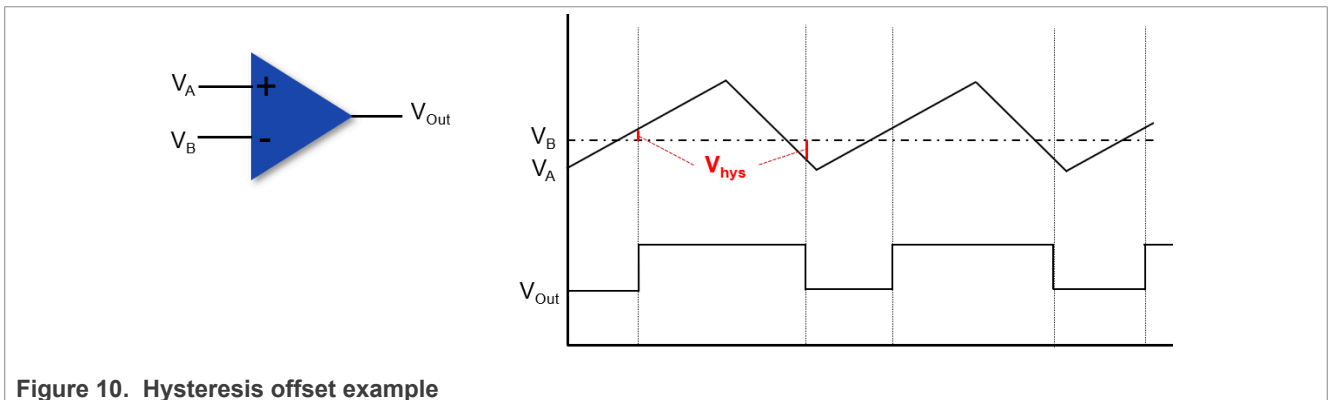


Figure 10. Hysteresis offset example

The LPC86x ACMP has four choices for ideal hysteresis offset: 5 mV, 10 mV, 20 mV, or none.

The measured hysteresis has a bit of offset voltage compared to the ideal one. The Positive hysteresis is a little different from the negative hysteresis.

Figure 11 shows LPC86x ACMP hysteresis offset characteristics.

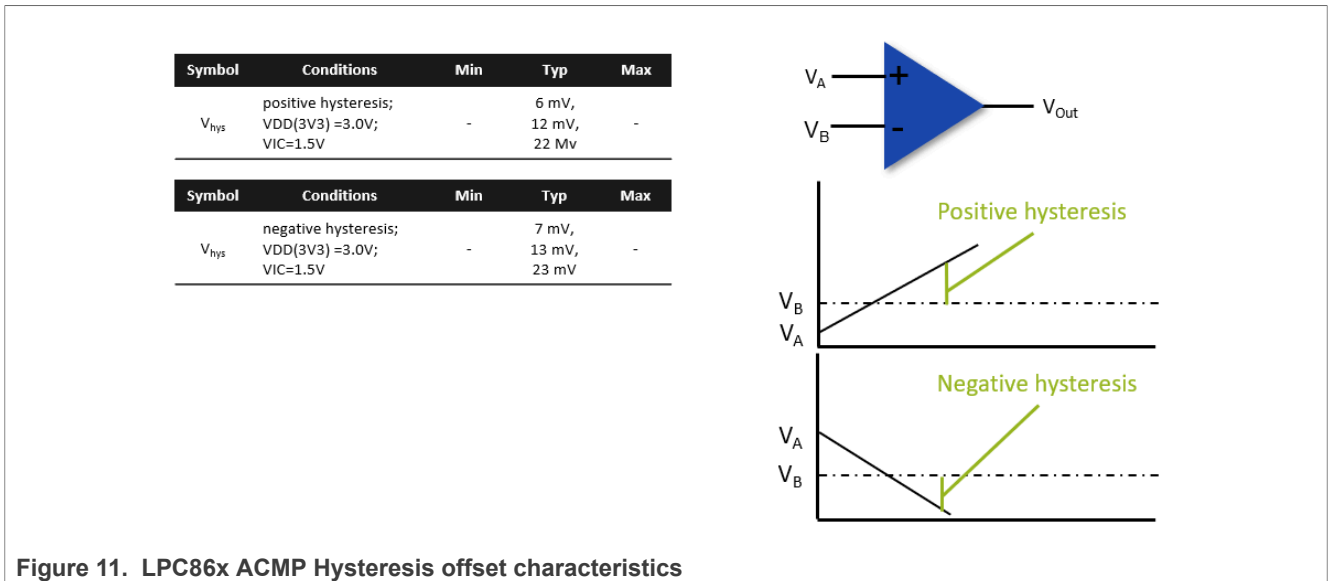


Figure 11. LPC86x ACMP Hysteresis offset characteristics

6 LPC86x ACMP basic configuration

To configure the LPC86x ACMP, perform the following steps:

- In the SYSAHBCLKCTRL register, set bit 19 to enable the clock to the register interface.
- Enable or disable the power to the analog comparator through the PDRUNCFG register.
- Clear the analog comparator peripheral reset using the PRESETCTRL register
- Connect the analog comparator interrupt to interrupt #11 in the NVIC.
- Configure the analog comparator pin functions through the switch matrix.

7 Application examples

7.1 Analog voltage monitoring

Using basic ACMP function, user can apply analog voltage monitoring, positive input as the monitored voltage and negative input as threshold voltage. When the voltage on the positive input (V_A) is greater or lesser than the voltage on the negative input (V_B), the output voltage (V_{OUT}) is changed, and V_{OUT} can connect to chip ADC or GPIO INT to take reaction from controller.

[Figure 12](#) shows the circuit example.

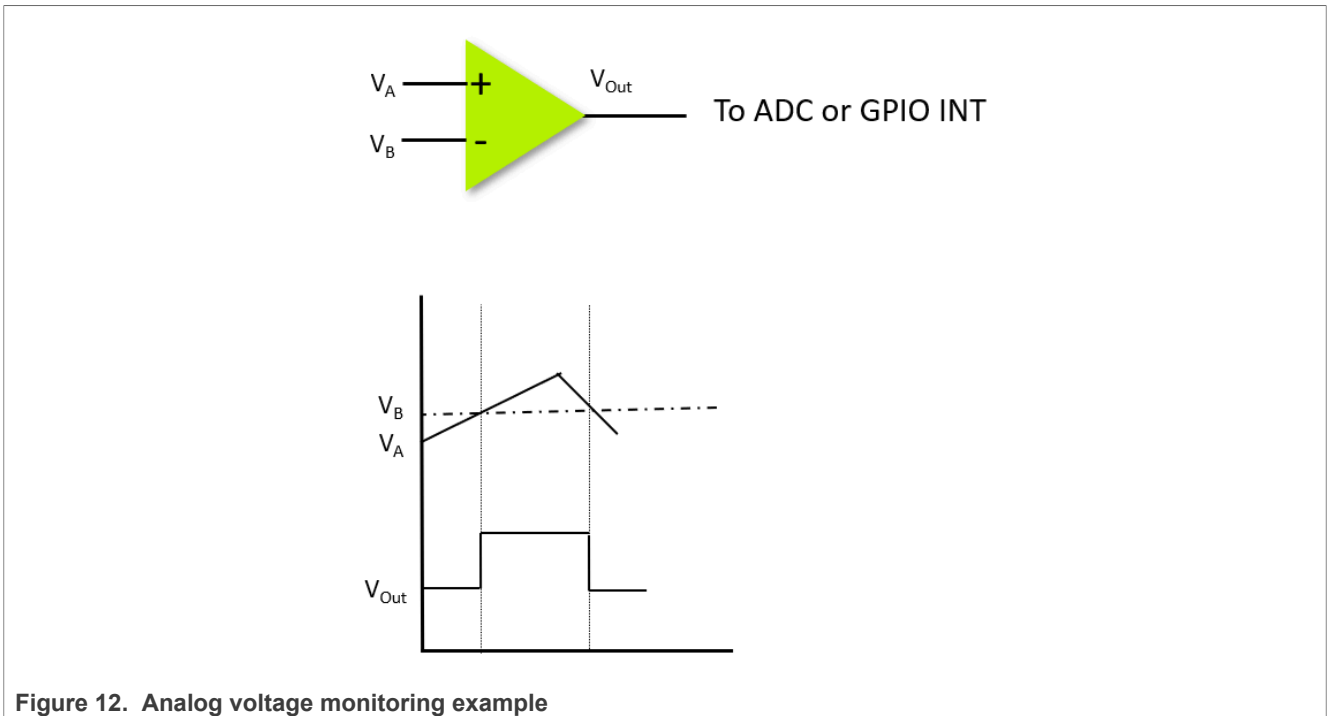


Figure 12. Analog voltage monitoring example

7.2 Pulse-width measurement

The width of a pulse can be measured using the comparator plus a timer. To implement this application, connect an external or internal reference voltage to the negative input (V_B) and connect the pulse signal to the positive input (V_A). When V_A exceeds V_B , the output becomes high and generates a rising edge on the timer input capture, triggering the timer start counting. The timer continues the counting until the output becomes low to generate a falling edge due to V_A becomes less than V_B . With this method, the time elapsed between the two consecutive captures represents the pulse width.

[Figure 13](#) shows the circuit example.

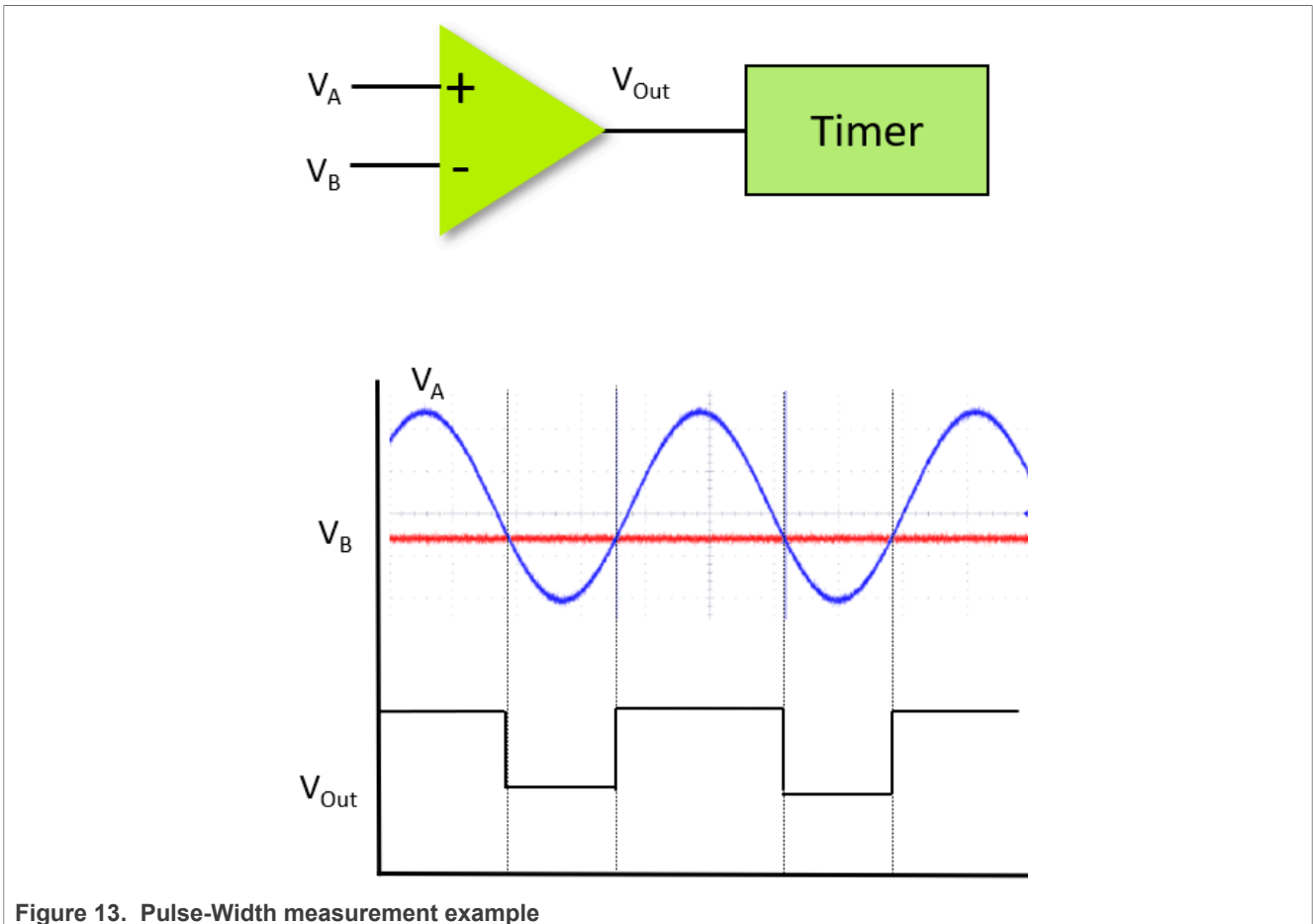


Figure 13. Pulse-Width measurement example

7.3 Using LPC86x ACMP as 5-bit ADC

When LPC86x is used in some applications which get LPC86x ADC resource limited, we can take advantage of the ACMP Voltage Ladder property and make one 5-bit ADC.

[Figure 14](#) shows the circuit example.

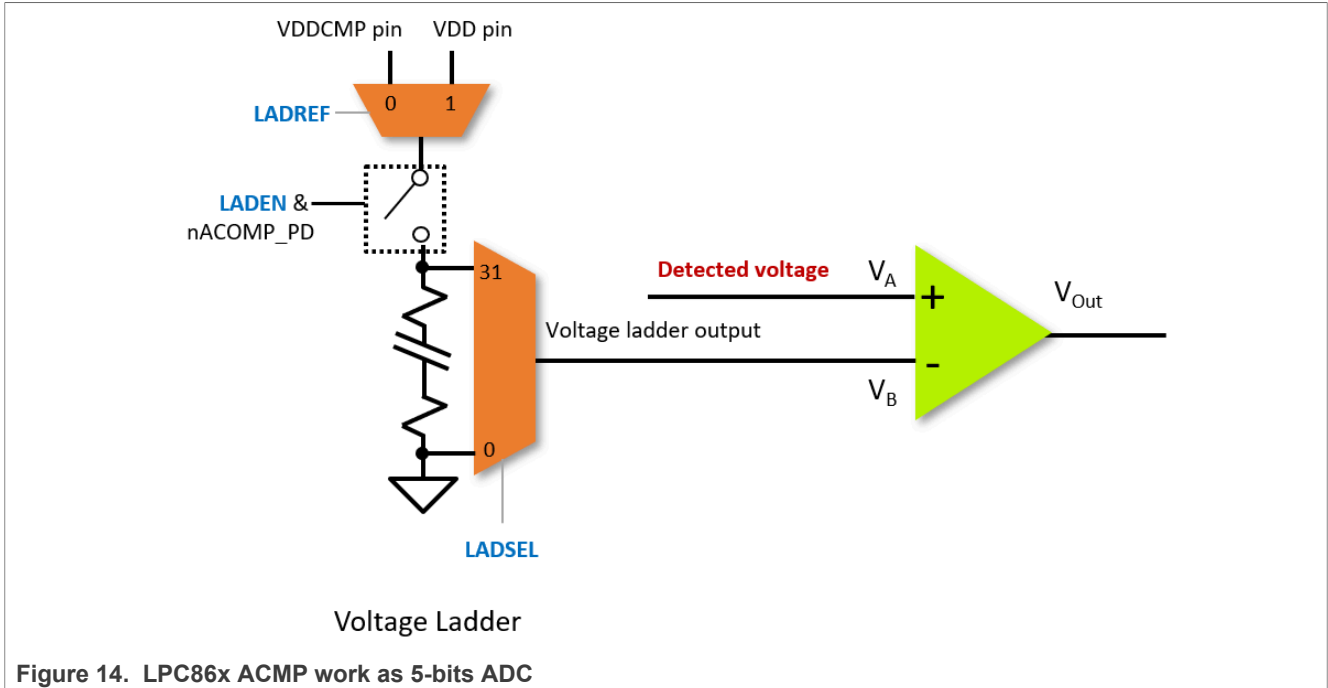


Figure 14. LPC86x ACMP work as 5-bits ADC

For example, using VDD = 3.1 V as Voltage Ladder Vref, considering voltage ladder value from 00000 to 11111, can get each step stands for $3.1 \text{ v} / 31 = 0.1 \text{ v}$. When the detected voltage equal to 0.15 v, using 11111 (3.1 v) to compare with it causes low ACMP output, and using 11110 (3.0 v) to compare with it also causes low ACMP output low. Try each step, and only using 00001 (0.1 v) to compare with it causes high ACMP output. Therefore, the detected voltage is judged between 0.1 v and 0.2 v. It makes the ACMP work as a 5-bit ADC.

Because this method uses each step to compare with detected voltage, the convert speed is limited and user can take some SW algorithm to raise the convert speed. For example, to speed up the comparison process, use the median algorithm of the software. Perform the first comparison with the middle step value of total steps, then the middle step value of the left steps, and so on.

8 Revision history

[Table 2](#) summarizes the revisions to this document.

Table 2. Revision history

| Revision number | Date | Substantive changes |
|-----------------|-------------|---------------------|
| 0 | 08 May 2023 | Initial release |

9 Legal information

9.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

9.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. - NXP B.V. is not an operating company and it does not distribute or sell products.

9.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

| | | |
|----------|---|-----------|
| 1 | Introduction | 2 |
| 2 | General function of ACMP | 2 |
| 3 | LPC86x ACMP introduction and diagram | 2 |
| 3.1 | LPC86x ACMP introduction | 2 |
| 3.1.1 | ACMP voltage ladder | 3 |
| 3.1.2 | ACMP input mux | 4 |
| 3.1.3 | ACMP analog comparator | 5 |
| 3.1.4 | ACMP output mux | 5 |
| 3.2 | LPC86x ACMP diagram | 6 |
| 4 | LPC86x ACMP pin description | 6 |
| 5 | LPC86x ACMP non-ideal behavior characteristics | 7 |
| 5.1 | Offset voltage | 7 |
| 5.2 | Propagation delay | 7 |
| 5.3 | Hysteresis offset | 8 |
| 6 | LPC86x ACMP basic configuration | 9 |
| 7 | Application examples | 9 |
| 7.1 | Analog voltage monitoring | 9 |
| 7.2 | Pulse-width measurement | 10 |
| 7.3 | Using LPC86x ACMP as 5-bit ADC | 11 |
| 8 | Revision history | 12 |
| 9 | Legal information | 13 |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.
