AN13591

FlexSPI CoreMark Performance on LPC553x/LPC55S3x

Rev. 3 — 20 September 2023 Application note

Document Information

Information	Content
Keywords	AN13591, FlexSPI, CoreMark, Octal NOR flash, LPC553x, LPC55S3x, CoreMark performance
Abstract	This document emphasizes on how to port CoreMark project and run on external FlexSPI interface, including octal NOR flash and HyperRAM. It provides test results of FlexSPI CoreMark performance data.

1 Introduction

CoreMark of EEMBC is a benchmark that measures the performance of microcontrollers (MCUs) and Central Processing Units (CPUs) used in embedded systems. It implements the following algorithms:

- List processing (find and sort)
- Matrix manipulation (common matrix operations)
- State machine (determines whether an input stream contains valid numbers)
- Cyclic redundancy check (CRC)

FlexSPI is a new peripheral for the LPC553x/LPC55S3x series. It expends code of application and data size. It brings opportunities of many new application designs.

This document emphasizes on how to port a CoreMark project and run on an external FlexSPI interface, including octal NOR flash and HyperRAM. It provides test results of FlexSPI CoreMark performance data.

Note:

Two prerequisite application notes are listed here:

1. *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide (document AN13579).*
   This document guides how to port a CoreMark project on LPC553x/LPC55S3x and gives a comprehensive view of the key point when evaluating a CoreMark project.
2. *Programming and Booting Images from External NOR flash on LPC553x/LPC55S3x (document AN13543).*
   This document introduces how to create an external NOR flash image and how to boot the image from external NOR flash.

This document heavily reuses the two application notes. If you are not familiar with basic knowledge related to FlexSPI or CoreMark, read them first.

2 Porting CoreMark project to FlexSPI external memory

The difference between a normal internal flash image and a FlexSPI image is the code space address. Because the FlexSPI AHB address space started is `0x0800_0000`. Boot ROM defines that any FlexSPI image code execution address starts at `0x0800_1000`. We must change the linker file of the CoreMark project.

2.1 Getting CoreMark demo source code

This document reuses a CoreMark demo source code package available with *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (Document AN13579). It provides a ready-to-use CoreMark project package for all three IDEs. For an original source code, the CoreMark data are running on internal flash and internal RAM. We recommend running the CoreMark demo first and getting familiar with the basic download process and hardware setup. Get the CoreMark result on internal flash/RAM. It provides a baseline score that can compare with FlexSPI external memory CoreMark data.

2.2 Changing code execution address

- **Keil**
  Switch the project configuration to `lpc55s3x_coremark_flash` configuration.

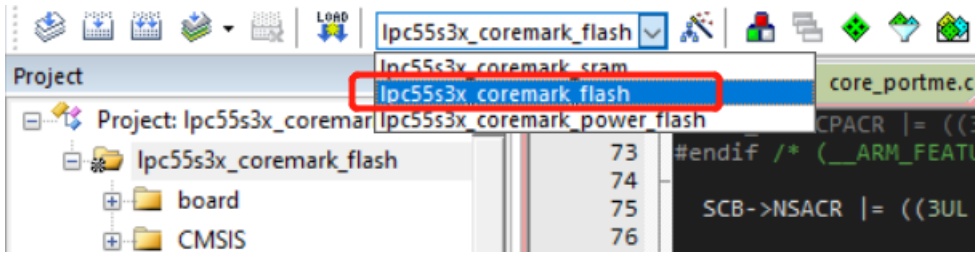


Figure 1. Switching to lpc55s3x_coremark_flash configuration

Change the linker file to set code space to start from `0x0800_1000`.

```
/* USB BDT size */
#define usb_bdt_size                    0x0
/* Sizes */
#define Stack_Size                      0x1000
#define Heap_Size                       0x1000

#define  m_interrupts_start             0x08001000
#define  m_interrupts_size              0x00000400

#define m_text_start                    0x08001400
#define m_text_size                     0x0003FC00

#define  m_data_start                   0x20000000
#define  m_data_size                    0x0001C000

#define  m_sramx_start                  0x04000000
#define  m_sramx_size                   0x00004000
```

Figure 2. Changing linker file in Keil

- **IAR**

  Switch the project configuration to `lpc55s3x_coremark_flash` configuration.

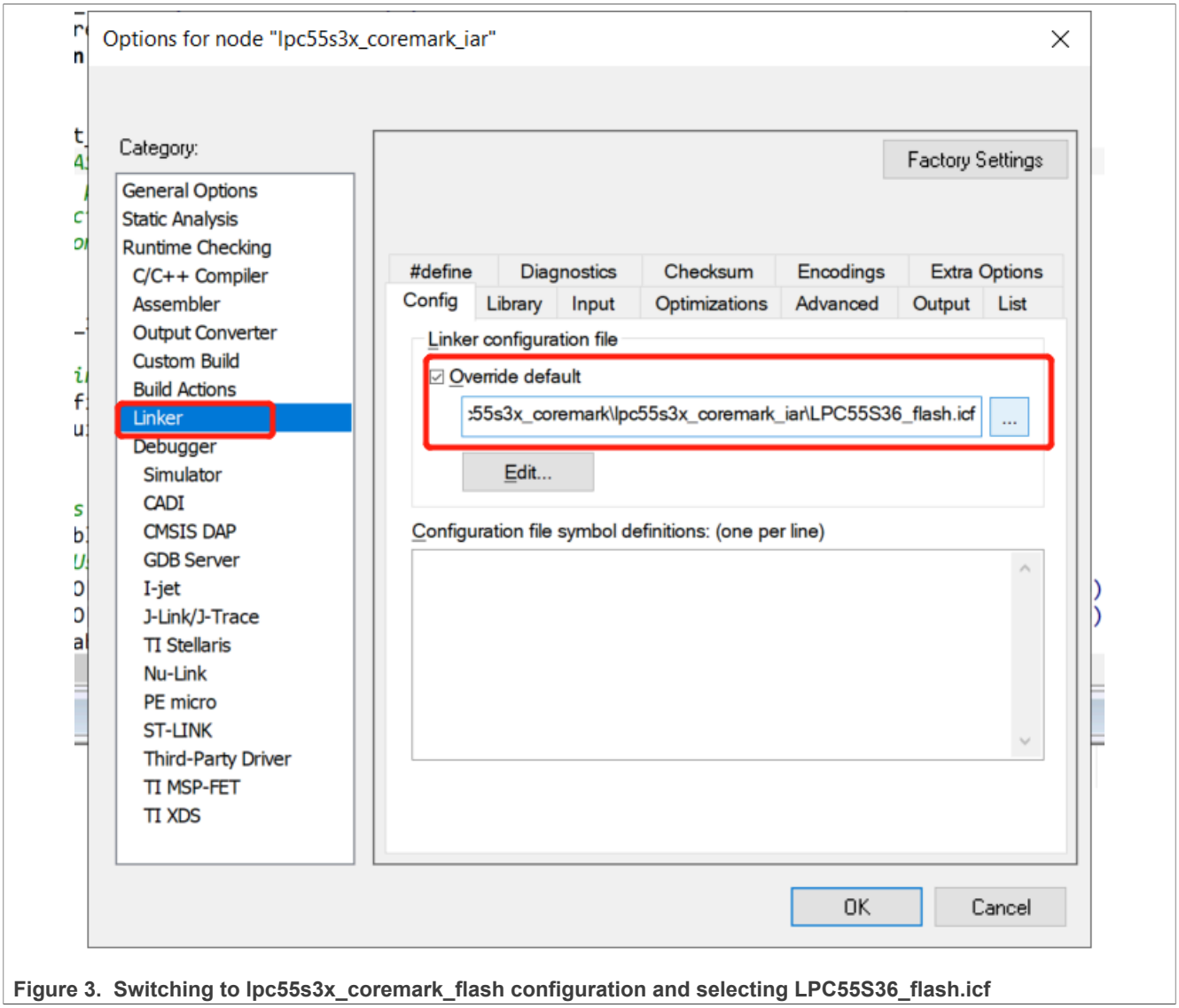


Figure 3. Switching to lpc55s3x_coremark_flash configuration and selecting LPC55S36_flash.icf

```
33
34  define symbol m_interrupts_start          = 0x08001000;
35  define symbol m_interrupts_end            = 0x080013FF;
36
37  define symbol m_text_start                = 0x08001400;
38  define symbol m_text_end                  = 0x0803FFFF;
39
40  define symbol m_data_start                = 0x20004400;
41  define symbol m_data_end                  = 0x20007FFF;
42
43  define symbol m_sramx_start               = 0x04000000;
44  define symbol m_sramx_end                 = 0x04003FFF;
45
```

Figure 4. Changing linker file in IAR

- **MCUX**
  Open **Property** > **C/C++ build** > **MCU Settings** and change flash location to `0x0800_1000`.

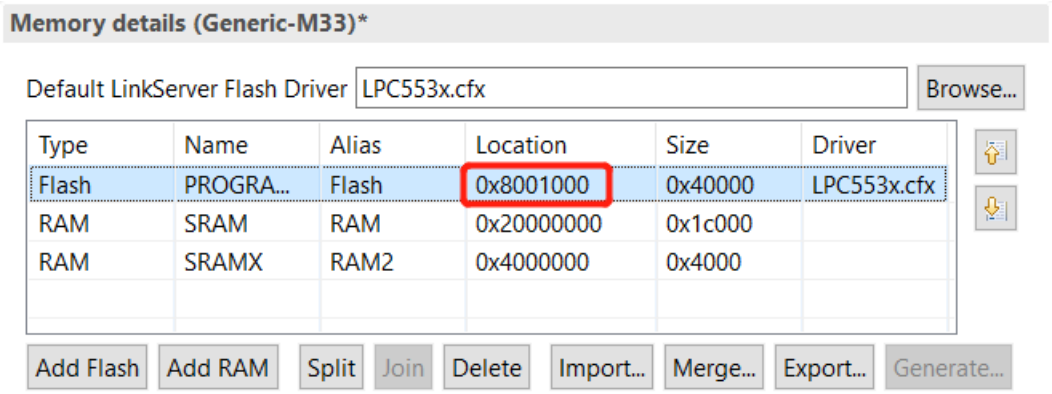


Figure 5. Changing linker file in MCUX

All other compile and download steps are the same as described in *Programming and Booting Images from External NOR flash on LPC553x/LPC55S3x* (document AN13543).

2.3 Enabling CACHE64

CACHE64 is a peripheral to accelerate FlexSPI performance. By default, CACHE64 is disabled. We must enable CACHE64.

```
cache64_config_t cacheCfg;

/* As cache depends on FlexSPI power and clock, cache must be initialized after FlexSPI power/clock is set */
CACHE64_GetDefaultConfig(&cacheCfg);
CACHE64_Init(CACHE64_POLSEL0, &cacheCfg);
```

Figure 6. Adding the CACHE64 init function in portable_init()

For more information about CACHE64, see *LPC55S36 Reference Manual*.

3 Coremark result (Octal Flash: MX25UM51345GXDI00)

- **Hardware**:
  - LPCXpresso55S36
  - External nor flash: MX25UM51345GXDI00
- **Internal Flash configuration**:
  - Cache enabled
  - Code in internal Flash
  - Data in SRAM
- **FlexSPI configuration**:
  - FlexSPI clock = FRO96M
  - CACHE64 enabled
  - Octal DDR mode
  - Code in external NOR flash
  - Data in SRAM
- IDE: All IDE optimization settings are the same as mentioned in *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (document AN13579).

Table 1. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 12 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	4.086	4.170	102 %
IAR	4.025	4.081	101 %
MCUX	2.964	2.971	101 %

Table 2. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 96 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.986	4.011	100 %
IAR	4.023	4.080	101 %
MCUX	2.956	2.952	100 %

Table 3. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 100 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.972	3.995	100 %
IAR	4.01	4.068	101 %
MCUX	2.945	2.938	99 %

Table 4. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 150 MHz

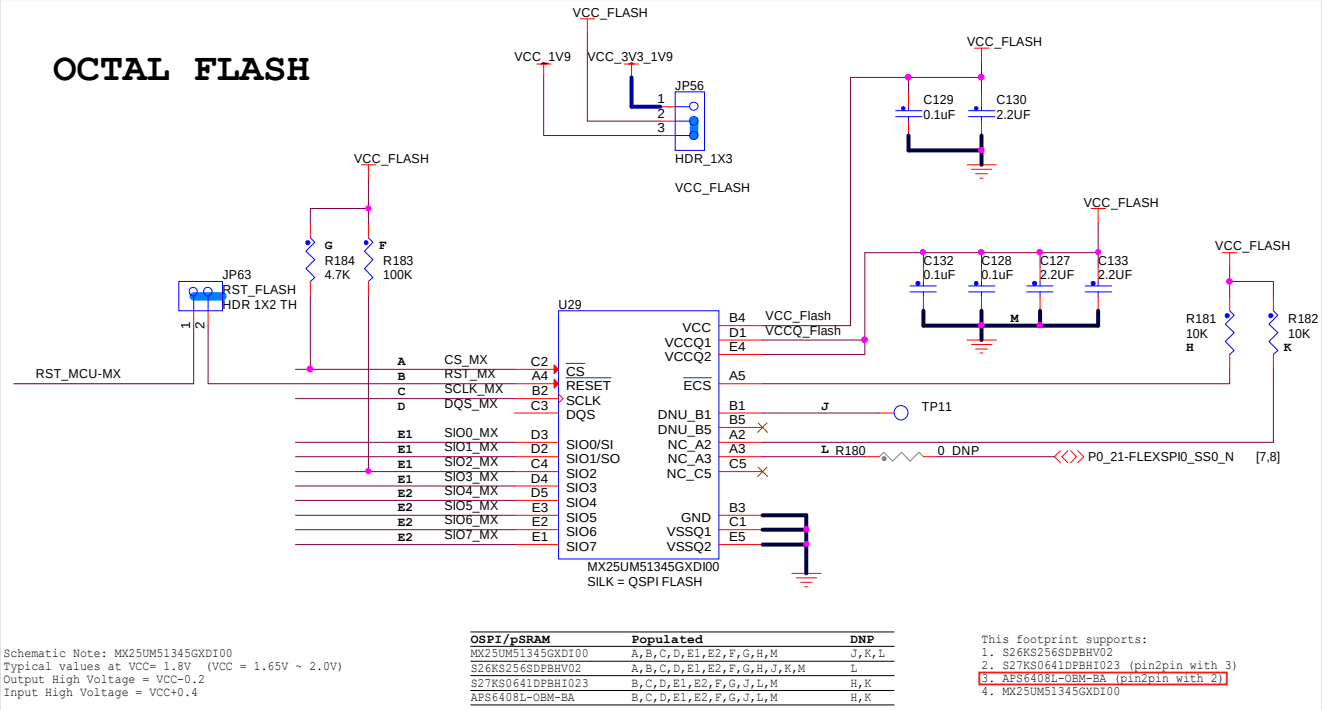
IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.905	3.874	99 %
IAR	4.004	4.062	101 %
MCUX	2.942	2.936	99 %

4 Coremark result (HyperRAM: W956D8MBYA5I)

By default, the FlexSPI is connected to octal NOR Flash on LPCXpresso55S36. Rework to enable HyperRAM. The LPCXpresso55S36 provides a rework guide on the schematic. The default configuration is for **4. MX25UM51345GXDI00**. Change resistor setting and align to **3. APS6408L-OBM-BA**. For HyperRAM, we choose **W956D8MBYA5I** of Winbond (same configurations as APS6408L).

As HyperRAM cannot save any code and data when power off, you must write a simple loader in internal flash that performs the below tasks:

1. Convert the CoreMark image into a C data array and copy to the image start address in FlexSPI space.
2. Jump to the start address and execute the image.



OSPI/pSRAM	Populated	DNP
MX25UM51345GXDI00	A,B,C,D,E1,E2,F,G,H,M	J,K,L
S26KS256SDPBHV02	A,B,C,D,E1,E2,F,G,H,J,K,M	L
S27KS0641DPBHI023	B,C,D,E1,E2,F,G,J,L,M	H,K
APS6408L-OBM-BA	B,C,D,E1,E2,F,G,J,L,M	H,K

Figure 7. Octal FlexSPI interface schematic for LPC553x/LPC55S3x

- **Hardware**:
  - LPCXpresso55S36 RevD
  - HyperRAM: W956D8MBYA5I
- **Internal Flash configuration**:
  - Cache enabled
  - Code in internal flash
  - Data in SRAM
- **FlexSPI configuration**:
  - FlexSPI clock = FRO96 M
  - CACHE64 enabled
  - Octal DDR mode
  - Code in HyperRAM
  - Data in SRAM
- IDE: IDE optimization setting is the same as mentioned in *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (document AN13579).

Table 5. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 12 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	4.086	4.173	102 %
IAR	4.025	4.041	100 %
MCUX	2.964	2.920	99 %

Table 6. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 96 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.986	3.991	100 %
IAR	4.023	4.010	99 %
MCUX	2.956	2.902	98 %

Table 7. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 100 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.972	3.971	100 %
IAR	4.01	4.039	100 %
MCUX	2.945	2.911	98 %

Table 8. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 150 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.905	3.842	98 %
IAR	4.004	4.049	101 %
MCUX	2.942	2.916	99 %

5 Conclusion

This application note extends the CoreMark project to FlexSPI external memory and gives a test result under different Core Clock configuration. Read this document as an extended version of *LPC553x CoreMark on Cortex-M33 Porting Guide* (document AN13579).

The FlexSPI NOR flash and HyperRAM CoreMark performance are similar to internal flash. There are limitless possibilities to extend the application code size without performance compromise.

6 Revision history

Section 6 summarizes the revisions to this document.

Table 9. Revision history

Revision Number	Release date	Description
3	20 September 2023	• Replaced "LPCXpresso55S36" with "LPCXpresso55S36 RevD" in Section 4 • Made some editorial changes
2	13 December 2022	Update reference of AN12284 with AN13579
1	26 May 2022	Replaced LPC553x with LPC553x/LPC55S3x
0	18 March 2022	Initial release

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