AN13571

Brushless DC (BLDC) Motor Control Demo on LPC553x/LPC55S3x

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Document information

Information	Content
Keywords	LPC553x/LPC55S3x processor, embedded systems, 3-phase BLDC motor control, Hall sensor, Arm Cortex-M33-based microcontrollers
Abstract	This application note describes the implementation of the 3-phase BLDC motor control with Hall sensor based on the NXP LPC553x/LPC55S3x processor.

1 Introduction

This application note describes the implementation of the 3-phase BLDC motor control with Hall sensor based on the NXP LPC553x/ LPC55S3x processor.

The LPC553x/LPC55S3x is an Arm Cortex-M33-based microcontroller for embedded applications. These devices include:

- Up to 256 kB on-chip flash
- Up to 128 kB of on-chip SRAM
- One SCTimer/PWM
- Eight flexible serial communication peripherals, which can be configured as a USART, SPI, high-speed SPI, I2C, or I2S interface
- Two 16-bit 2.0 Msamples/sec (12-bit 3.3 Msamples/sec) ADCs capable of four simultaneous conversions
- Four comparators
- Two temperature sensors
- Three 12-bit 1 Msample/sec DACs
- Three OpAmps
- Two FlexPWM timers

The Arm Cortex-M33 provides a security foundation, offering isolation to protect valuable IP and data with TrustZone technology. It simplifies the design and software development of digital signal control systems with the integrated Digital Signal Processing (DSP) instructions.

This application note introduces the principle of BLDC six-step control with hall sensor, hardware, and software implementation, including a detailed peripheral setup and driver description.

2 LPC553x/LPC55S3x features and advantages

The LPC553x/LPC55S3x is an Arm Cortex-M33-based microcontroller for embedded applications. The Arm Cortex-33 provides a security foundation, offering isolation to protect valuable IP and data with TrustZone technology. It simplifies the design and software development of digital signal control systems with the integrated DSP instructions. To support security requirements, the LPC553x/LPC55S3x supports secure boot, Advanced Encryption Standard (AES), Rivest Shamir Adleman (RSA), Universal Unique Identifier (UUID), Device Identifier Composition Engine (DICE), dynamic encrypt and decrypt, debug authentication, and TBSA compliance. Figure 1 shows the feature.

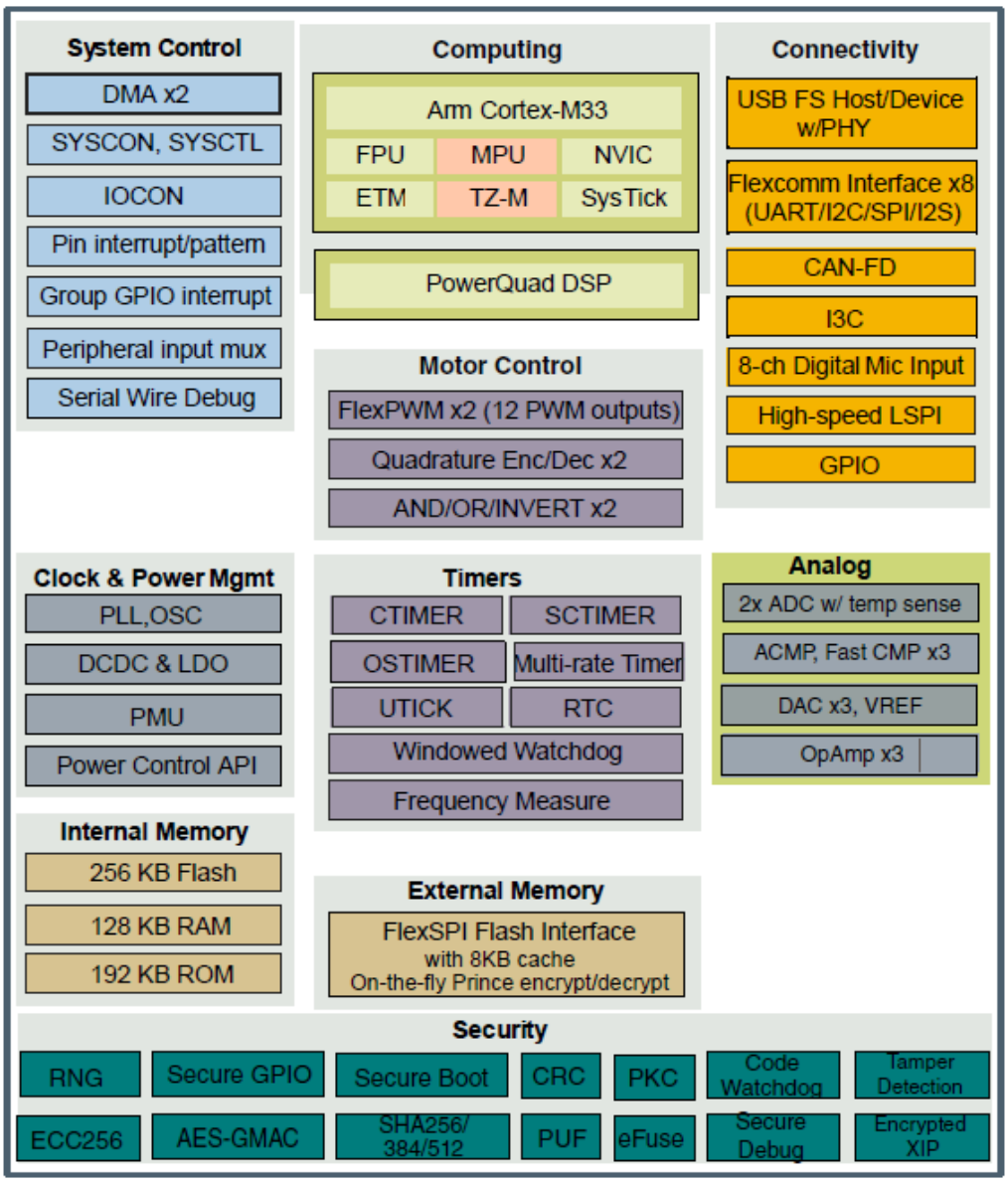

Figure 1. Features overview of LPC553x/LPC55S3x

For BLDC motor control, the advantages of LPC553x/LPC55S3x are:

- Multi-channel PWM signal output.
- Abundant timer and communication interfaces.
- Rich internal analog peripherals integrated.

3 BLDC motor control theory

The BLDC motor is a type of rotating electric machine. The stator is similar to the three-phase stator of a traditional induction motor, and the rotor has surface-mounted permanent magnets. There are no brushes on the rotor, and it is commutated electronically at certain rotor positions. Figure 2 shows a typical cross section of a BLDC motor.

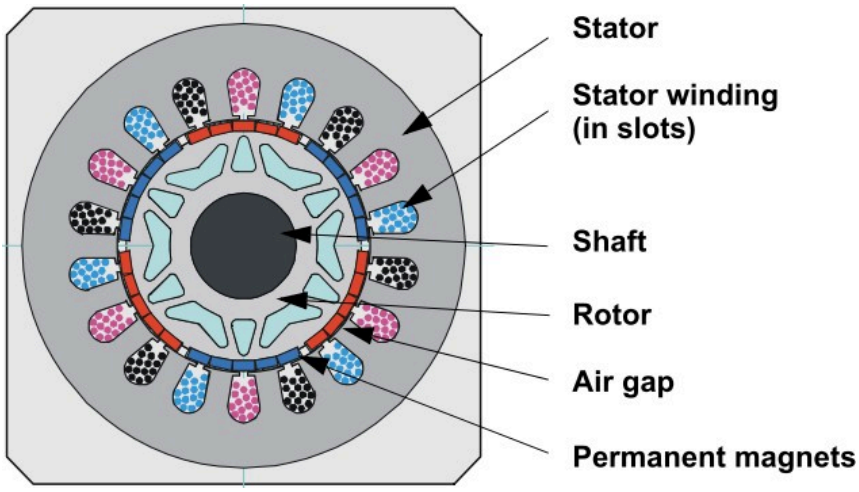

Figure 2. BLDC motor cross section

The Hall sensor is installed on the axis of the stator three-phase winding to detect the rotor position.

- When the position of the direct axis of the rotor magnet is within 180° of the positive direction of a phase axis, the Hall sensor of corresponding phase feedback gets a high level.
- When the position of the direct axis of the rotor magnet is within the reserved 180°, the Hall sensor of corresponding phase feedback gets a low level.

The midpoint of the trapezoidal back EMF is the position where the direct axis of the rotor is perpendicular to the phase axis of the stator, and the output signal of the Hall sensor jumps here, as shown in Figure 3.

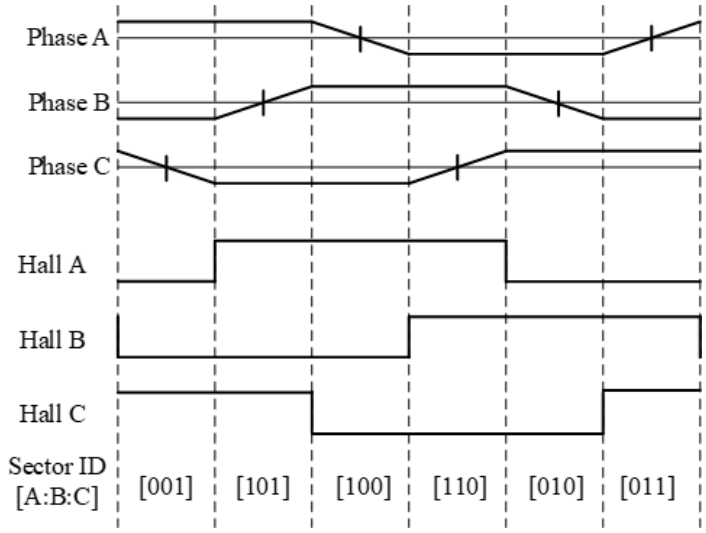

Figure 3. Phase inverter circuit

The three-phase Hall sensor is not all 0 nor all 1 at the same time, so a rotor-electrical angle can be divided into six 60° sectors. In the square wave control method, only two of the three-phase windings are selected for conduction at the same time, and the generated voltage vector coincides with the boundary of the sector divided by the Hall sensor. Position relationship between sector and voltage vector is as shown in Figure 4.

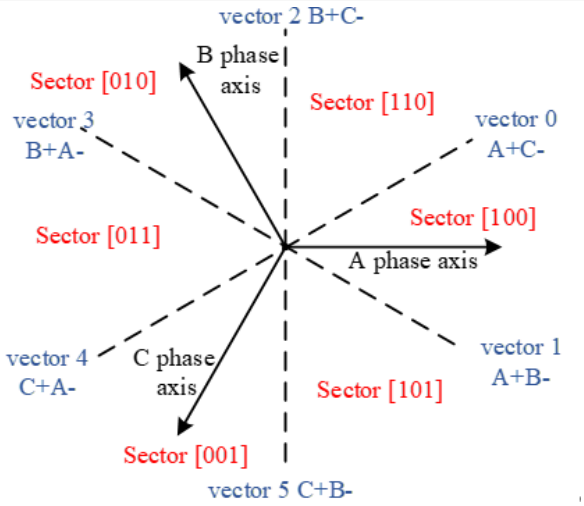

Figure 4. Phase voltage system of BLDC motor

Select the appropriate voltage vector and square wave duty cycle according to the location of the sector and the required motor rotation. For example, when the direct axis of the rotor is in sector [100], select voltage vector 2 if the motor rotates counterclockwise and select voltage vector 5 if the motor rotates clockwise.

According to different applications, double-chop PWM modulation and single-chop `H_PWM-L_ON, H_ON-L_PWM, PWM-ON, and ON-PWM` modulation can be used.

Double chop PWM modulation is used in this use case.

4 Hardware and software implementation

This chapter describes the hardware and software implementation.

4.1 System hardware design

The application hardware includes the following parts:

- LPCXpresso55S36-EVK
  The LPCXpresso55S36-EVK board is designed to work in standalone mode or as the main board of LPC553x/LPC55S3x. The onboard interfaces include RGB and other LED. Two motor control interfaces are for BLDC motor control applications. Each interface includes a three-phase PWM output and a corresponding sampling signal input interface.
- FRDM-MC-LVBLDC
  The FRDM-MC-LVBLDC low-voltage, 3-phase BLDC Freedom development board platform adds BLDC motor control capabilities, such as, rotational or linear motion, to your design applications.
  LINIX 45ZVN24-40 BLDC motor is selected. The motor control development platform block diagram and actual demo picture are as shown in Figure 5 and Figure 6.

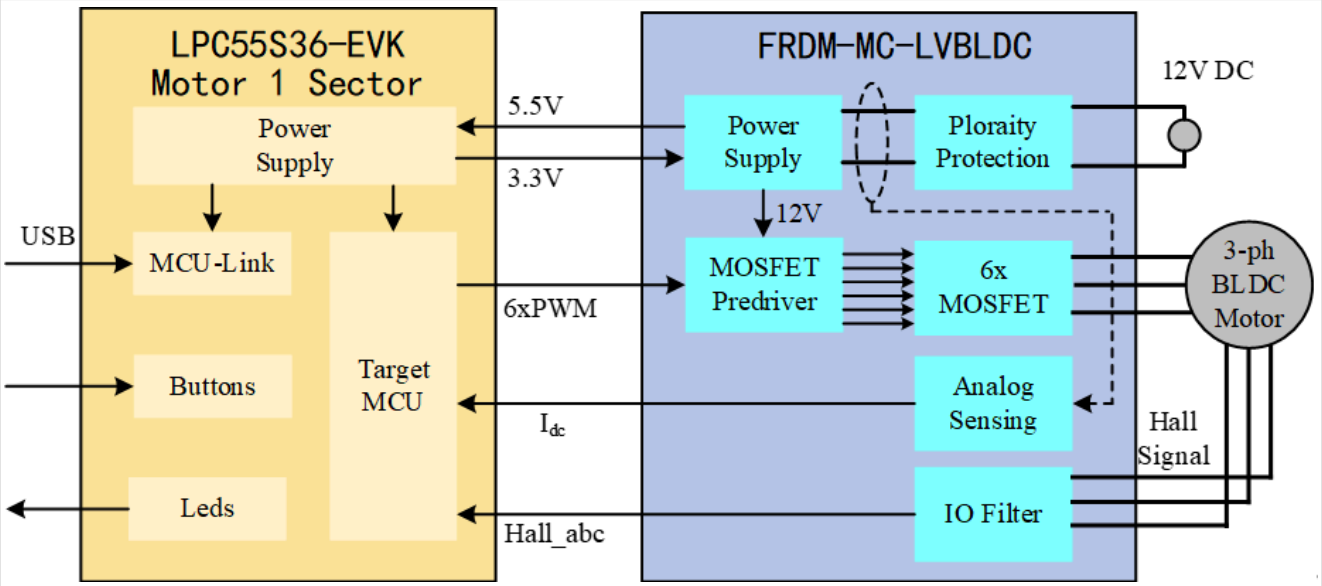

Figure 5. Motor control development platform block diagram

Figure 6. Actual demo picture

4.2 System software design

The software and hardware application can meet the below design requirements:

- Select LPC553x/LPC55S3x as controller
- Speed closed-loop control based on Hall sensor
- Overvoltage, undervoltage, and overcurrent faults protection based on hardware and software
- Minimal speed of 300 rpm, maximal speed of 2200 rpm
- Set limit current to 4 A as default
- Support two directions of rotation
- Start from any motor position without rotor alignment

Figure 7 shows the system block diagram. The overall control process contains three parts.

- Communication

Hall signal acquisition and commutation control are done in communication interrupt generated by PINT. To select the sector where the rotor located, poll the GPIO values connected to hall signals in this interrupt. At the same time, the timer stores the commutation time.

- Timed control loop
  Speed PI controller calculation, application state machine update, and software fault protection are completed in the ADC ISR (1 kHz) triggered by PWM slow loop. The output PWM duty cycle of speed PI controller is updated in timed control loop. Read cache commutation time to calculate speed.
- Software/Hardware protection
  HSCMP realizes hardware protection of bus current. It generates fault signal to eFlexPWM and DAC, which can configure current protect threshold. Software protection is executed in control loop.

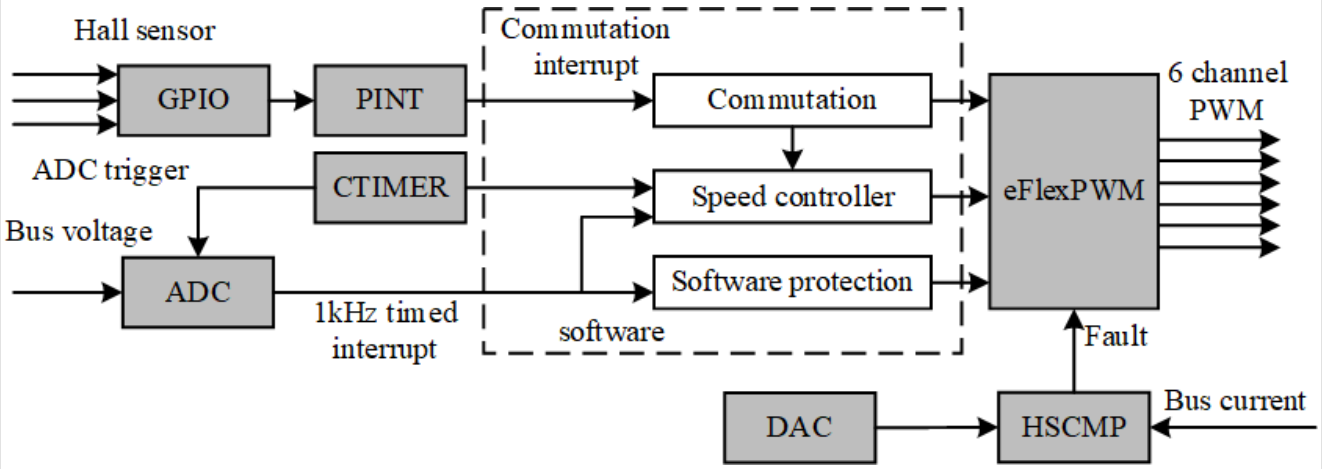

Figure 7. System block diagram

5 Peripheral configuration

This section describes the configuration of peripherals used for the motor control on LPC553x/LPC55S3x, including eFlexPWM, CTIMER, ADC, PINT, GINT, DAC, and HSCMP.

5.1 eFlexPWM

Configure eFlexPWM0 to generate 6 PWM outputs to drive the BLDC motor and enable count reset of Sub-Module 0 synchronizes Sub-Modules 1 and 2.

eFlexPWM0 configuration includes:

- Enable IPBus clock source 150 MHz.
- Full cycle reload and full cycle re-enabled

Sub-Module 0

- Running frequency of 20 kHz with 5 µs.
- Output edge-aligned and high-true complementary PWM with 1 µs dead time.
- PWM reload and initialization signals generated from this sub-module to Sub-Module 1, 2.

Sub-Module 1, 2

- Running frequency of 20 kHz with 5 µs.
- Output edge-aligned and high-true complementary PWM with 1µs dead time.
- PWM reload and initialization signals generated from Sub-Module 0.

5.2 ADC

ADC samples the DC-bus voltage. The sampled values are used to compare the overvoltage value with undervoltage value given by the user. ADC realizes the software protection of the motor control system.

ADC configuration includes：

- Bus clock source. Clock divide value is 2.
- Standard resolution. Single-ended 12-bit conversion.
- To sample DC-bus voltage, configure sampling channels, `P0_10/ADC0_1A` channel.

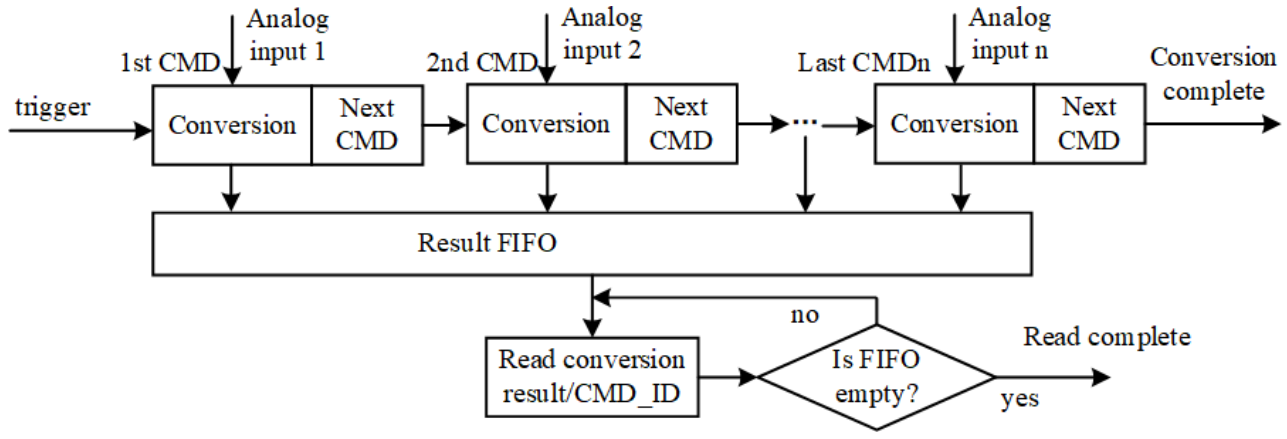

Figure 8. ADC sampling sequence and reading method

5.3 CTIMER

CTIMER0 is used to:

- Generate 1 kHz trigger to trigger ADC converting
- Enter timed control interrupt to perform speed control CTIMER0 configuration includes:
- Fixed-frequency clock source FRO 96 MHz.
- Work in Timer model and reset on match value 3.
- Connect MAT3 to ADC TRIG0 through INPUTMUX.

CTIMER1 runs freely to record and caches the commutation time point of each sector for speed calculation. CTIMER1 configuration includes:

- Fixed-frequency clock source FRO 96 MHz.

5.4 GPIO

Table 1 lists the GPIO configuration related to BLDC control on the EVK board.

Table 1. GPIO configuration

Pin_num	Pin_name	Pin_function	Pin_num	Pin_name	Pin_function
11	PIO1_20	PWM0_A0	70	PIO0_13	GPIO_input
91	PIO1_17	PWM0_B0	71	PIO0_14	GPIO_input
50	PIO1_6	PWM0_A1	78	PIO1_11	GPIO_input
40	PIO1_22	PWM0_B1	30	PIO1_19	ADC0_1A
36	PIO1_8	PWM0_A2	35	PIO1_5	HSCMP0_IN3

Table 1. GPIO configuration...*continued*

Pin_num	Pin_name	Pin_function	Pin_num	Pin_name	Pin_function
75	PIO1_4	PWM0_B2			

The GPIO configuration can be realized through Configure Tools of MCUXpresso IDE as shown in Figure 9.

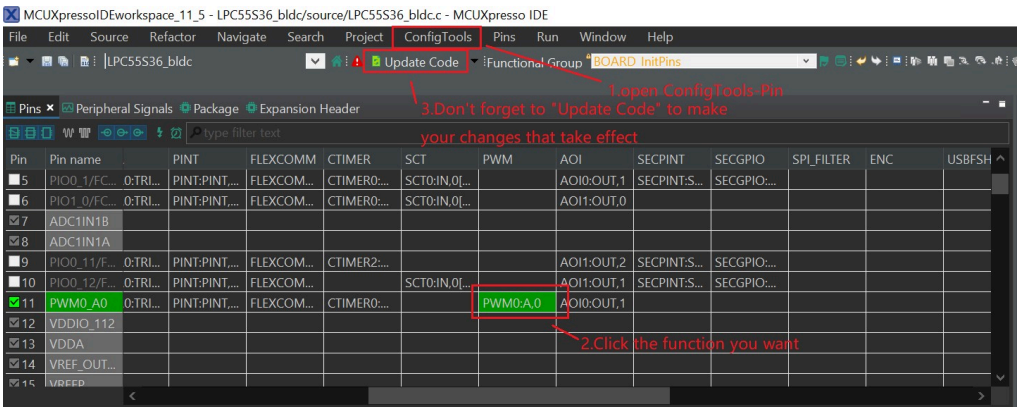

Figure 9. ADC sampling sequence and reading method

5.5 GINT

GINT0 is used to generate general-purpose interrupt to detect SW3 switch condition to realized control function by users. GINT0 configuration includes:

- Enable AHB clock.
- Level-triggered and low-level active.
- Enable `PIO1_17` to contribute to grouped interrupt.

5.6 PINT

`PIN_INT_IRQ 0-2` is used to detect edge of hall signal A, B, and C respectively to generate interrupt and complete communication. `PINT0` configuration includes:

- Select `PIO0_13`, `PIO0_14`, and `PIO1_11` as interrupt source of `PIN_INT_IRQ` 0-2 respectively.
- Level-triggered and both rise and fall edge active.

5.7 DAC

DAC is used to configure bus current threshold and the negative input of the HSCMP. DAC0 configuration includes:

- Enable clock source main clock 150 MHz and 6 divided get a 25 MHz clock.
- Select VREFH1 as the reference voltage.
- Use OPAMP as the DAC analog buffer.
- DAC convert value is DATA × 3.3 V/4096.

5.8 HSCMP

HSCMP is used to compare bus current sampling signal and user configured DAC threshold value to perform hardware protection. HSCMP0 configuration includes:

- Input minus = External DAC, input plus = analog mux in3, high power/high speed mode.

- Connect compare output to fault of eFlexPWM.

6 Software implementation

This section describes the software design of the BLDC motor application.

6.1 State machine

State machine control in ADC interrupt controls motor running state, as shown in Figure 10.

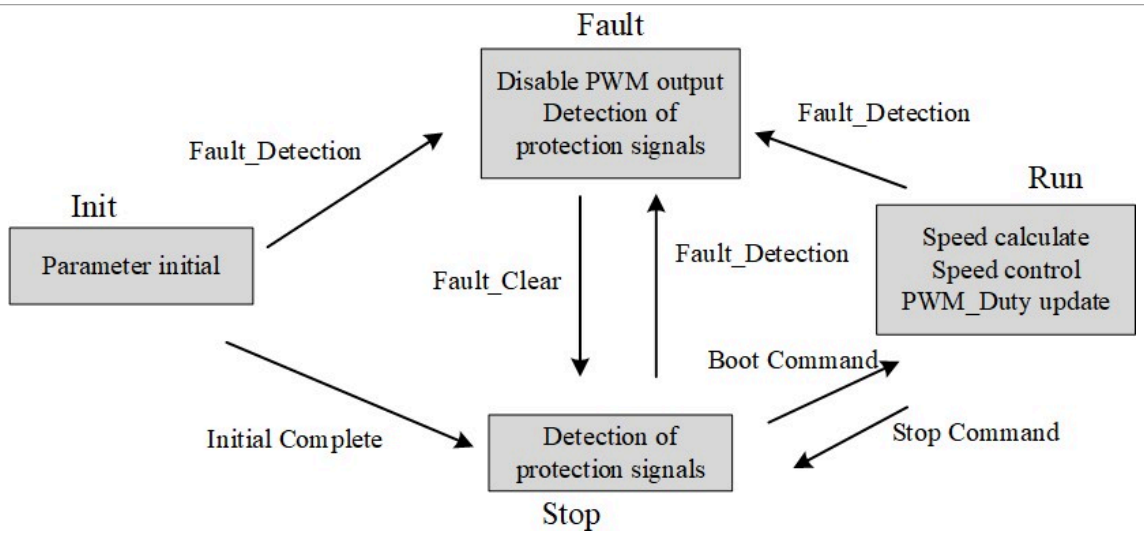

Figure 10. State machine flowchart

6.2 Speed calculation

CTIMER1 records the duration of each sector. The motor speed (RPM) can be calculated according to the time of the first six sectors.

$$Speed\_Fed = \frac{60}{Cnt_{SixSector} * Period * Polepair} \quad (1)$$

7 Demo operation

This chapter describes the demo operation.

7.1 Motor parameters

Table 2 provides motor specifications.

Table 2. GPIO motor specifications

Manufacturer name	Linux	Stator resistor /Ohm	1
Model	45ZWN24-40	Stator winding inductance d-axis/μH	426
Rated speed/rpm	4000	Stator winding inductance q-axis/μH	460
Rated line voltage/V	24	Pole pairs	2
Rated power/W	40	Back EMF Constant/V.s.rad-1	0.01456

The application parameters (speed PI controller and starting current value) are set for a motor with a plastic ring (part of the kit) mounted on the shaft. Otherwise, speed oscillations may occur.

7.2 Demo experiment performance

As shown in Figure 11, when the motor runs at a speed of 1000 rpm,

- The signal of the Hall sensor changes alternately.
- The voltage of the motor-winding terminal is chopped according to the output of the Hall signal.
- The opposite potential is a zero-crossing waveform without conduction.

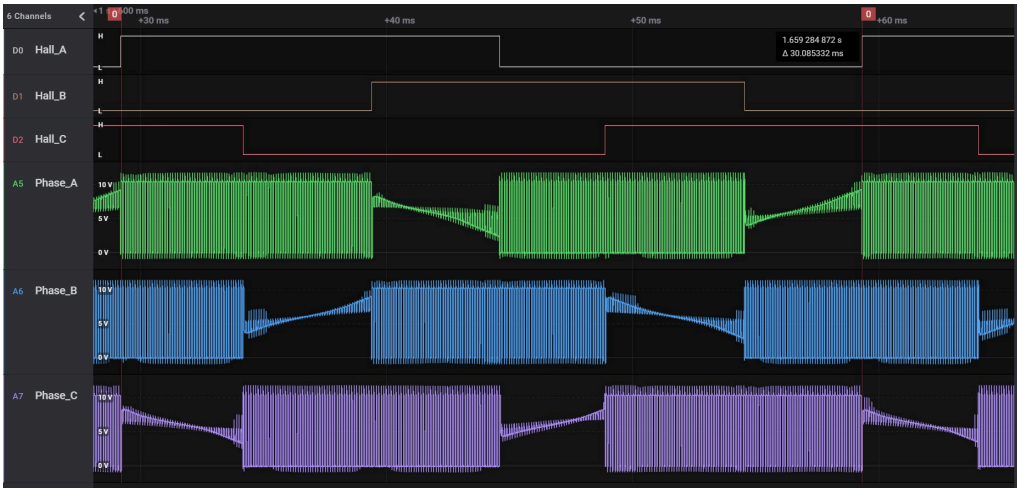

Figure 11. Hall signal and motor-winding terminal at 1000 rpm

7.3 CPU load and memory usage

Table 3 shows the space usage and core load of the demo program. The CPU load is measured using the SYSTick timer.

Table 3. LPC553x/LPC55S3x BLDC motor control demo CPU load and memory usage

Code memory [bytes]	20132
Data memory [bytes]	8720
CPU cycles	257
CPU load	1.71 %

8 References

These references are available on www.nxp.com:

- *LPC553x Reference Manual* (document LPC553xRM)
- *MCUXpresso SDK 3-Phase PMSM Control(LPC)* (document 3PPMSMCLPCUG)

9 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Revision number	Release date	Description
4	30 January 2024	Corrected a typo in Section 6.
3	7 December 2023	Updated according to the SDK, IDE, and EVK board update
2	17 July 2023	• Updated Section 4.1 • Updated Section 5.1 • Updated Section 5.3 • Updated Section 7.3
1	25 May 2022	Replaced LPC55S3x with LPC553x/LPC55S3x
0	25 March 2022	Initial release

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