AN13125

IW416 Design Guide

Rev. 1 — 26 May 2021 Application note

Document information

Information	Content
Keywords	Power supply, clock source, reset, host interface, RF interface, PCB layout, PCB stackup
Abstract	Provides design guidelines for IW416 device.

Revision history

Rev	Date	Description
v.1	20210526	Initial version

1 Overview

This document provides design guidelines for NXP IW416 device. The IW416 is a highly integrated Wi-Fi® 4 (2.4 GHz/5 GHz) and Bluetooth® 5.1 single-chip solution.

The IW416 is available in two package options – QFN and WLCSP.

NXP releases reference designs to provide examples on how to design a PCB using the device. We strongly recommend follow these design guidelines closely. Please contact your NXP representative to schedule a design review and discuss design options.

Note: *In the following sections, the IW416 may be referred to as "Wireless SoC"*

2 Power supply

2.1 Power supply overview

Table 1 lists the power supplies.

Table 1. Power supplies

Supply	Description	Typical value
VCORE	Core power supply	1.05 V
AVDD18	Analog power supply	1.8 V
VPA	Wi-Fi PA power supply	2.2 V
VIO	Digital I/O power supply	1.8 V or 3.3 V
VIO_SD	SDIO power supply	1.8 V or 3.3 V
VIO_RF	RF power supply	1.8 V or 3.3 V

A “2-wire” power management interface is used to lower the core voltage to reduce power consumption in sleep mode. The power management interface uses two control signals, DVSC1 and DVSC0, to dynamically adjust the voltage level from the power management IC (PMIC). Under normal operation, the core voltage level is 1.05 V. In sleep mode, the core voltage is dropped to 0.8 V.

The following sections describe PMIC solutions from MPS, NXP, and Marvell manufacturers:

- MPS: MP2182, MP2162A, MP8904
- Marvell 88PG823
- NXP PM823

2.2 Power supply using MPS PMICs

Figure 1 shows a simplified block diagram using the MPS MP2182, MP2162A and MP8904. Two control signals, DVSC1 and DVSC0, are used to control the core voltage level. Table 2 shows the part numbers.

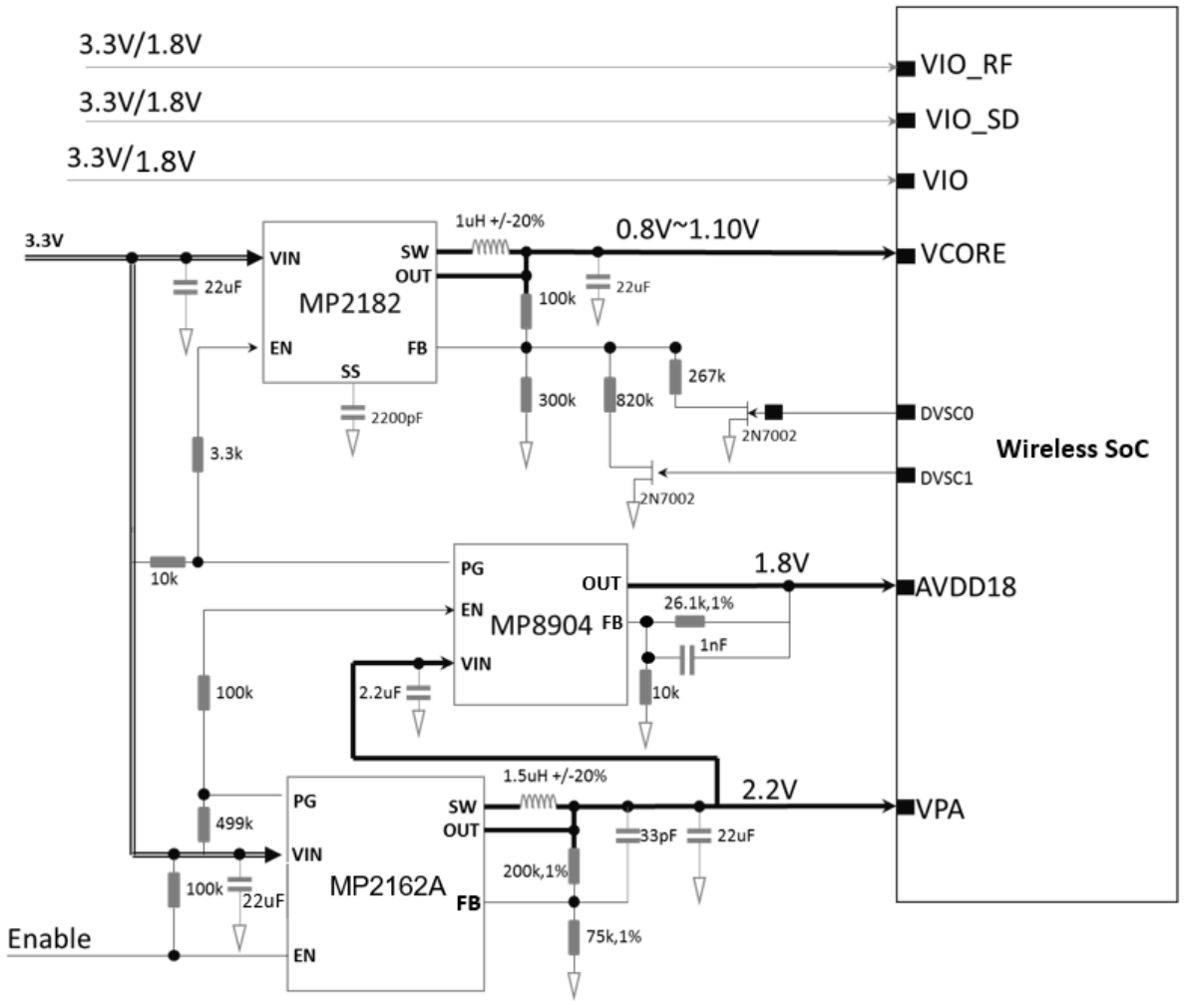

Figure 1. Power supply by MPS PMICs

Table 2. MPS PMICs part numbers

Manufacturer	Part number
MPS	BUCK: MP2162AGQH-C867-Z
MPS	BUCK: MP2182GTL-C867-Z
MPS	BUCK: MP8904DD-C867-LF-Z

2.3 Power supply using NXP PM823 or Marvell 88PG823

Figure 2 shows a simplified block diagram using the NXP PM823 or Marvell 88PG823 (QFN). Two control signals, DVSC1 and DVSC0, are used to control the core voltage level. Table 3 shows the part numbers.

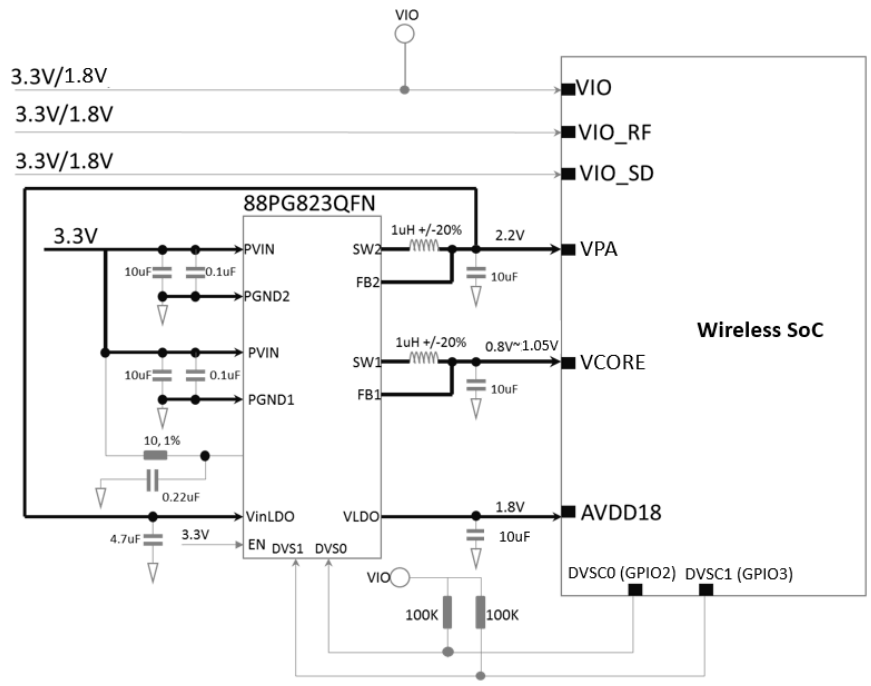

Figure 2. Power supply by 88PG823 (QFN)

Table 3. Marvell and NXP PMICs part numbers

Manufacturer	Part number
Marvell	QFN package option: 88PG823-xx-NPD2C000
Marvell	WLCSP package option: 88PG823-xx-CBK2-T
NXP	QFN package option: PM823HN/A0CHP
NXP	WLCSP package option: PM823UK/A0CZ

2.4 Power-up sequence requirements

All the power rails must meet correct power-up sequence. Refer to IW416 data sheet.

2.5 PCB layout guidelines

Refer to the following PCB layout guidelines for power supply.

- Follow the PMIC schematic/layout exactly. Any deviation must be reviewed with PMIC vendor Applications Engineer.
- Use power planes (layer) and polygons to lower the power impedance.
- Use decoupling capacitors with low ESR
- Place the power vias and ground vias as close as possible to the decoupling capacitors, as shown in Figure 3.

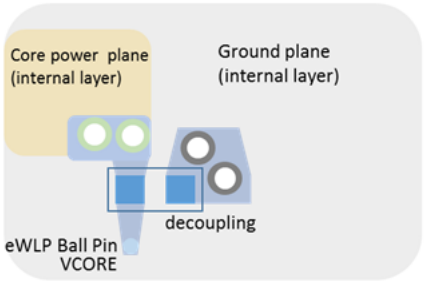

Figure 3. Power vias and ground vias

- Ensure each power pin has its own decoupling capacitor. Place the decoupling capacitors as close as possible to the power pin.
- The power from source to the power pin should go through the decoupling network before connecting to the power pin. As shown in Figure 4

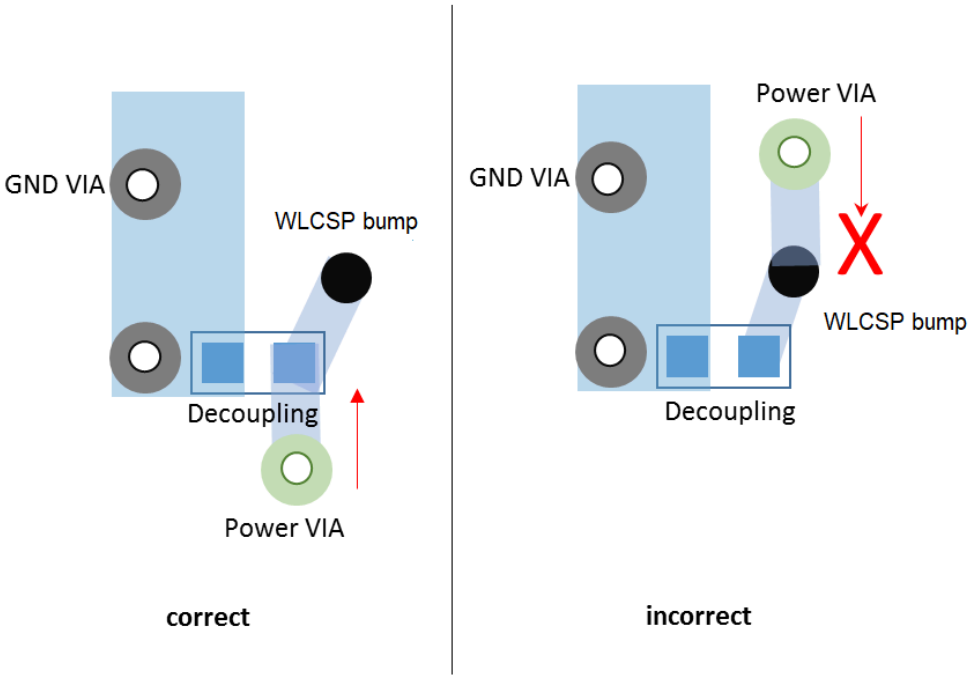

Figure 4. Example of power trace outing to power pin

- There is a decoupling capacitor for each power pin and a bulk capacitor for each rail. Place the decoupling capacitor as close as possible to the power pin, then place the bulk capacitor. Figure 5 shows an example where C9 is the decoupling capacitor for K5 pin. In this example, place C9 as close as possible to K5 pin, and place C58 close to C9.

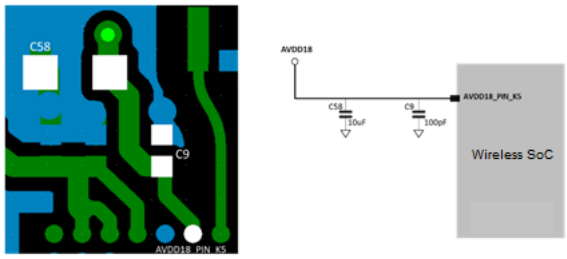

Figure 5. Decoupling capacitor and bulk capacitor placements

- Do not place any analog power plane (trace) as ring and loop in the layout. Figure 6 shows the correct top layer (left hand side of the figure) and the incorrect top layer (right hand side). In the correct top layer, there is no loop on the AVDD18 net.

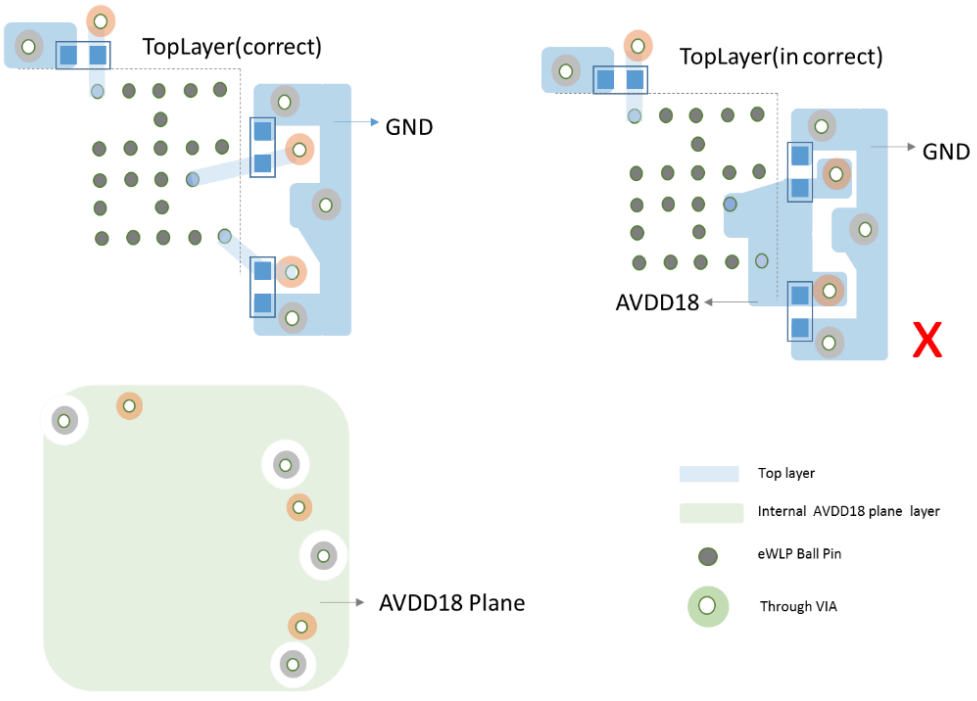

Figure 6. Power plane without loop

3 Clock source

Two main clock sources are available: a crystal, and an external oscillator. An optional sleep clock is also available for low power mode.

3.1 Crystal

In a typical application, a 26 MHz or 40 MHz crystal is used as a reference clock source. We recommend to select a crystal with ±10 ppm at 25°C and ±10 ppm over the operating temperature range. For detailed crystal specifications, refer to IW416 data sheet.

Figure 7 shows the crystal connections. The internal capacitor in the Wireless SoC is used to tune the crystal frequency. External loading capacitors are typically not needed.

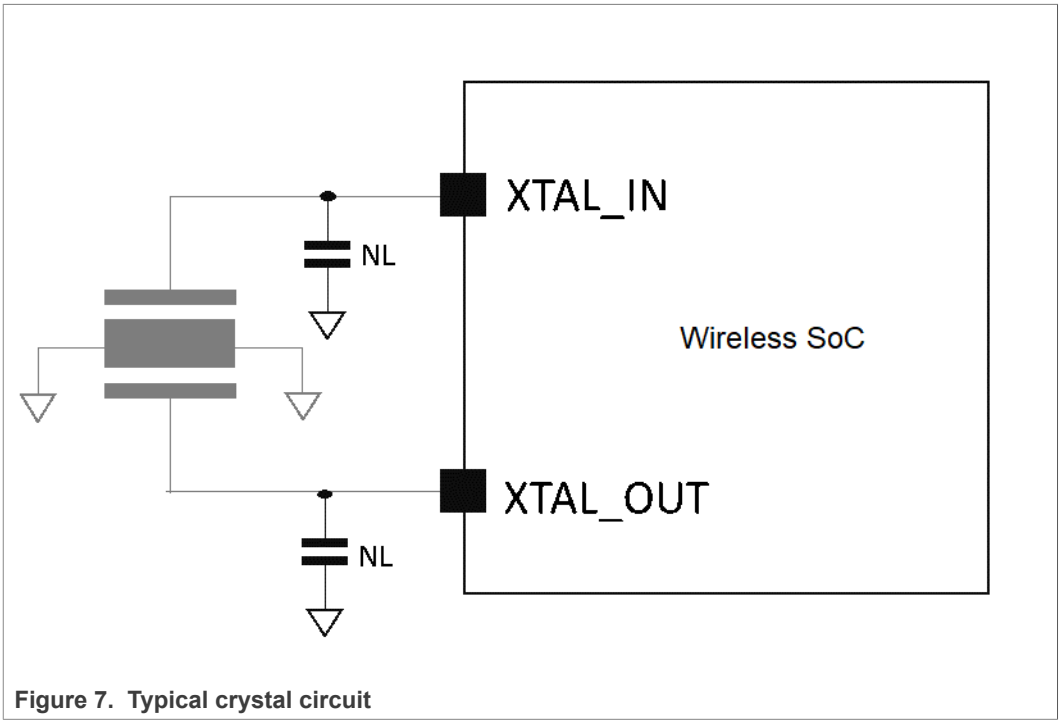

Figure 7. Typical crystal circuit

PCB layout guidelines for the crystal

Refer to the following guidelines for the crystal:

- Place the crystal close to the device and keep it as far away as possible from the RF side of the device and high frequency signal traces such as SDIO, PCIe, or USB.
- Keep XTAL_IN and XTAL_OUT traces far from any noisy or switching signal, at a distance of at least ten times the substrate height.

- Keep XTAL_IN and XTAL_OUT traces as short as possible, as shown in Figure 8.

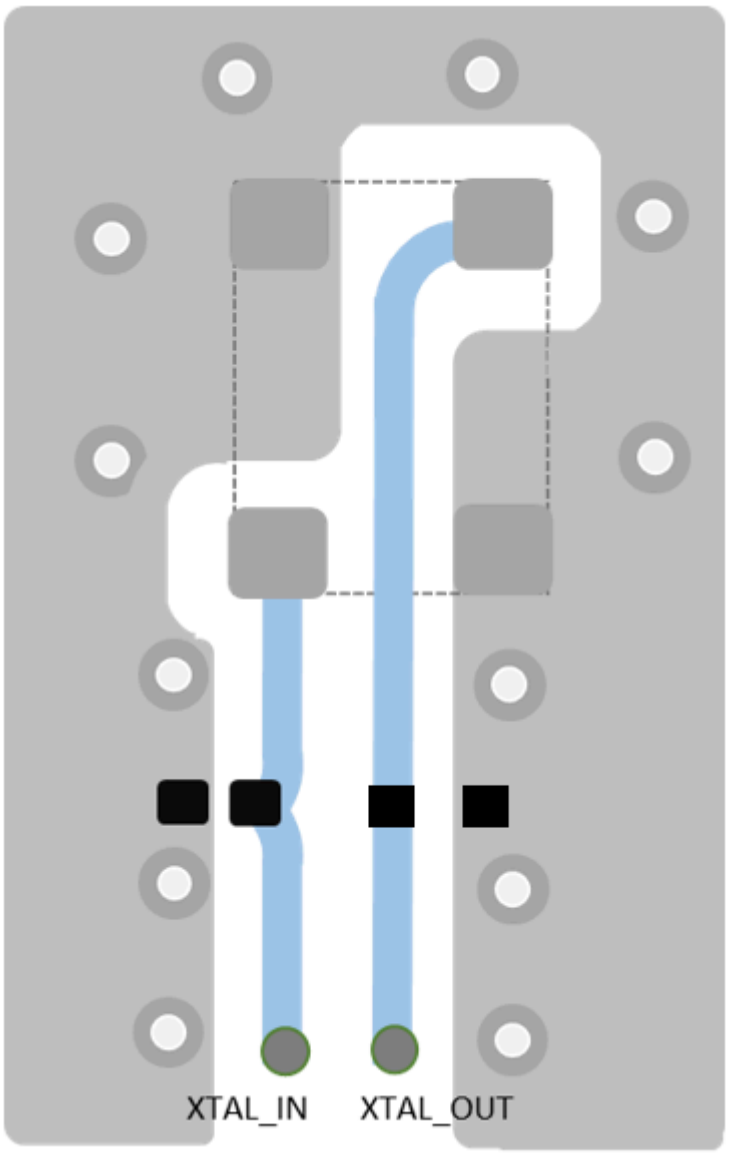

Figure 8. Crystal PCB layout

- Make sure XTAL_IN and XTAL_OUT traces are referenced to the solid ground plane in the second layer.
- Place the ground guard with ground stitching vias around the XTAL_IN and XTAL_OUT traces, as shown in Figure 8.
- To minimize the reference clock signals, cut out all internal metal planes under the crystal and keep the last ground plane as the reference plane.

3.2 External oscillator

Figure 9 shows the typical application circuit for an external oscillator.

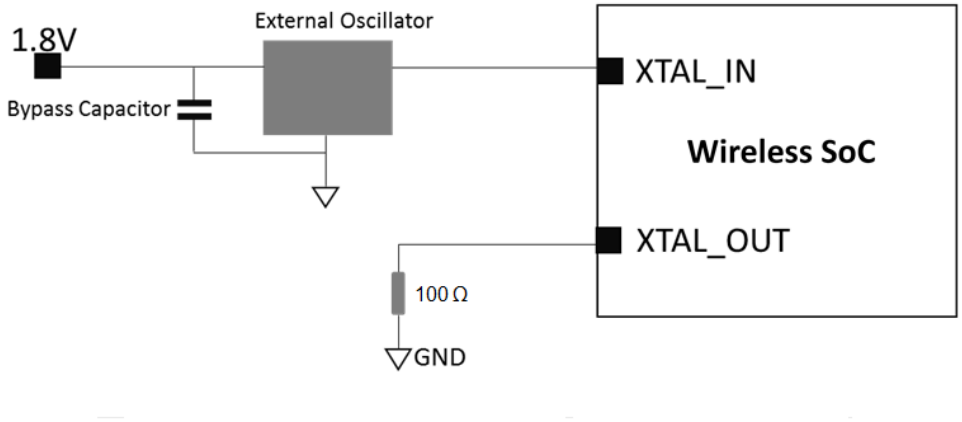

Figure 9. External oscillator circuit

An external 26 MHz external oscillator may be used as reference clock source. If using an external oscillator, make sure its frequency accuracy meets the ±20 ppm IEEE specification over the operating temperature range of the product. Refer to IW416 data sheet for the oscillator requirement specification.

PCB layout guidelines for the external oscillator

- Follow the external oscillator vendor's recommendations for the layout.
- Place the oscillator as far as possible from the Wireless SoC RF side.
- Keep the clock trace as short as possible.
- Ground the guard trace with the ground via around the clock trace.

3.3 Sleep clock

An optional external sleep clock may be used to further reduce the power consumption in sleep mode.

Note the following:

- The external sleep clock frequency is 32.768 kHz.
- The external sleep clock usage is optional
- If an external sleep clock is not used, it is recommended to leave the SLP_CLK_IN pin floating.

4 Reset

4.1 Reset overview

Power on reset (POR) is triggered when the correct power up sequence is followed. Refer to IW416 data sheet for details on power up sequence requirements.

The PDn signal is used to reset the Wireless SoC. On the NXP reference design, the PDn signal is pulled up to VIO to meet the power-up sequence requirements. The PDn pin may be connected to a reset signal from the host CPU. Refer to IW416 data sheet for further details on PDn usage.

4.2 Reset strap configuration

It is critical to set the reset configuration pins correctly at reset to ensure the proper configuration for the Wireless SoC. Refer to IW416 data sheet for details on the configuration pins and host configuration options.

4.3 PCB layout guidelines

- Do not route PDn signal next to a large switching signal or on the edge of the PCB to avoid EMI affecting the reset signal, as shown in Figure 10.
- The pull-up resistor on the external reset signal is placed close to PDn pin.

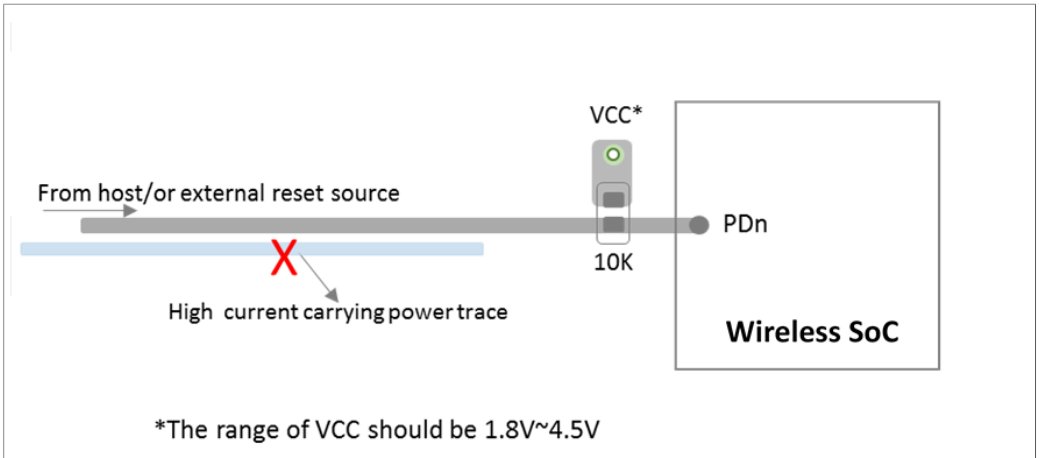

Figure 10. PDn signal trace routing

5 Host interface

Table 4 lists the supported host interfaces.

Table 4. Wi-Fi and Bluetooth host interfaces

Wi-Fi	Bluetooth
SDIO 3.0	UART

5.1 SDIO interface

The SDIO interface has the following characteristics:

- SDIO v3.0 is backward compatible with SDIO v2.0 HOST. SDIO 3.0 is recommended for maximum throughput.
- For SDIO clock running at 25 MHz (SDR12) and 50 MHz (SDR25), VIO_SD must be 3.3V.
  For SDIO clock running at > 50 MHz (SDR50 and DDR50), VIO_SD must be 1.8V.
- SDIO clock (SD_CLK) supports up to 208 MHz clock speed
- The required pull up for SDIO interface on SD_CMD, and SD_D[3:0] signals should be provided by the host. The pull up value is between 10 kΩ to 100 kΩ according to SDIO v3.0 specifications.
- Series damping resistors may be needed to help with signal integrity issues. When extending the SDIO signals through ribbon cable, series resistors of 75 Ω are recommended to reduce the undershoot/overshoot due to long trace run and cable impedance mismatch.

Figure 11 shows the SDIO interface connection to the host processor.

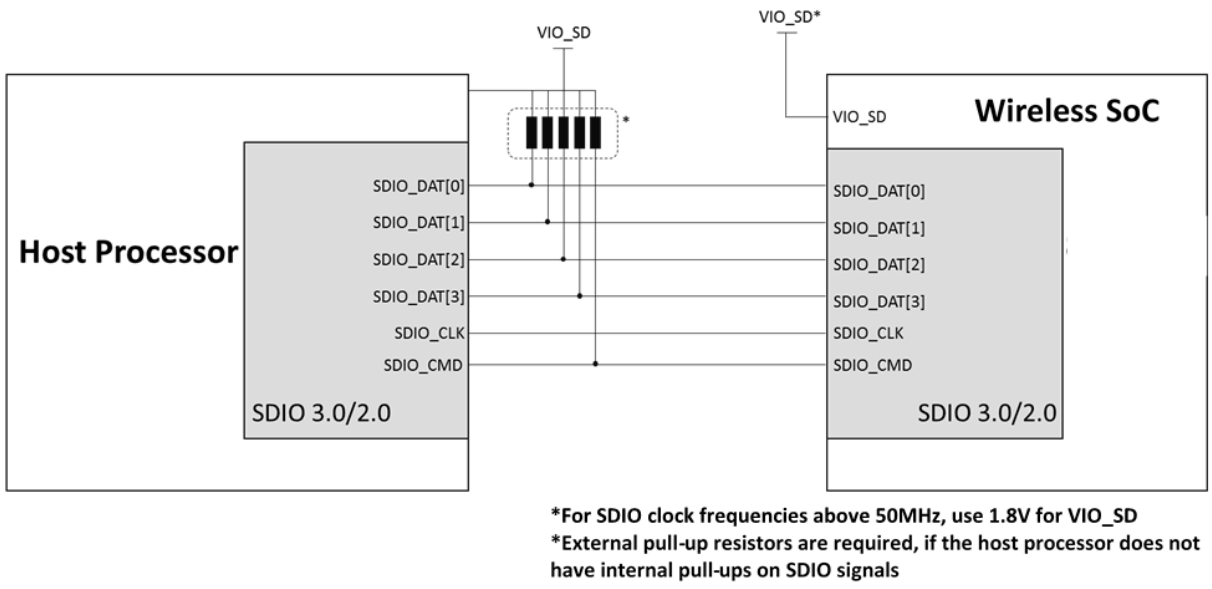

Figure 11. SDIO interface connection to host processor

PCB layout guidelines for SDIO interface

Refer to the following PCB layout guidelines for SDIO interface:

- SDIO signals are routed with 50(±10%) ohm impedance
- Route the SDIO signals as far away as possible from the RF trace
- Route all SDIO signal lines entirely over a solid ground plane. Avoid splits and voids on an adjacent layer.
- Keep the same length for all SDIO signal traces and as short as possible.
- Place the ground plane along with SDIO signals with stitch vias as shown in Figure 12.

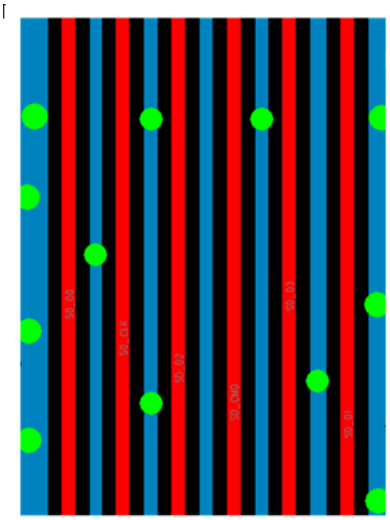

Figure 12. Place ground between SDIO signals with ground stitch vias

- Avoid routing power supply traces under or above SDIO signal traces. If SDIO signal traces are routed on one of the inner layers, then make sure to shield them by having solid ground above and below SDIO traces.
- The bend trace routing should be smooth with a large radius rather than of 90 degree with a sharp edge, as shown in Figure 13.

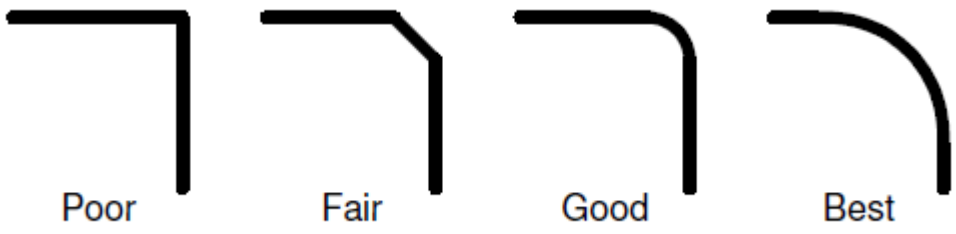

Figure 13. Bend trace routing

5.2 UART interface

Figure 14 shows a typical application circuit for the UART interface.

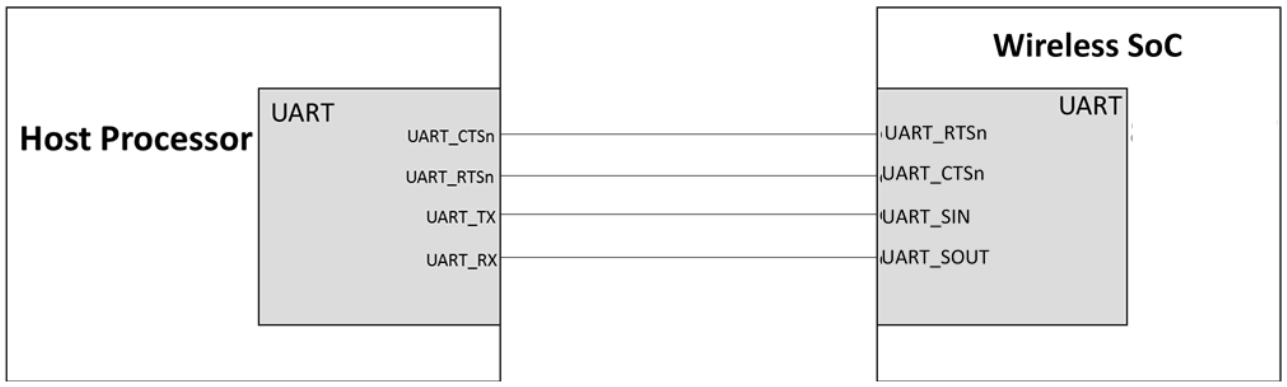

Figure 14. UART host interface connections

6 RF interface

The NXP reference designs for the Wireless SoC show the front-end configurations currently supported by NXP. It is recommended to discuss your desired front-end configuration with your NXP representative and have your design reviewed by NXP.

6.1 RF front-end for QFN package

The QFN package can be used in single and dual antenna applications. In a dual antenna application, one antenna is for Wi-Fi and the other antenna is for Bluetooth. In a single antenna application, the antenna is shared between Wi-Fi and Bluetooth.

Figure 15 shows the typical front-end topology for a two-antenna application. Use discrete low pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance needs to match 50 Ω.

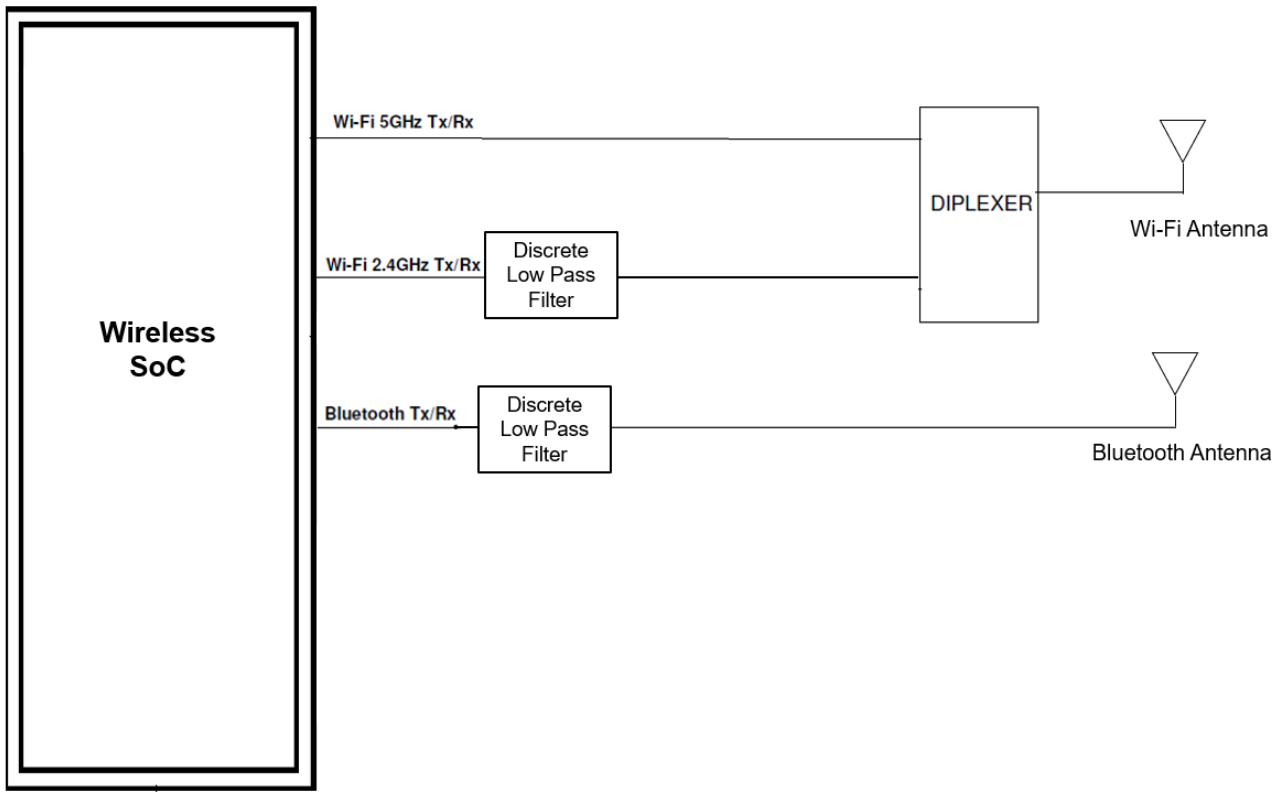

Figure 15. RF front-end for two antenna application

Figure 16 shows the filter circuit for Wi-Fi 2.4 GHz path.

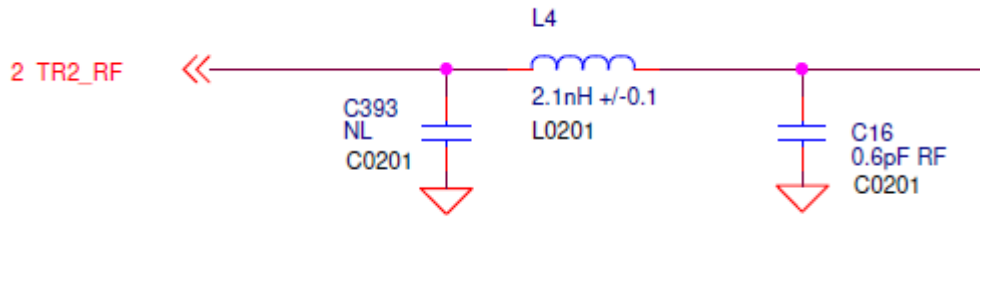

Figure 16. Discrete LPF on Wi-Fi 2.4GHz RF path

Figure 17 shows the filter circuit for Bluetooth path.

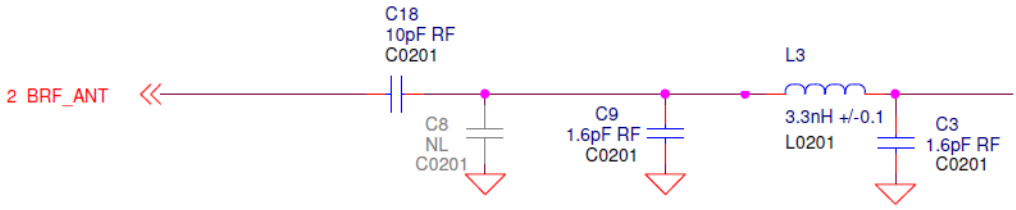

Figure 17. Discrete LPF on Bluetooth RF path

For two antenna applications and where simultaneous 2.4 GHz Wi-Fi and Bluetooth transmission is possible, note the following recommendations:

- To reduce the impact of mutual interference, provide at least 30 dB isolation between the two antennas
- Keep the antenna gain to a minimum, outside the 2.4 and 5 GHz bands
- In applications where the antenna isolation is limited, the transmit power level for the Bluetooth radio may need to be reduced. The transmit power level depends on various system design factors such as antenna gain and isolation.

Figure 18 shows the typical front-end topology for a single-antenna application. An external SPDT switch is required to combine the 2.4 GHz Wi-Fi and Bluetooth transmit/receive paths. Use discrete low pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance needs to match 50 Ω. Refer to Figure 16 for the filter circuit on Wi-Fi 2.4 GHz path.

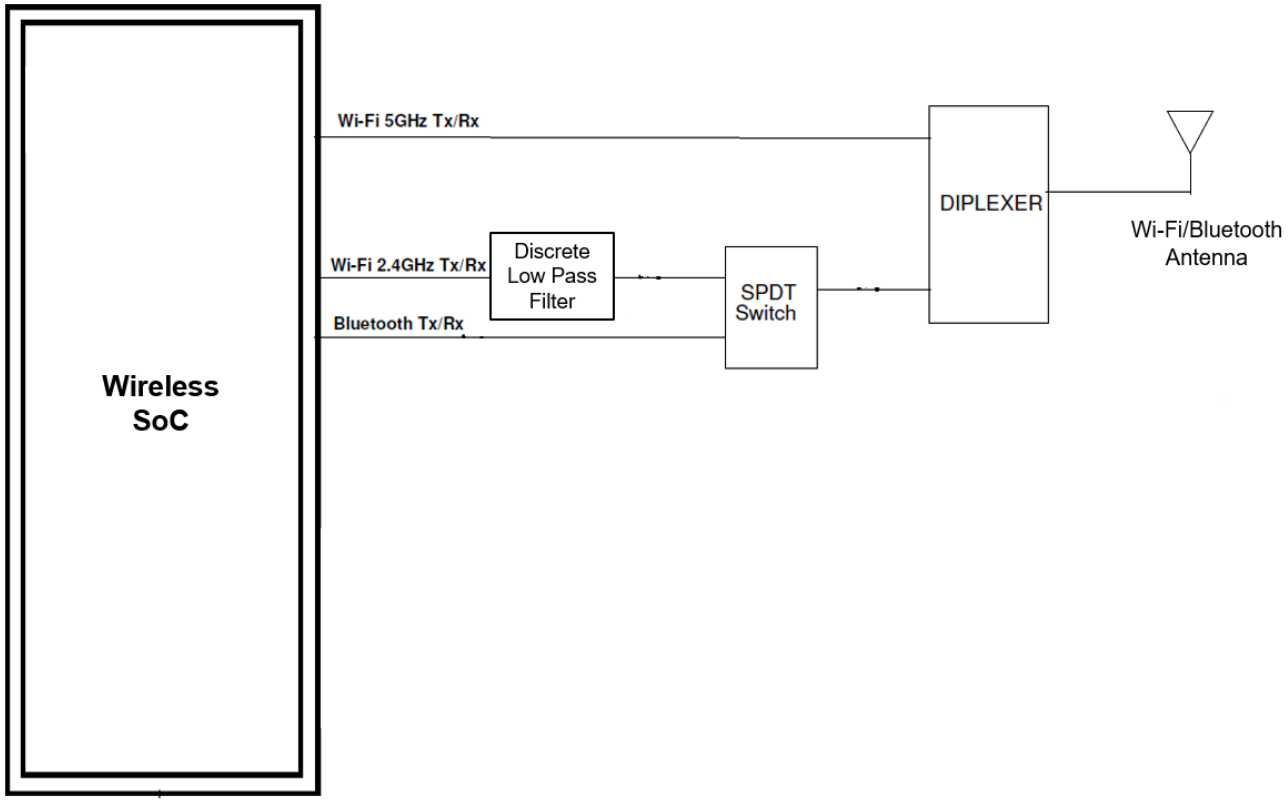

Figure 18. RF Front-end for single antenna application

Table 5 lists the recommended RF front-end components.

Table 5. Recommended RF front-end components

RF component	Manufacturer	Part number
Diplexer	TDK	DPX166000DT-8093A1
SPDT switch	SKYWORKS	SKY13323-378LF
Discrete LPF on Wi-Fi 2.4 GHz path	—	L = 2.1 nH ± 0.1 nH (0201), C = 0.6 pF (0201)
Discrete LPF on Bluetooth path	—	C= 1.6 pF (0201), L = 3.3 nH ± 0.1 nH (0201), C = 1.6 pF (0201)

6.2 RF front-end for WLCSP package

Similar to QFN package, WLCSP package can also be configured as single or dual antenna front-end application. WLCSP package requires an external RF SPDT switch on 5 GHz Wi-Fi path to provide additional rejection to out-of-band emissions. The following RF front-end components must be used to reduce out-of-band emissions.

- RF SPDT switch on Wi-Fi 5 GHz path
- Bandpass-bandpass structure diplexer

Figure 19 shows a typical front-end topology for dual antenna applications.

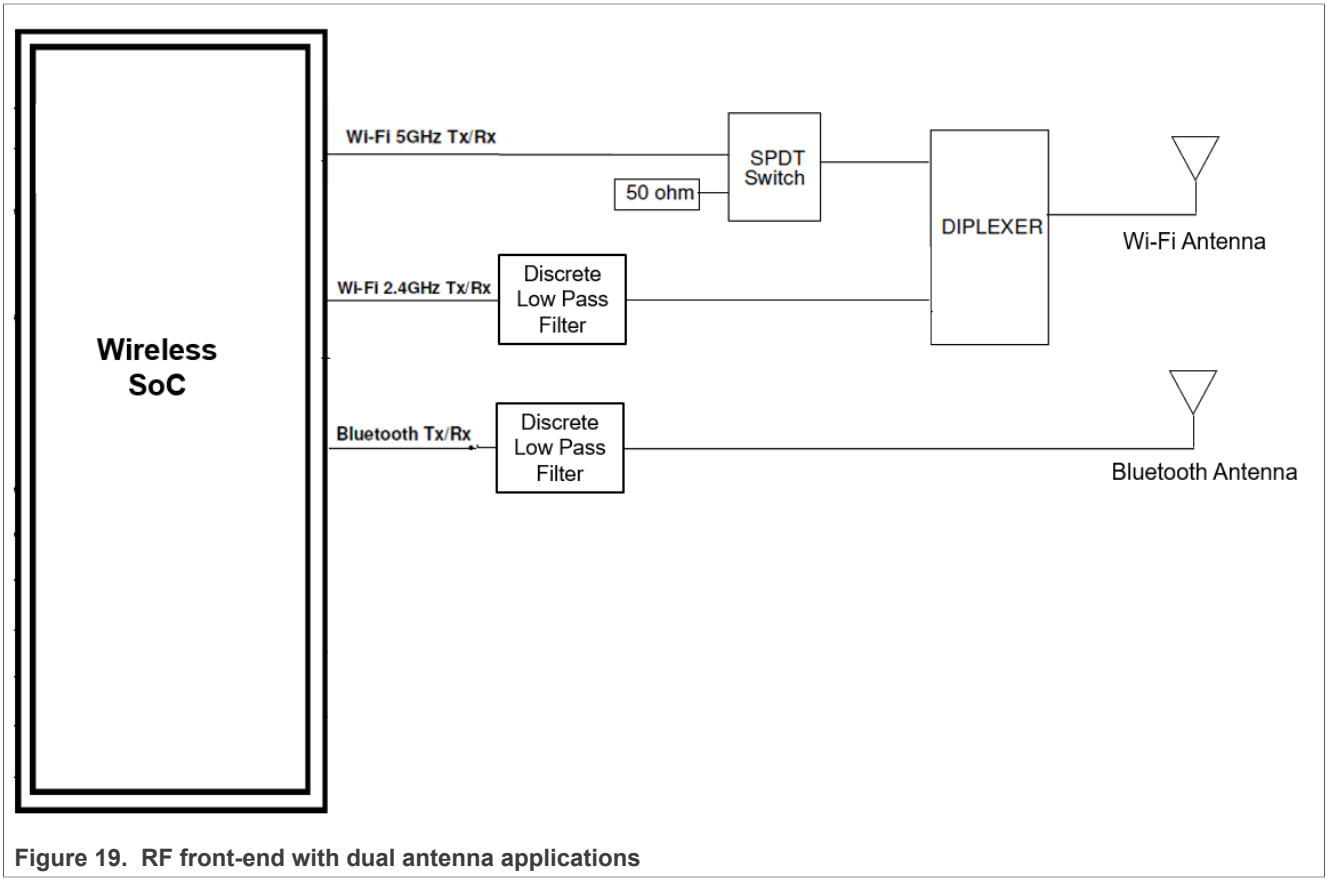

Figure 19. RF front-end with dual antenna applications

Use discrete low pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance needs to match 50 Ω. Refer to Figure 16 for filter circuit on Wi-Fi 2.4 GHz path and Figure 17 for the filter circuit on Bluetooth path.

Figure 20 shows the circuit diagram for SPDT switch on Wi-Fi 5 GHz path.

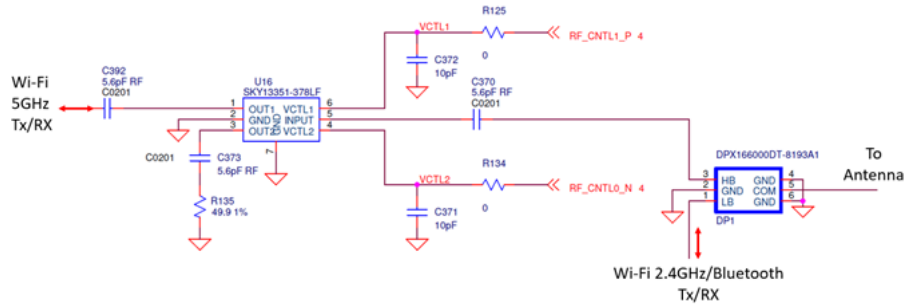

Figure 20. Circuit diagram for SPDT switch on Wi-Fi 5 GHz path

Table 6 shows the list of recommended RF front-end components.

Table 6. Recommended RF front-end components

RF component	Manufacturer	Part number
Diplexer	TDK	DPX166000DT-8193A1
SPDT switch	SKYWORKS	SKY13323-378LF
Discrete LPF on Wi-Fi 2.4 GHz path	—	L = 2.1 nH ± 0.1 nH (0201), C = 0.6 pF (0201)
Discrete LPF on Bluetooth path	—	C= 1.6 pF (0201), L = 3.3 nH ± 0.1 nH (0201), C = 1.6 pF (0201)

For single antenna designs, use the second SPDT switch to combine Wi-Fi 2.4 GHz and Bluetooth transmit/receive paths.

Figure 21 shows a typical front-end topology for single antenna applications.

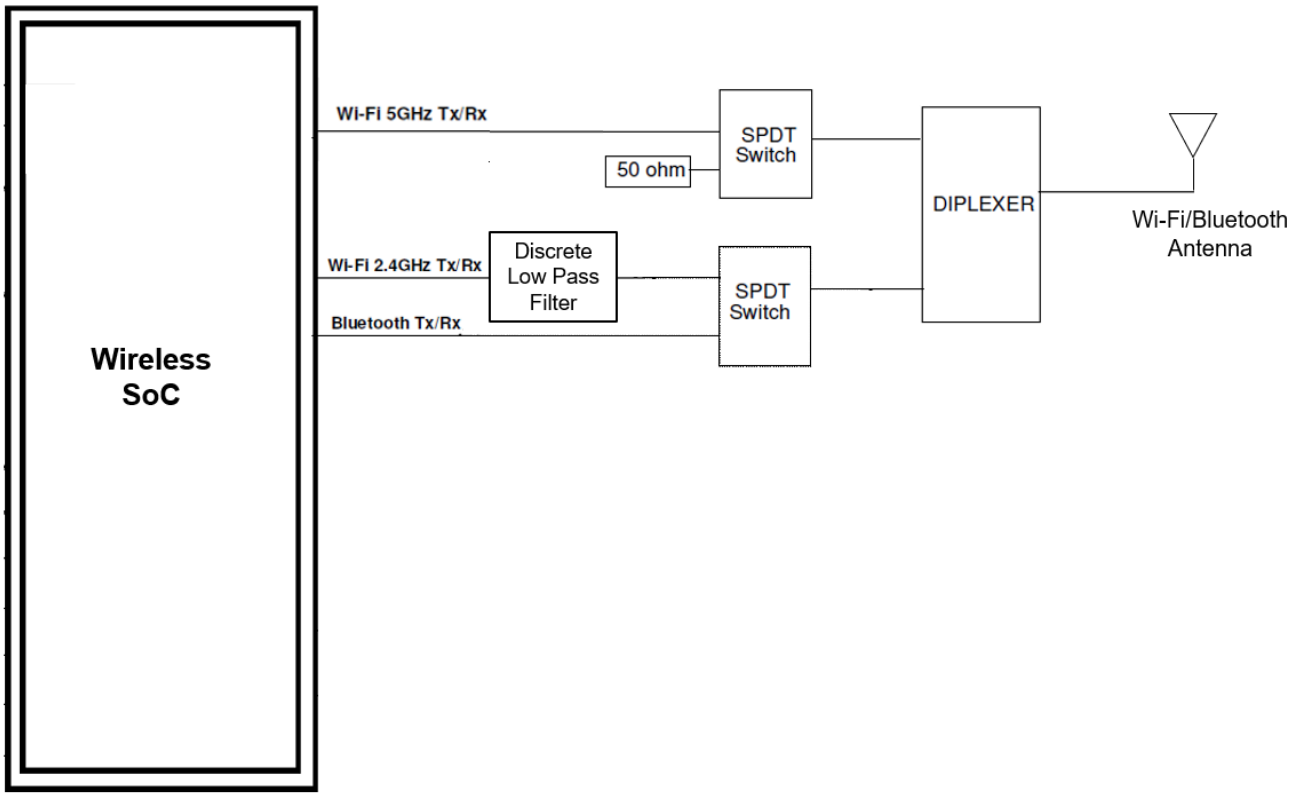

Figure 21. RF front-end for single antenna application

Use discrete low pass filters (LPF) to ensure the rejection of out-of-band emissions. LPF components also act as impedance matching circuits between the wireless SoC pin and the diplexer part on the PCB. For maximum power transfer in RF, the input/output impedance needs to match 50 Ω. Refer to Figure 16 for the filter circuit on Wi-Fi 2.4 GHz path.

Keep the antenna gain to a minimum, outside the 2.4 GHz and 5 GHz bands. An RF shield is recommended to minimize radiated emissions and any RF interference.

6.3 PCB layout guidelines

Refer to the following PCB layout guidelines for RF interface:

- Route the RF signals on the top layer (micro strip) with 50 ohm impedance.
- Reference the RF signals to a solid ground plane.
- Use at least a 3X H clearance between the ground pour and RF micro strip to minimize the impact on the micro strip impedance. Maintain this gap around any RF signal via, as shown in Figure 22.

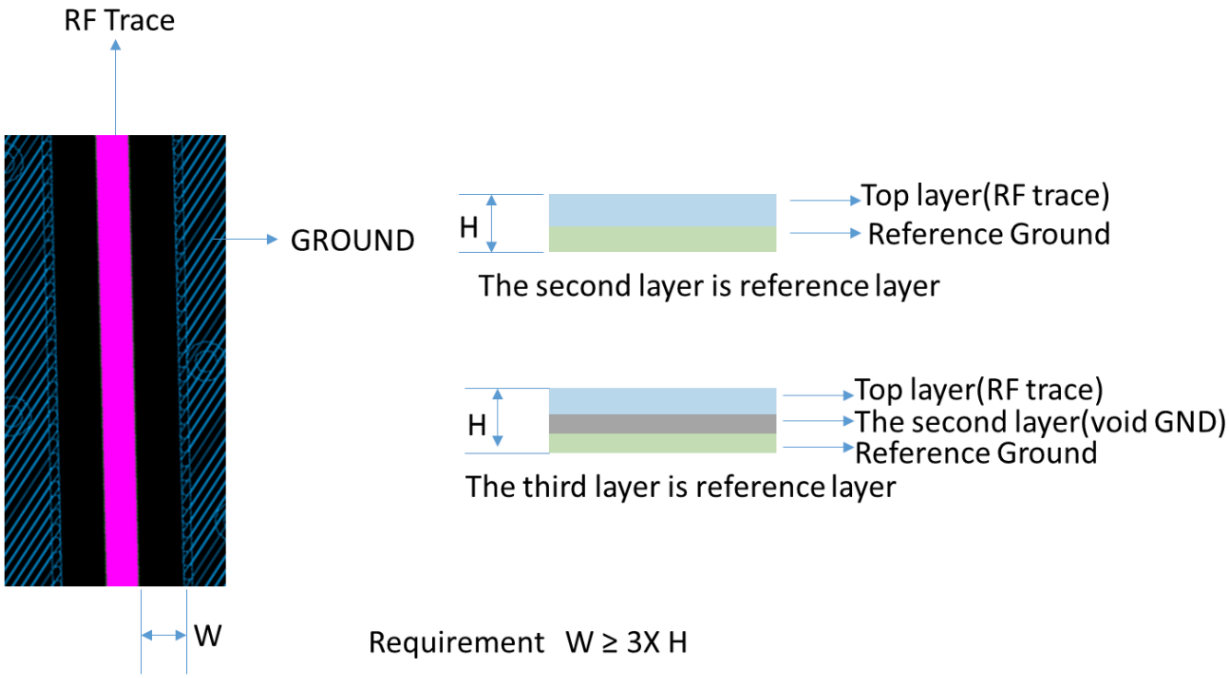

Figure 22. 3X H clearance between the ground pour and RF trace

- Keep the RF trace lengths as short as possible.
- The bend trace routing should be smooth with a large radius rather than of 90 degree with a sharp edge.

- Place stitching vias between the top and reference ground layers to increase isolation as shown in Figure 23.

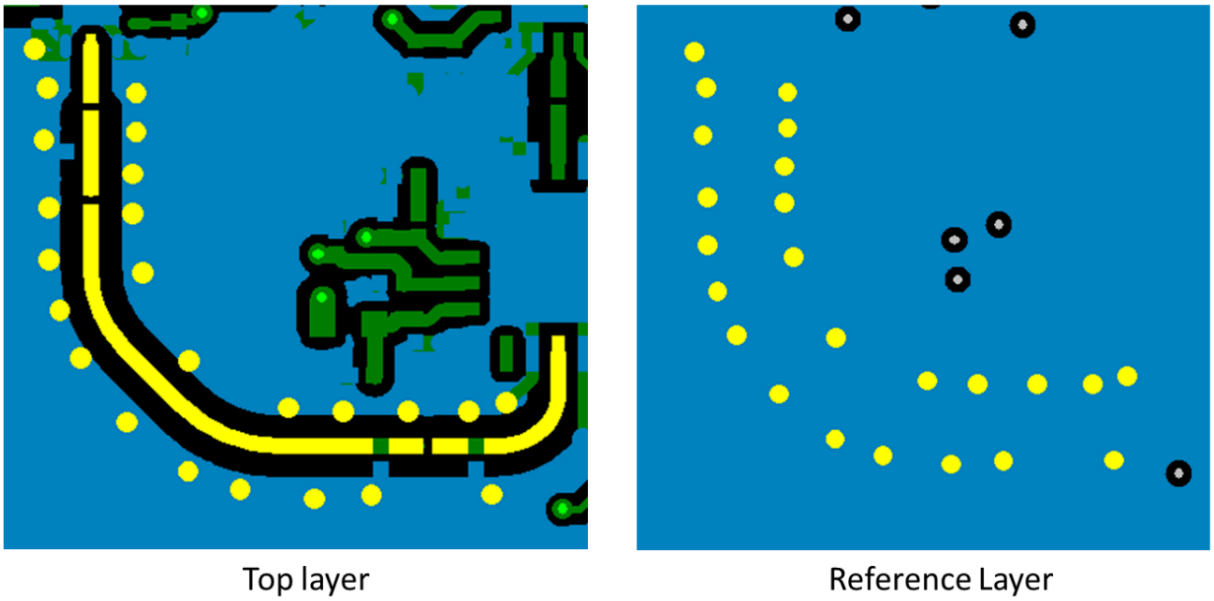

Figure 23. Ground pour with stitching vias

- Extend the ground plane between paths as much as possible. Extend the ground to the point where a ground via can be placed at the end, as shown in Figure 24.

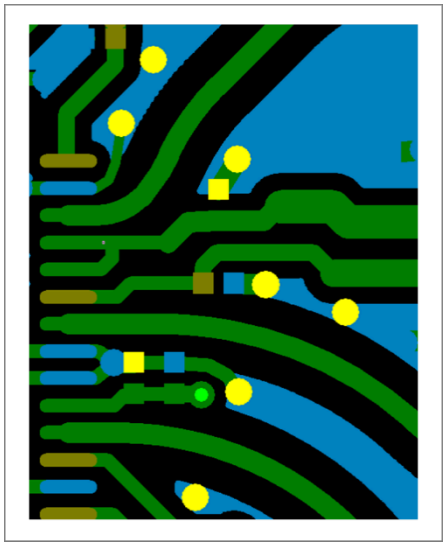

Figure 24. Ground pour along with RF trace end with a ground via

- Keep the RF control signal traces as far away as possible from the RF traces.
- Follow the manufacturer's recommendations for RF front-end parts that require matching networks.
- RF ground via along the RF shield must be less than 100 mil interval.
- Ground via must be close to the matching capacitor ground pin.

- RF trace to RF connector pad transition must be tapered to avoid discontinuity and high insertion loss, especially at 5 GHz band. An example is shown in Figure 25.

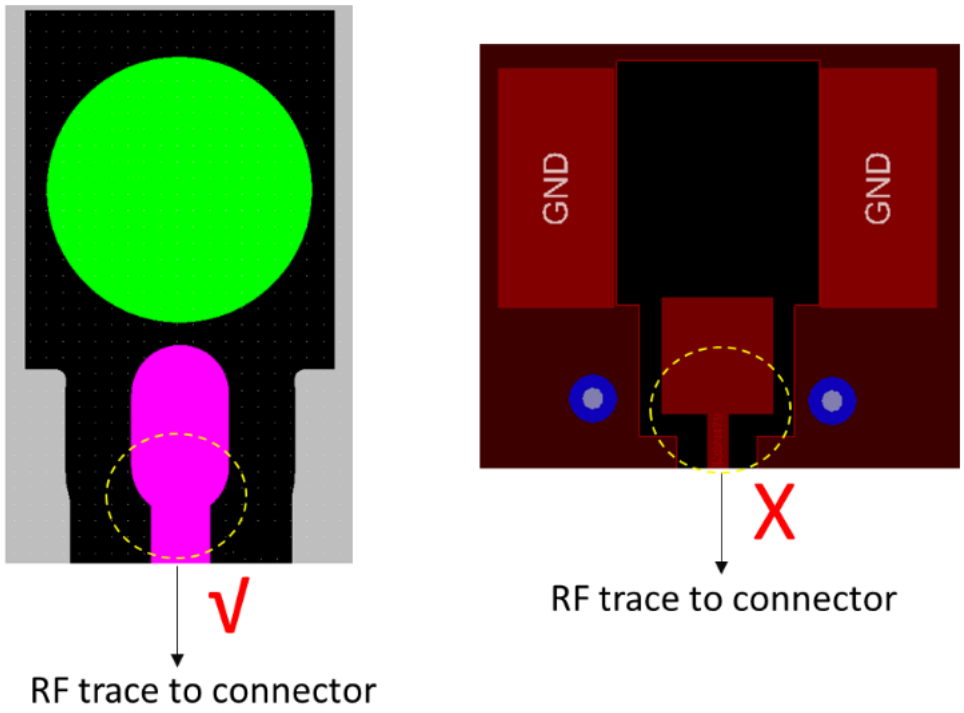

Figure 25. Taper line for RF trace to connector

- We recommend to place a non-plated through hole under the RF connector to minimize the insertion loss as shown in Figure 26.

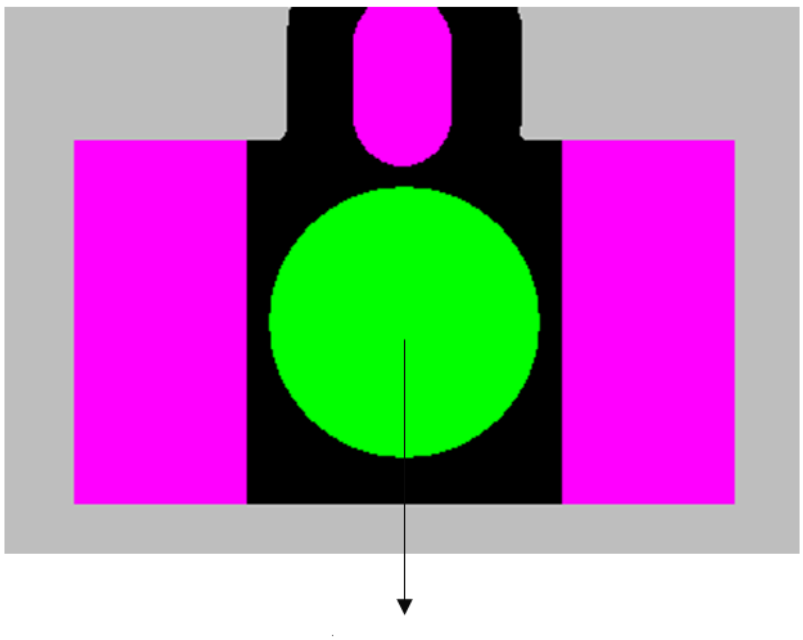

Figure 26. Non-plated through hole under the RF connector

- Add a ground via on each side of RF via near the RF trace layer transition, the distance between the via and RF trace edge to edge is about 20 mil.
- Add ground vias close to the diplexer ground pins for a good return path.
- If an ESD protection inductor is required, place the inductor close to the RF connector or close to the ESD sensitive front-end component.
- An RF shield is recommended to minimize radiated emissions and any RF interference.
- Avoid clock signal routes (system clock, SDIO_CLK, SLP_CLK) crossing the power supply traces or vice-versa.

- For QFN package only, add a ground EPAD under the package for thermal relief as shown in Figure 27.
  - Make sure the GND EPAD has a good number of thermal vias for the thermal path to be effective.

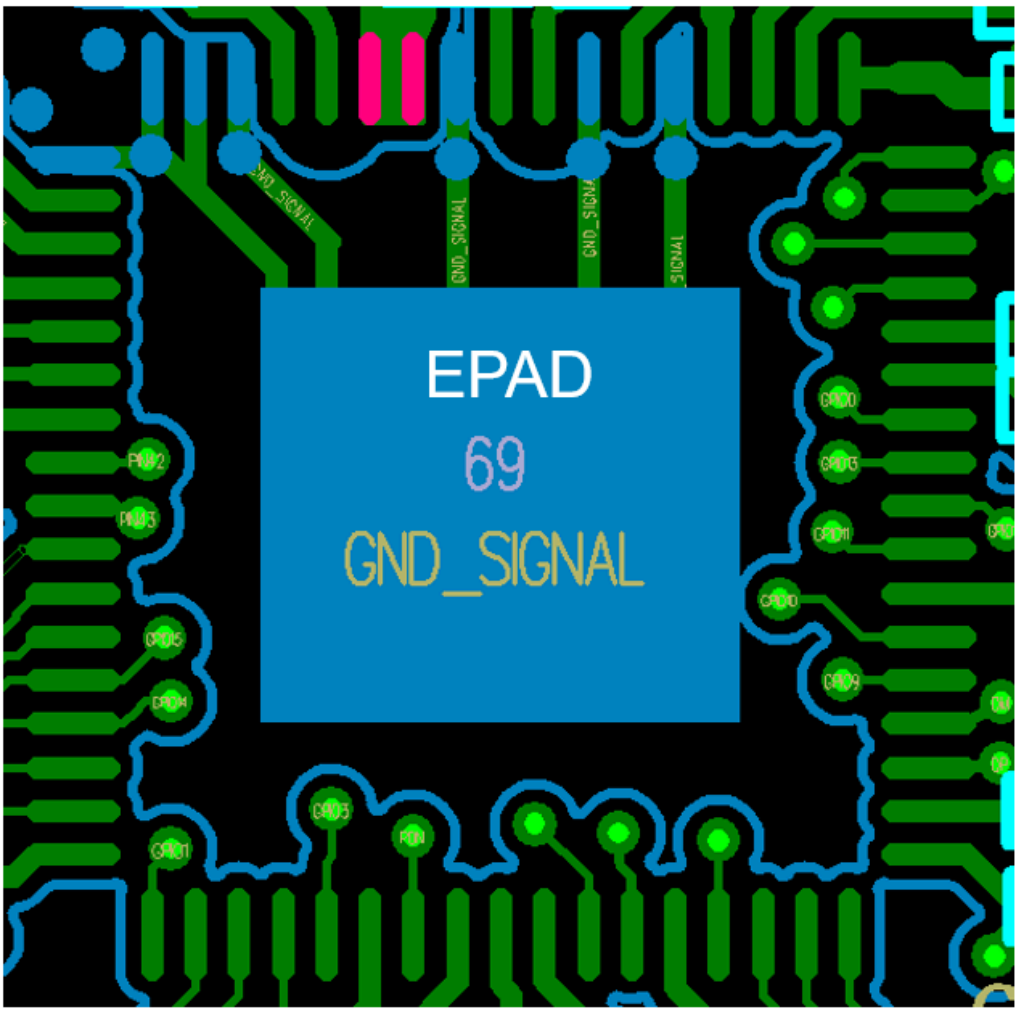

Figure 27. Ground EPAD for QFN package

- For the WLCSP package only, do not route any signal traces, power planes, ground planes over the on-chip inductor keep-out areas. The on-chip inductor keep-out areas are highlighted in Figure 28.

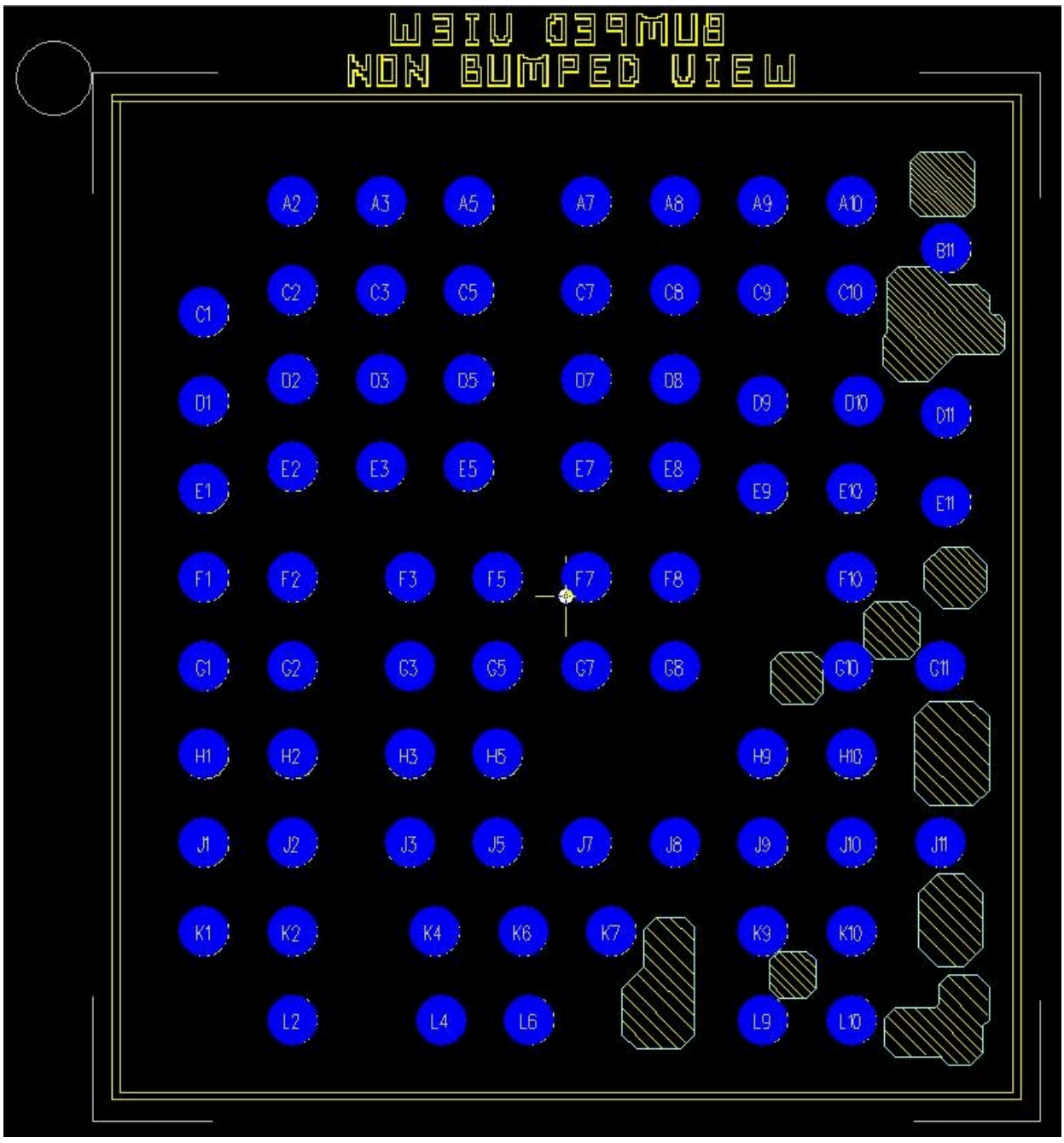

Figure 28. On-chip inductor area under WLCSP package

For additional details, refer to DXF drawing layer included in Wireless SoC WLCSP reference design PCB layout file on NXP website.

7 Miscellaneous

7.1 Unused interfaces and pins

Table 7 shows the PCB connection for unused pins.

Table 7. Unused pins

Pin name	PCB connection when not used
LDO_VIN	Connect to ground
LDO_VOUT	Keep floating/No connect
SLP_CLK_IN	Keep floating/No connect
XTAL_OUT	Connect a 100 Ω resistor to ground
RF_TR_2 or RF_TR_5 or BRF_ANT	Connect a 50 Ω resistor to ground
RF_CNTL	Keep floating/No connect
VPA	Connect to 2.2 V supply rail
VIO_SD	Connect to 1.8 V supply rail
VIO_RF	Connect to 1.8 V or 3.3 V supply rail

Table 8 shows the PCB connection for unused interfaces.

Table 8. Unused interfaces

Interface	PCB connection when not used
SDIO interface	Keep floating/No connect
UART interface	Keep floating/No connect
PCM interface	Keep floating/No connect
WCI-2 interface	Keep floating/No connect

7.2 GPIOs

Refer to IW416 data sheet for the typical function assigned to the GPIO pins.

7.3 PCB stackup

- Ensure the stackup is symmetrical.
- Ensure all layers meet specified thickness.
- For WLCSP package, NXP reference design PCB typically consists of six layers with FR-4 material and blind buried vias.
  Figure 29 shows the typical 6 layer PCB stack up for WLCSP package

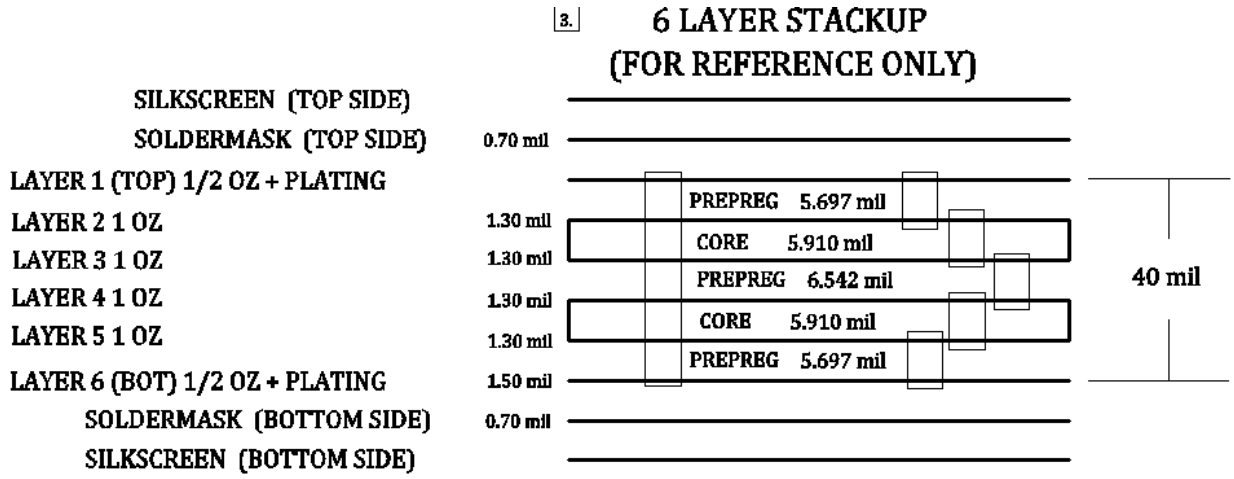

Figure 29. PCB stackup for WLCSP package

- For QFN package, NXP reference design PCB can be of four to six layers with FR-4 material and plated through hole vias
  Figure 30 shows the typical six-layer PCB stack up for QFN package.

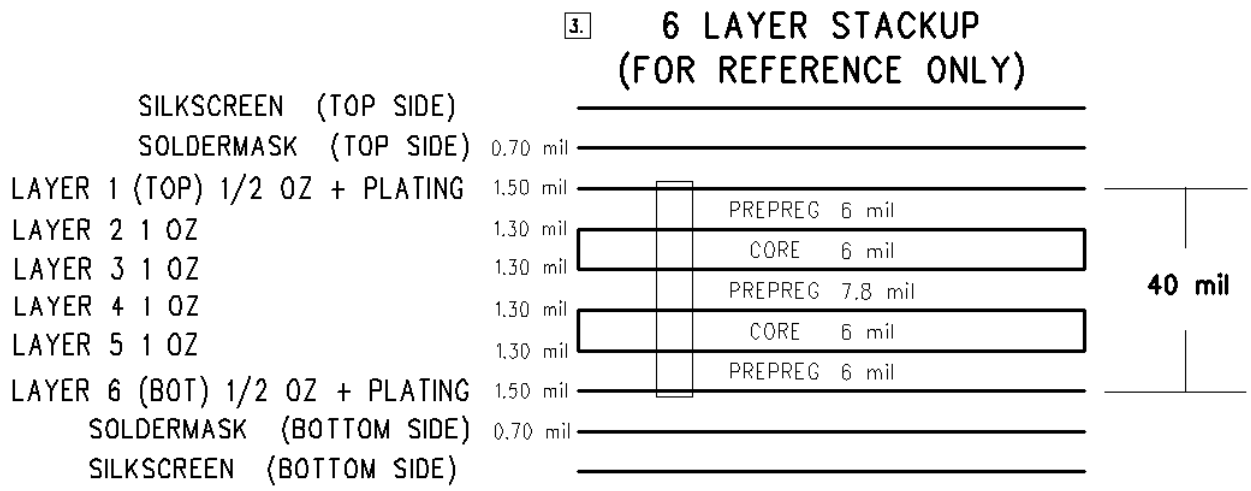

Figure 30. Six-layer PCB stackup for QFN package

Figure 31 shows the typical four-layer PCB stackup for QFN package.

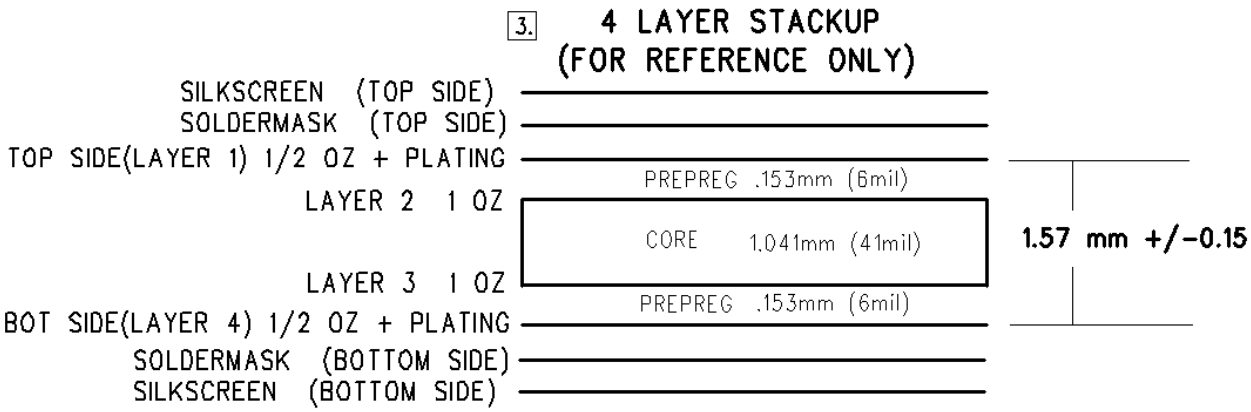

Figure 31. Four-layer PCB stackup for QFN package

- In general, RF routing is on the top layer with RF trace reference ground is on the layer 2

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Figures

Contents

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