AN13080

PCAL6524 debounce function implementation

Rev. 1.0 — 13 December 2021 Application note

Document information

Information	Content
Keywords	I^2C-bus, SMBus, PCAL6524, Agile I/O, 24-bit generator purpose I/O expansion, switch debounce, bit-wise I/O programming, POR .
Abstract	This document describes the PCAL6524 debounce function implementation which includes debounce circuitry operation mechanism, registers settings as well as power consumption explanations.

Revision history

Rev	Date	Description
v.1.0	20211213	Initial version

1 Introduction

The PCAL6524 is a 24-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I^2C-bus interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 0.8 V.

The PCAL6524 fully meets the Fm+ I^2C-bus specification at speeds to 1 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include I^2C software reset and device ID. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

This application note provides debounce circuitry operation mechanism explanations, registers setting as well as debounce circuitry measurement result.

2 Debounce circuitry operation mechanism

The PCAL6524 implements hardware state machine to ease the hardware interface by debouncing switch button with dedicated circuitry.

P0_1 to P0_7, P1_0 to P1_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods.

The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 1) shows functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output.

The first time external clock is connected, external clock is required to wait 9 clock cycles for the debounce circuit in normal operation.

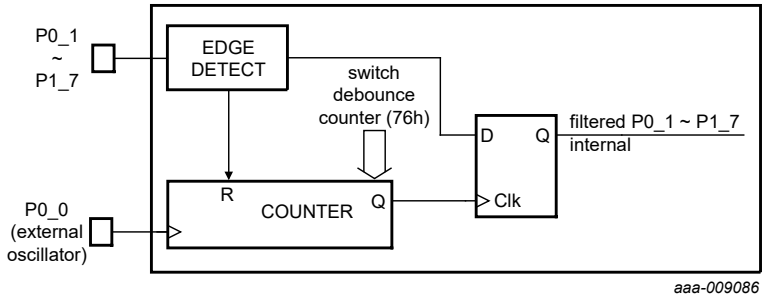

Figure 1. Debouncer block diagram

3 Debounce registers

There are three registers to be used for setting up debounce circuitry.

3.1 Switch debounce enable registers (74h, 75h)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin.

3.2 Switch debounce count register (76h)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time.

4 Debounce current and function measurement

4.1 Test setup

The measurement was done using one OM13526 board.

1. Connect OM13515 (PCA85063A eval board) 32.768 kHz clock output to OM13526 (PCAL6524 eval board) P0_0 port
2. Connect probe 1 to PCAL6524 P0_0 pin
3. Connect probe 2 to PCAL6524 /INT pin
4. Connect probe 3 to PCAL6524 P1_3 pin
5. Serial DMM to measure $I_{DD(P)}$ current on J7
6. Serial DMM to measure $I_{DD(I2C\text{-}bus)}$ current on J8

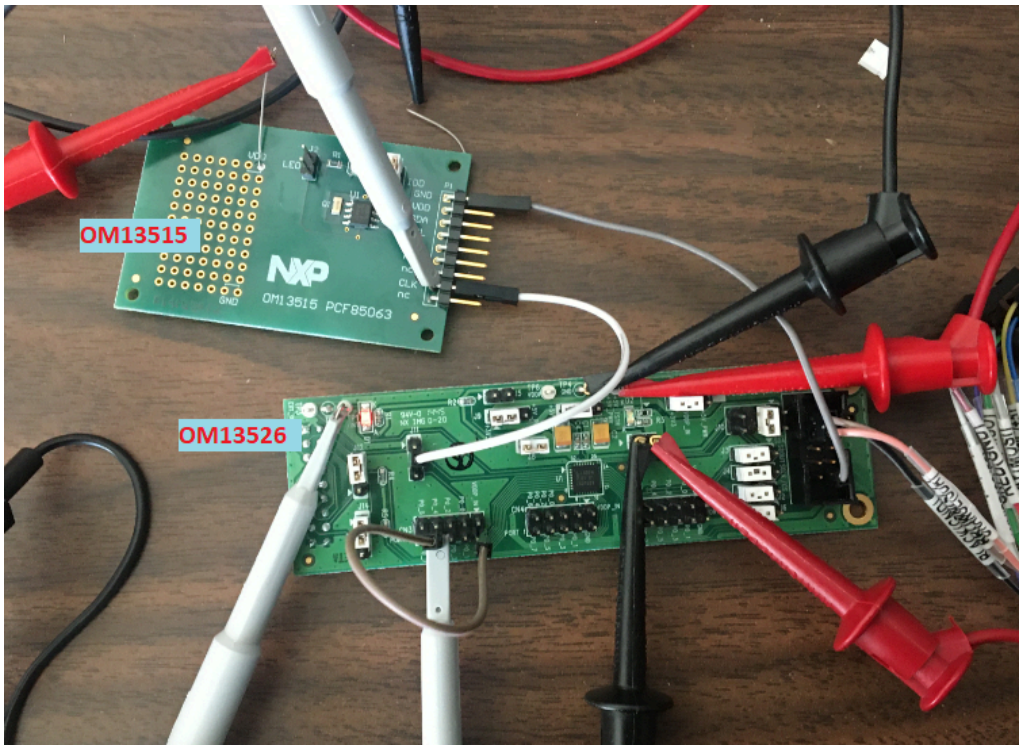

Figure 2. Test setup

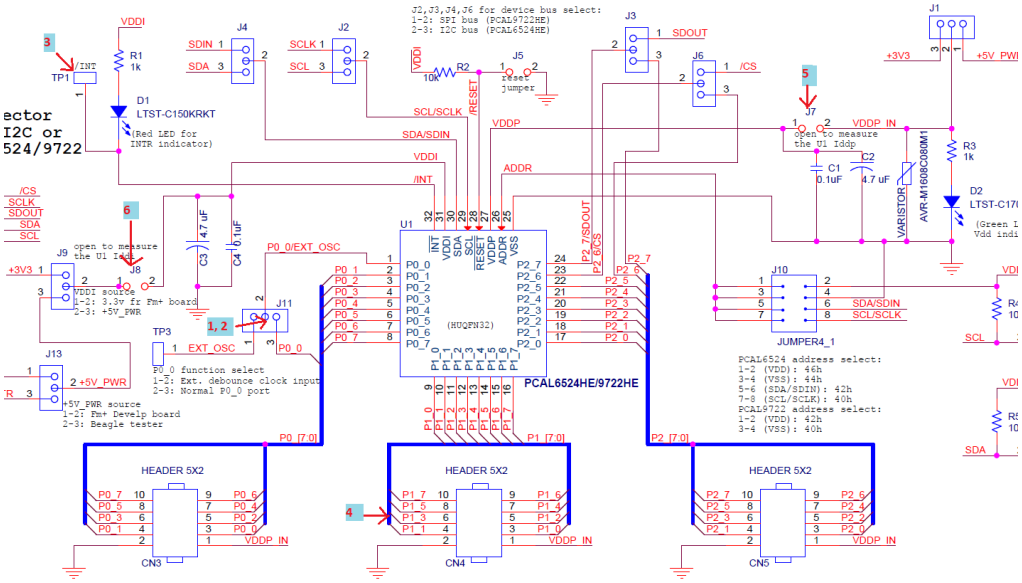

Figure 3. Schematic

4.2 Registers setting

- **Set switch debounce enable registers 0x74, 0x75 = 0xFF, 0xFF.**
  To enable the switch debounce function for Port 0 and Port 1 pins, P0_0 is designated as the oscillator input port, P0_1 – P0_7 and P1_0 – P1_7 are is designated as switch input port.
- **Set switch debounce count register 0x76 = 0x0A.**
  To enable the switch debounce function for Port 0 and Port 1 pins, P0_0 is designated as the oscillator input port, P0_1 – P0_7 and P1_0 – P1_7 are is designated as switch input port.

4.3 Current measurement data

- **$I_{DD(P)}$ and $I_{DD(I2C\text{-}bus)}$ current measurement without 32.768 kHz clock input and without debounce function enabled:**
  – PCAL6524 V_{DD} = 1.8 V, PCA85063A V_{DD} = 1.8 V

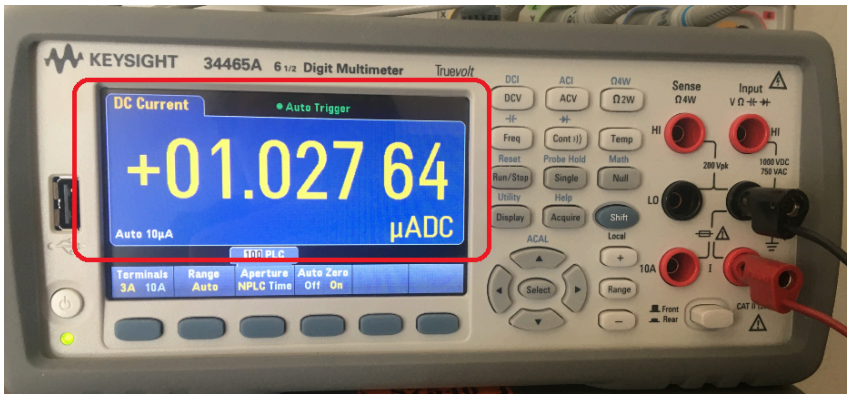

Figure 4. Serial DMM on J7; $I_{DD(P)}$ = 1.027 µA

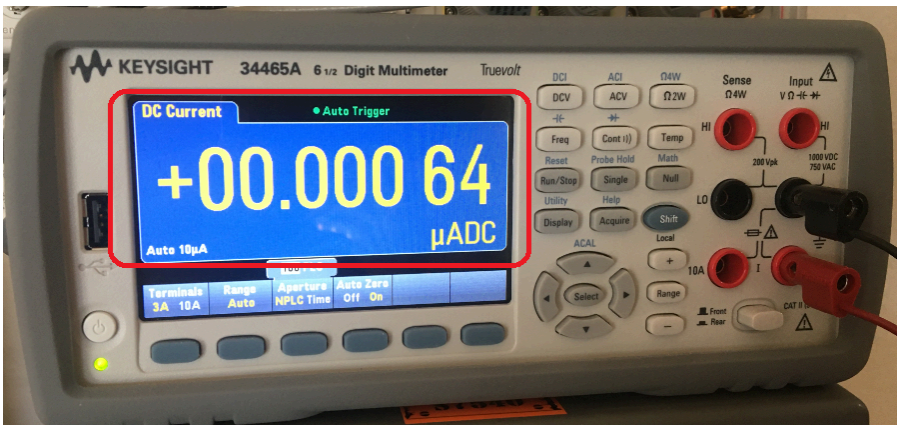

Figure 5. Serial DMM on J8; $I_{DD(I2C\text{-}bus)} \cong$ 0.001 µA (I^2C adapter is not connected to SCL/SDA)

- **$I_{DD(P)}$ and $I_{DD(I2C\text{-}bus)}$ current measurement with 32.768 kHz clock input and debounce function enabled:**
  - PCAL6524 V_{DD} = 1.8 V, PCA85063A V_{DD} = 1.8 V
  - Write register 0x0C, 0x0D to 0xFF: Set P0-1 to be input port.
  - Write register 0x74, 0x75 to 0xFF: Set P0-1 to enable debounce function.
  - Write register 0x76 to 0x0A: Set debounce counter

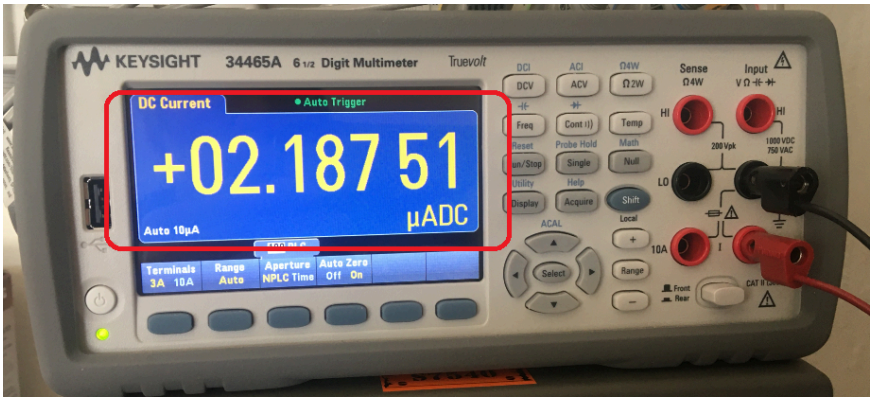

Figure 6. Serial DMM on J7; OM13515 clock output is connected to PCAL6524 P0_0 (OM13526); $I_{DD(P)}$ = 2.187 µA

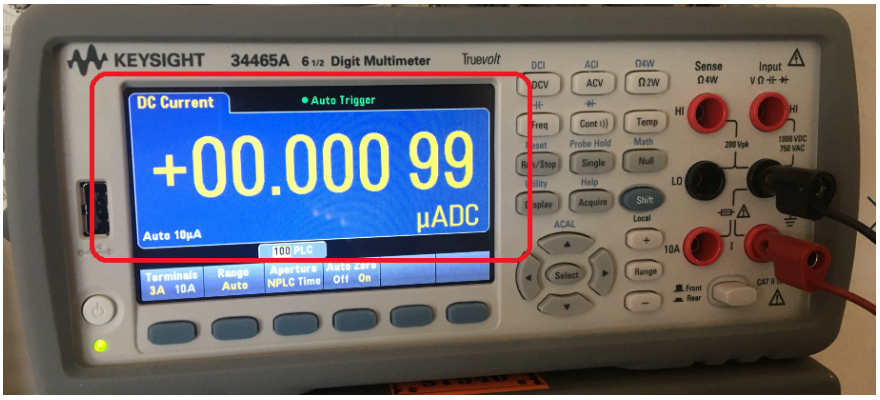

Figure 7. Serial DMM on J8; $IDD_{(I2C\text{-}bus)}$ = 0.001 µA (I^2C adapter is not connected to SCL/SDA)

4.4 Function measurement data

- Switch goes low test:
  - Connect P1_3 pin to low level, and capture waveform.
  - Probe 1 (Yellow) is 32KHz clock input to the P0_0/EXT Clk pin.
  - Probe 3 (green) shows P1_3 pin goes low level with some glitches.
  - Probe 2 (blue) shows /INT pin going low after P1_3 level stable for 10 clock cycles.

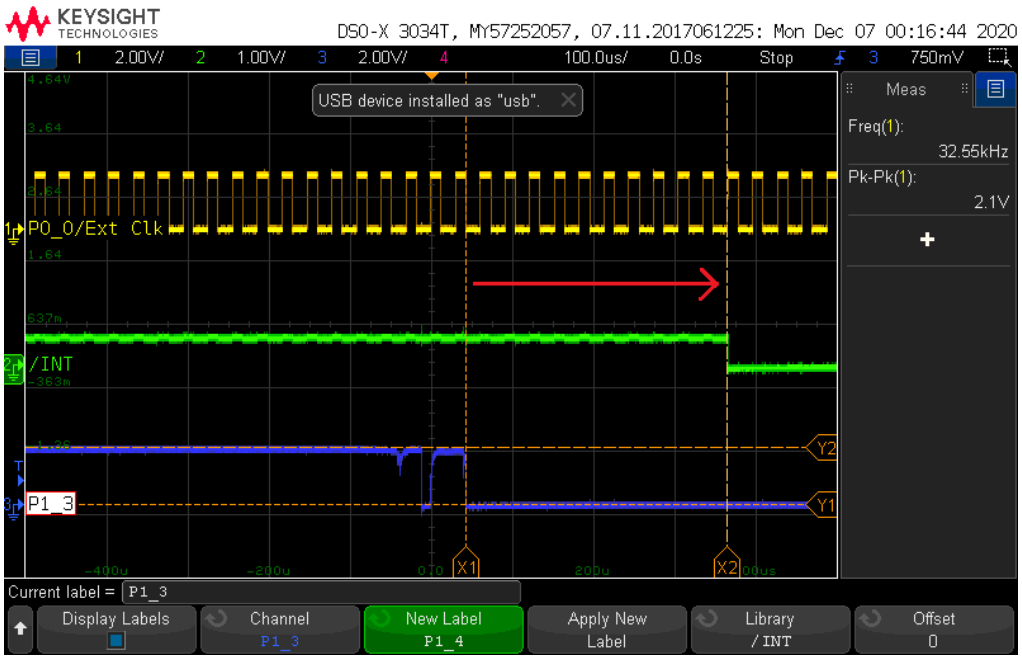

Figure 8. Switch goes low test

- Switch goes high test:
  - Connect P1_3 pin to high level, and capture waveform.
  - Probe 1 (yellow) is 32KHz clock input to the P0_0/EXT Clk pin.
  - Probe 3 (green) shows P1_3 pin goes high level with some glitches.
  - Probe 2 (blue) shows /INT pin going high after P1_3 level stable for 10 clock cycles.

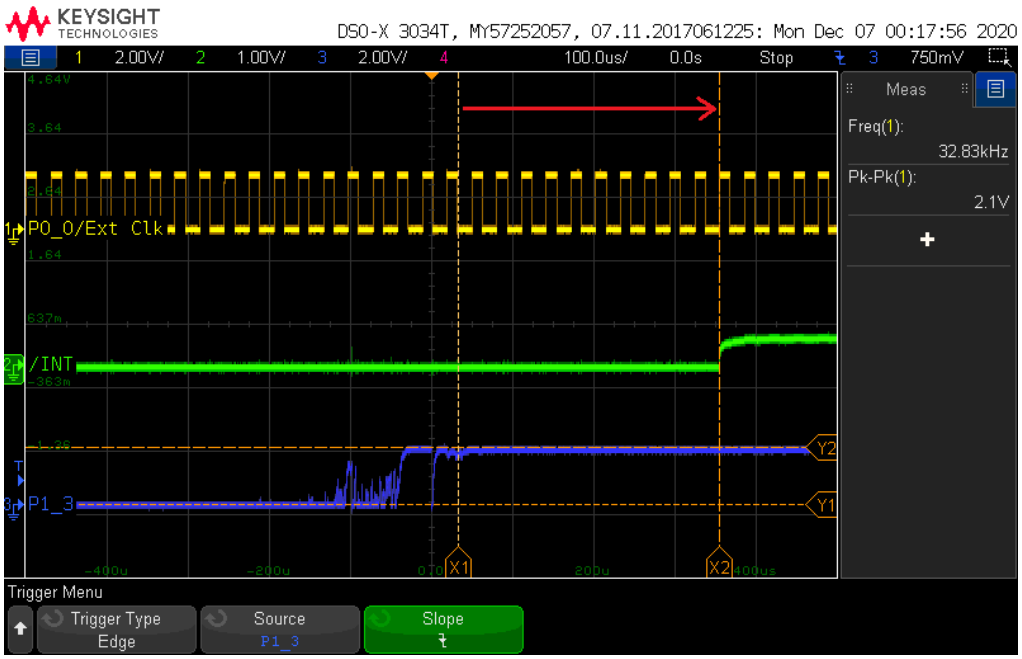

Figure 9. Switch goes high test

5 Legal information

5.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

5.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 December 2021
Document identifier: AN13080