AN12778

i.MX 8M Nano Power Consumption Measurement

Rev. 1 — 2020/7/10 Application Note

Contents

1 Introduction

This application note helps you to design power management systems. It illustrates the current drain measurements of the i.MX 8M Nano application processors taken on the NXP EVK platform through several use cases. You may choose the appropriate power supply domains for the i.MX 8M Nano processors and become familiar with the expected processor power consumption in various scenarios.

Because the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

2 Overview of i.MX 8M Nano Voltage Supplies

The i.MX 8M Nano processors have several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

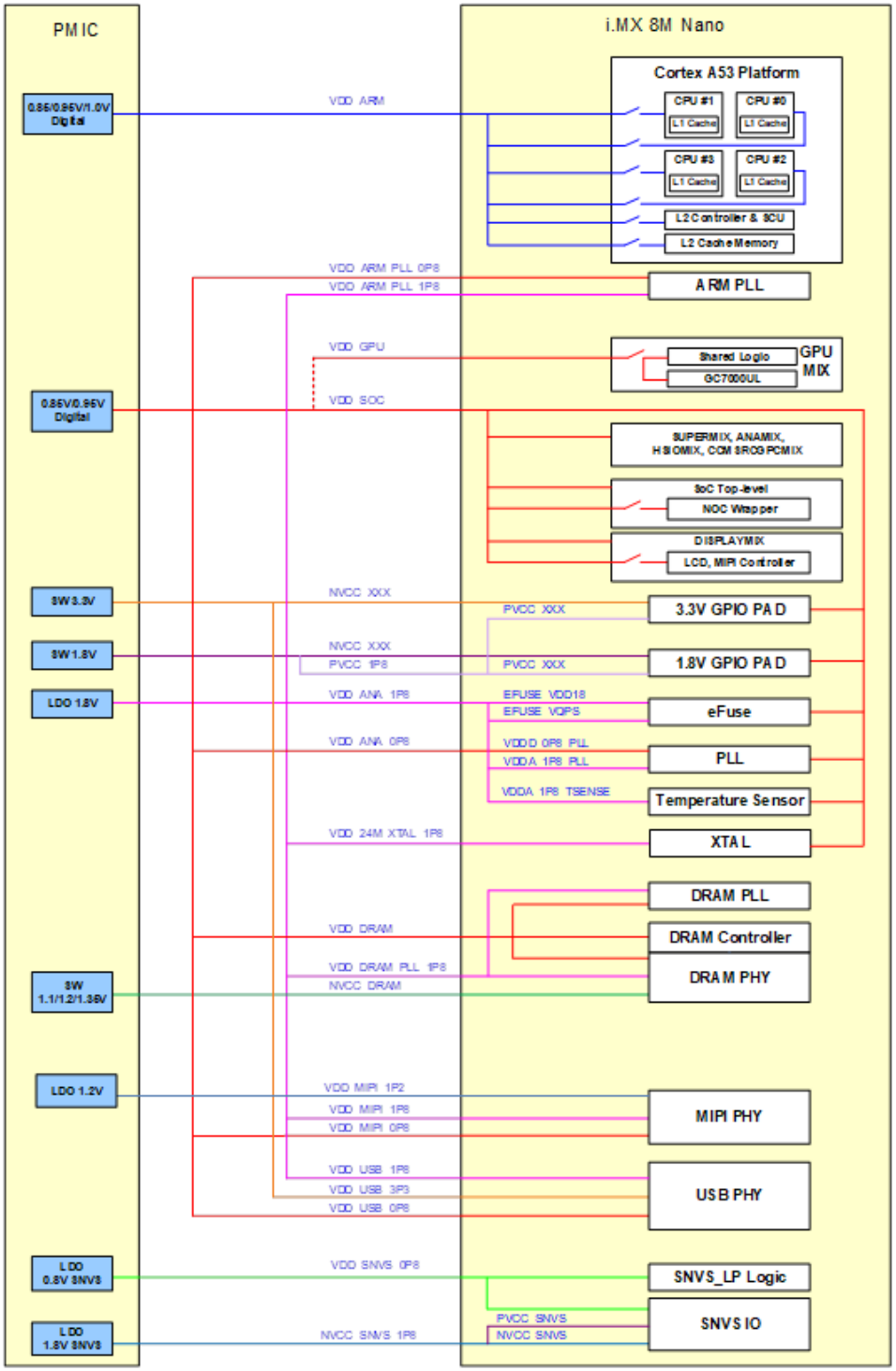

Figure 1. i.MX8M Nano power rails

NOTE

For the recommended operating conditions of each supply rail and for a detailed description of the groups of pins that are powered by each I/O voltage supply, see the *i.MX 8M Nano datasheet for consumer products*. For more information about the i.MX 8M Nano power rails, see Chapter “Power Management Unit (PMU)” in the *i.MX 8M Nano Applications Processor Reference Manual*.

Figure 2 is a snippet from the i.MX 8M Nano DDR4 EVK Board schematic showing the power distribution. The power distribution for i.MX 8M Nano LPDDR4 EVK Board schematics is same. The difference is for DDR4 board, NVCC_DRAM default power up voltage is 1.1V, and SW will configure it as 1.2V after boot up; for LPDDR4 board, NVCC_DRAM is always 1.1V.

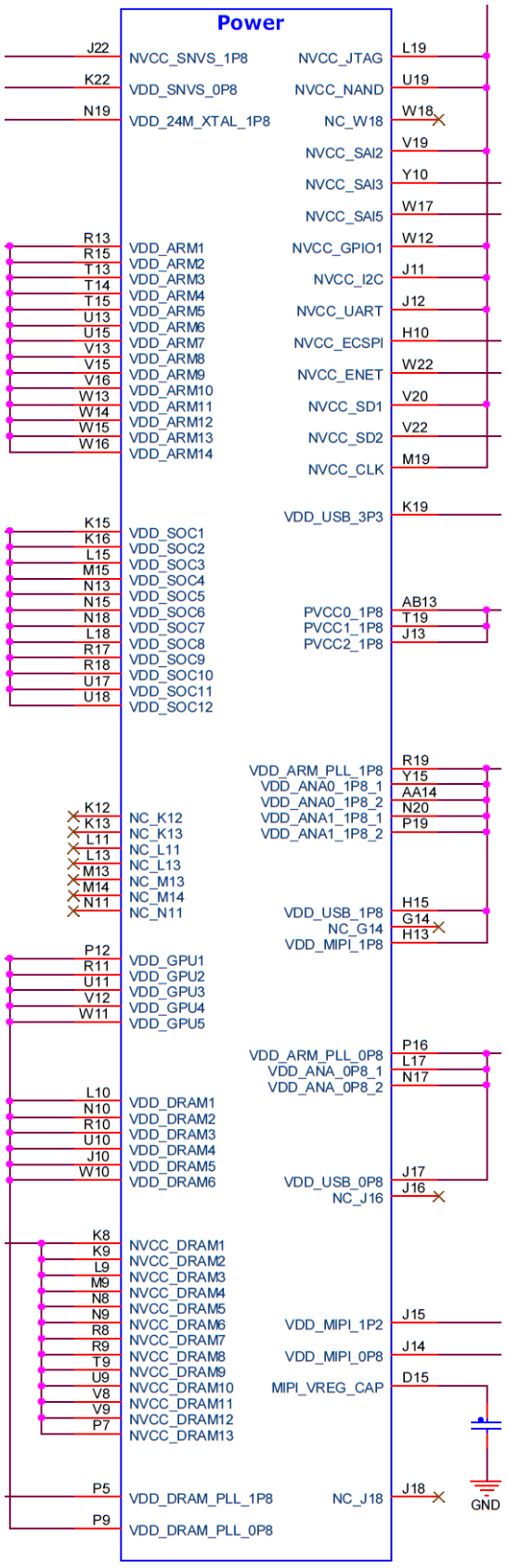

Figure 2. i.MX 8M Nano power schematic

3 Internal Power Measurement of the i.MX 8M Nano Processor

Several use cases (described in Section Use-Case Configuration and Usage Guidelines) are run on the EVK platform. The measurements are taken mainly for these power supply domains:

- VDD_ARM: Arm® Cortex®-A53 cores supply
- VDD_SOC_DRAM_GPU: SoC logic, DRAM, GPU controller and PHY digital logic, and PLL power supply
- NVCC_DRAM: DRAM IO power supply (including an external DDR device)

These supply domains consume the majority of the processor's internal power. For relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but on whether these modules are used or not. The power consumption of the SNVS is comparatively negligible (except for the Suspend mode).

The NVCC_* power consumption depends primarily on the board-level configuration and the components. Therefore, it is not included in the i.MX 8M Nano internal power analysis.

The power consumption of these supplies (in different use cases) is provided from Table 2 through Table 30.

NOTE

Unless stated, otherwise, all measurements were taken on a typical process silicon, at a room temperature (approximately 20 °C).

3.1 DDR I/O power

The DDR I/O is supplied from the NVCC_DRAM, which provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface used. The target voltages for the different DDR interfaces are:

- 1.35 V for DDR3L
- 1.2 V for DDR4
- 1.1 V for LPDDR4

The power consumption of the NVCC_DRAM supply is affected by various factors, including:

- The amount of activity on the DDR interface
- On-Die Termination (ODT): enabled/disabled, termination value, which is used for the DDR controller and the DDR memories
- Board termination for the DDR control and the address bus
- Configuration of the DDR pads (such as the drive strength)
- Board layout
- Load of the DDR memory devices

NOTE

Due to the factors specified in the previous paragraph, the measurements provided in the following tables vary from one system to another. The provided data is the average data but not peak data, and for guidance only and should not be treated as a specification.

The measured current on the EVK Platform also includes the current of the on-board DDR4/LPDDR4 memory device.

3.2 Voltage levels in the measurement process

The voltage levels of all the supplies (except for VDD_ARM, VDD_SOC, VDD_GPU and VDD_DRAM) are set to the typical voltage levels, as defined in the *i.MX 8M Nano Data Sheet for Consumer Products*.

The VDD_SOC, VDD_GPU and VDD_DRAM supplies are required to be tied together and keep the same voltage or grounded.

3.2.1 VDD_ARM/VDD_SOC/VDD_GPU/VDD_DRAM voltage levels

The target voltage levels of the VDD_ARM, VDD_SOC, VDD_GPU may vary for different modes according to the use cases. The modes are the nominal mode and the overdrive mode. There are several factors that contribute to the mode decisions, with the module load being the most important. The other factors are module latency requirements, thermal restrictions, and peripheral I/O performance requirements. The voltage levels used for the measurements are listed in Table 1:

Table 1. VDD_ARM/VDD_GPU/VDD_VPU/VDD_DRAM voltage levels (for reference only)

Power rail	Vmin (V)	Vtyp (V)	Vmax (V)	Description
VDD_ARM	0.760	0.800	0.850	Lowdrive Mode
	0.805	0.850	0.950	Nominal mode
	0.900	0.950	1.000	Overdrive mode
	0.950	1.000	1.050	1.0V mode
VDD_SOC	0.760	0.800	0.850	Lowdrive Mode
	0.805	0.850	0.900	Nominal mode
	0.900	0.950	1.000	Overdrive mode
VDD_GPU	0.760	0.800	0.850	Lowdrive Mode
	0.805	0.850	0.900	Nominal mode
	0.900	0.950	1.000	Overdrive mode
VDD_DRAM	0.760	0.800	0.850	Power supply for DDRC, 0.80 V supports up to 800 MHz (DDR clock)
	0.805	0.850	0.900	Power supply for DDRC, 0.85 V supports up to 1.2 GHz (DDR clock)
	0.900	0.950	1.000	Power supply for DDRC, 0.95 V supports up to 1.6 GHz (DDR clock)

NOTE

For the official operating points, see the operating ranges table in the *i.MX 8M Nano Data Sheet for Consumer Products*.

VDD_SOC, VDD_GPU, VDD_DRAM, VDD_DRAM_PLL_0P8, VDD_ARM_PLL_0P8, VDD_ANA_0P8, VDD_USB_0P8 and VDD_MIPI_0P8 are combined on the EVK board, due to the consideration of simplified board design.

Most of the measurements are performed using these voltage levels and the power data that appears in this document is in accordance with these values. If the measurement is done at different voltage levels, the power consumption scales change with the voltage. In real applications, the software (in conjunction with the hardware) automatically adjusts the voltage and frequency values based on the use-case requirements.

The voltage used for the power calculation is the average voltage between those setpoints. It depends on the amount of time spent at each setpoint.

3.3 Temperature measurements

In some use cases, the die temperature is measured. The temperature measurements were done using the on-chip temperature sensor. When measuring the temperature, it is recommended to wait until the temperature stabilizes.

NOTE

The measured temperatures are for reference only and vary on different systems due to the differences in the board, enclosure, and heat spreading techniques. When using the same board type, the measured temperature may vary due to factors such as environment, silicon variations, and measurement errors.

3.4 Hardware and software used

The software versions used for the measurements are:

- i.MX 8M Nano Rev.A DDR4 EVK platform with latest SW release: Linux® Kernel version: *L 4.14.98_2.3.2 i.MX8MNano RC1*
- i.MX Nano Rev.A LPDDR4 EVK platform with latest SW release: Linux® Kernel version: *L 5.4.24_2.1.0 i.MX8MNano RC2*
- The measurements were performed using the 34470A 6½ digital multimeter.

3.5 Measuring points on the EVK platform

To measure the power consumption, do the rework first. Split the connection between the PMIC and CPU, and then solder a 0.025 Ω sensor resistor in series. The power data is obtained by measuring the average voltage drop over the measurement points and dividing it by the resistor value to determine the average current. The tolerance of the 0.025 Ω resistors you use should be 1 % or less. The measuring points for the various supply domains are as follows:

- VDD_ARM: A53 Arm complex current for low-power measurements. The resistance value is 0.025 Ω.
- VDD_SOC_DRAM_GPU: Chip domain current for SOC, GPU and DRAM. The recommended resistance value for this measurement is 0.025 Ω.
- DRAM I/O plus memory: Current in this domain includes the NVCC_DRAM current and the overall current of the on-board DRAM memory device. The recommended resistance value for this measurement is 0.025 Ω.

4 Use Cases and Measurement Results

The main use cases and subtypes that form the benchmarks for the i.MX 8M Nano internal power measurements on the EVK platform are described in the following sections.

A 1080p TV display was used only for the GPU and video playback use cases.

NOTE

For all use cases, platform is booted from an SD card with the default dtb configuration in the U-Boot stage.

For DDR4 EVK Board, to check whether the default dtb file is fsl-imx8mn-ddr4-evk.dtb for DDR4 EVK Board:

```
printenv fdt_file
```

For LPDDR4 EVK Board, to check whether the default dtb file is fsl-imx8mn-lpddr4-evk.dtb for LPDDR4 EVK Board:

```
printenv fdt_file
```

If the default dtb file isn't fsl-imx8mn-lpddr4-evk.dtb, set it as below :

```
setenv fdt_file "fsl-imx8mn-lpddr4-evk.dtb"
saveenv
```

4.1 Low-power mode use cases

These use-case scenarios were tested:

- Suspend mode
- IDLE_DEFAULT
- IDLE_DDRC_266MHz on DDR4 EVK Board
- IDLE_DDRC_25MHz on LPDDR4 EVK Board

NOTE

For DDR4 EVK Board, IDLE_DDRC_266MHz is to set DDR PLL Clock as 266MHz, and the DDR clock is 533MHz

For LPDDR4 EVK Board, IDLE_DDRC_25MHz is to disable PLL and use DDR bypass Clock as 50MHz, and the DDR clock is 50MHz.

DDR data rate is 2:1 for DDR clock. For example, DDR clock at 533MHz means 1066MTS.

4.1.1 Suspend mode

This mode is called either "Dormant mode" or "Deep sleep mode" in the Linux BSP. This is the lowest possible power state where the external supplies are still on.

The use case is as follows:

- The Arm platform is power-gated.
- The L2 Cache peripherals are power-gated.
- The Arm Cortex-M7 is in the reset status.
- All PLL (Phase-Locked Loop) and CCM (Clock Controller Module) generated clocks are off.
- The CKIL (32 kHz) input is on.
- All modules are disabled.
- The external high-frequency crystal and the on-chip oscillator are powered down (by asserting the SBYOS bit in the CCM).

Table 2 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 2. Suspend Mode

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	0.001	0.500	0.000	0.001	0.678	0.001
VDD_SOC_DRAM_GPU	0.855	5.117	4.376	0.852	5.464	4.654
NVCC_DRAM	1.199	5.433	6.513	1.098	1.984	2.179
Total power	—	—	10.889			6.834

For more details about this use case and settings, see Section Use-Case Configuration and Usage Guidelines.

4.1.2 IDLE_DEFAULT

For this use case, a MIPI-DSI-to-HDMI card adapter was connected to the EVK DSI port and no display was attached to the MIPI-DSI card port.

The use case is as follows:

- The CPU frequency is set to 1200 MHz (default).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The GPU, and DISPMIX are in low-power mode.
- The operating system is on.
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 3 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 3. IDLE_DEFAULT

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	0.861	5.764	4.960	0.852	6.883	5.863
VDD_SOC_DRAM_GPU	0.856	365.390	312.788	0.955	487.948	466.033
NVCC_DRAM	1.199	50.931	61.079	1.097	30.871	33.880
Total power	—	—	378.827			505.777

1. The die temperature was not logged because it impacts the default governor (conservative) and sets the CPU clock frequency to 1.2 GHz.

For more details about this use case and settings, see Section Use-Case Configuration and Usage Guidelines.

4.1.3 IDLE_DDRC_266MHz on DDR4 EVK Board

For this use case, a MIPI-DSI-to-HDMI card adapter was connected to the EVK DSI port and no display was attached to the MIPI-DSI card port.

The use case is as follows:

- The CPU frequency governor is set to `powersave` (The CPU frequency is set to the minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 266 MHz.

Table 4 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 4. IDLE_DDRC_266MHz for DDR4 EVK Board

Supply domain	Voltage (V)	L4.14.98-MX8MN-DDR4	
		I (mA)	P (mW)
VDD_ARM	0.861	5.580	4.803
VDD_SOC_DRAM_GPU	0.854	198.515	169.439
NVCC_DRAM	1.198	32.793	39.292
Total power	—	—	213.534

1. The die temperature was not logged because it impacts the default governor (conservative) and sets the CPU clock frequency to 1.2 GHz.

For more details about this use case and settings, see Section Use-Case Configuration and Usage Guidelines.

4.1.4 IDLE_DDRC_25MHz on LPDDR4 EVK Board

For this use case, a MIPI-DSI-to-HDMI card adapter was connected to the EVK DSI port and no display was attached to the MIPI-DSI card port.

The use case is as follows:

- The CPU frequency governor is set to `powersave` (The CPU frequency is set to the minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 25 MHz.

Table 5 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 5. IDLE_DDRC_25MHz for LPDDR4 EVK Board

Supply domain	Voltage (V)	L4.14.98-MX8MN-LPDDR4	
		I (mA)	P (mW)
VDD_ARM	0.852	7.086	6.039
VDD_SOC_DRAM_GPU	0.953	107.297	102.250
NVCC_DRAM	1.098	18.661	20.485
Total power	—	—	128.774

1. The die temperature was not logged because it impacts the default governor (conservative) and sets the CPU clock frequency to 1.2 GHz.

For more details about this use case and settings, see Section Use-Case Configuration and Usage Guidelines.

4.2 Audio_Playback, M7 idle

These use-case scenarios were tested:

- Audio_Playback(gplay)
- Audio_Playback(gplay)_DDRC_266MHz on DDR4 EVK Board
- Audio_Playback(gplay)_DDRC_25MHz on LPDDR4 EVK Board
- Audio+Video_Playback(gplay)
- Audio+Video_Playback_Stream(gplay)

4.2.1 Audio_Playback(gplay)

The audio file used was an mp3 file with a 128-kbps bitrate and a 44 kHz sample rate/s, played using the following options:

```
gplay-1.0 $audio_file
```

The use case is as follows:

- The CPU frequency governor is set to *performance* (The CPU frequency is set to the maximum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- The GPU, and DISPMIX are in low power mode.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz.

Table 6 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 6. Audio_Playback(gplay)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	38.143	38.380	1.003	29.682	29.773
VDD_SOC_DRAM_GPU	0.857	386.657	331.231	0.955	499.328	476.943
NVCC_DRAM	1.200	61.440	73.713	1.098	40.084	43.993
Total power	—	—	443.324			550.709
Die Avg Temperature (**°C**)			42			41

1. The ambient temperature was approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the audio file was playing.

For more details about this use case and settings, see Section Use-Case Configuration and Usage Guidelines.

4.2.2 Audio_Playback(gplay)_DDRC_266MHz on DDR4 EVK Board

For this use case, DDRC clock frequency was set to 266 MHz, as specified in Section Use-Case Configuration and Usage Guidelines.

The audio file used was an mp3 file with a 128-kbps bitrate and a 44kHz sample rate/s, played using the following options.

```
gplay-1.0 $audio_file
```

The use case is as follows:

- The CPU frequency governor is set to `powersave` (CPU frequency is set to minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- The VPU, GPU, and DISPMIX are in low power mode.
- All the unused PLLs are OFF and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 266 MHz.

Table 7 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 7. Audio_Playback(gplay)_DDRC_266MHz on DDR4 EVK Board

Supply domain	Voltage (V)	L4.14.98-MX8MN-DDR4	
		I (mA)	P (mW)
VDD_ARM	0.859	26.028	22.366
VDD_SOC_DRAM_GPU	0.854	222.982	190.422

Table continues on the next page...

Table 7. Audio_Playback(gplay)_DDRC_266MHz on DDR4 EVK Board (continued)

Supply domain	Voltage (V)	L4.14.98-MX8MN-DDR4	
		I (mA)	P (mW)
NVCC_DRAM	1.199	46.920	56.263
Total power	—	—	269.051

1. The die temperature was approximately **X°C** (avg.). The ambient temperature was approximately **20 °C**.

cat/sys/class/thermal/thermal_zone0/temp was used to log the temperature while the audio file was playing.

4.2.3 Audio_Playback(gplay)_DDRC_25MHz on LPDDR4 EVK Board

For this use case, DDRC clock frequency was set to 25 MHz, as specified in Section Use-Case Configuration and Usage Guidelines.

The audio file used was an mp3 file with a 128-kbps bitrate and a 44kHz sample rate/s, played using the following options.

```
gplay-1.0 $audio_file
```

The use case is as follows:

- The CPU frequency governor is set to *powersave* (CPU frequency is set to minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- The GPU, and DISPMIX are in low power mode.
- All the unused PLLs are OFF and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 25 MHz.

Table 8 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 8. Audio_Playback(gplay)_DDRC_25MHz on LPDDR4 EVK Board

Supply domain	Voltage (V)	L4.14.98-MX8MN-LPDDR4	
		I (mA)	P (mW)
VDD_ARM	0.852	47.023	40.076
VDD_SOC_DRAM_GPU	0.953	177.067	168.825
NVCC_DRAM	1.098	66.497	73.014
Total power	—	—	281.916

1. The die temperature was approximately **X °C** (avg.). The ambient temperature was approximately **20 °C**.

cat/sys/class/thermal/thermal_zone0/temp was used to log the temperature while the audio file was playing.

4.2.4 Audio+Video_Playback(gplay)

For this use case, the MIPI-DSI port was connected to a 1080p TV display.

The video file used for playback was a mkv file format compressed using the HEVC standard with full HD resolution at 29.97 fps and the audio encoding was AACL with a 44.1-kHz sample rate in a 2-channel configuration.

The video file was locally played using gplay, with the following options:

```
gplay-1.0 $path/$FILE
```

The use case is as follows:

- The CPU frequency governor is set to **performance** (The CPU frequency is set to the maximum value).
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are OFF and the unused clocks are gated.
- The operating system is on.

Table 9 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 9. Audio+Video_Playback(gplay)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	39.035	39.263	1.003	36.698	36.818
VDD_SOC_DRAM_GPU	0.858	444.825	381.695	0.956	561.221	536.605
NVCC_DRAM	1.201	121.627	146.105	1.098	114.855	126.115
Total power	—	—	567.063			699.538
Die Avg Temperature (**°C**)			42			49

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.2.5 Audio+Video_Playback_Stream(gplay)

For this use case, MIPI-DSI port was connected to a 1080p TV display.

The video file used for playback was mkv file format compressed using the HEVC standard with full HD resolution at 29.97 fps and the audio encoding was AACL in a 2-channel configuration with 44.1 kHz samples/s.

A server was setup to host the mkv video file for streaming.

The video streaming was done using an Ethernet adapter and the player was gplay:

```
gplay-1.0 $FILE
```

The use case is as follows:

- The CPU frequency governor is set to **performance** (The CPU frequency is set to the maximum value).
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are OFF and the unused clocks are gated.

- The operating system is on.

Table 10 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 10. Audio+Video_Playback_Stream(gplay)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	24.268	24.413	1.0032	12.9574	12.999
VDD_SOC_DRAM_GPU	0.858	456.359	391.617	0.9560	573.0397	547.815
NVCC_DRAM	1.201	118.969	142.895	1.0979	112.3750	123.374
Total power	—	—	558.925			684.188
Die Avg Temperature (**°C**)			45			42

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.3 Core benchmark

These use-case scenarios were tested:

- 4-core Dhrystone
- 4-core Whetstone
- Coremark

4.3.1 4-core Dhrystone

Dhrystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhrystone benchmark enables it to fit into the L1 cache and minimizes accesses to the L2 cache and DDR.

In this use case, the Dhrystone test is performed by 4 Cortex-A53 cores (because dhrystone is a single thread benchmark, 4 instances were started). All Cortex-A53 cores run the test in a loop at a frequency of 1500 MHz.

- The DDRC clock for DDR4 is 600 MHz, for LPDDR4 is 800MHz
- The NOC clock is 600 MHz
- The AXI clock is 333 MHz.
- The AHB clock is 133 MHz.
- The IPG clock is 67 MHz.
- CPU frequency governor is set to `performance` (CPU frequency is set to maximum value).

Table 11 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 11. Dhrystone

Supply domain	L4.14.98-MX8MN-DDR4			L4.14.98-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	1031.830	1036.999	1.008	1023.588	1032.215
VDD_SOC_DRAM_GPU	0.857	396.970	340.240	0.957	516.565	494.121
NVCC_DRAM	1.200	53.941	64.748	1.099	32.203	35.389
Total power	—	—	1441.987			1561.725
Die Avg Temperature (**°C**)			51			57

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.3.2 4-core Whetstone

Whetstone is a similar benchmark for integer and string operations like Dhrystone. The Whetstone is also a synthetic benchmark which primarily measures the floating-point arithmetic performance.

In this use case, the Whetstone test is performed by 4 Cortex-A53 cores (because Whetstone is a single thread benchmark too, 4 instances were started). All Cortex-A53 cores run the test in a loop at a frequency of 1500MHz.

- CPU frequency governor is set to `performance` (CPU frequency is set to maximum value).
- The DDRC clock for DDR4 is 600 MHz, for LPDDR4 is 800MHz

Table 12 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 12. Whetstone

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	740.929	745.377	1.007	713.784	718.709
VDD_SOC_DRAM_GPU	0.857	391.638	335.613	0.956	507.618	485.330
NVCC_DRAM	1.200	52.836	63.404	1.098	31.695	34.809
Total power	—	—	1144.394			1238.848
Die Avg Temperature (**°C**)			54			52

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.3.3 Coremark

Coremark is a modern, sophisticated benchmark that lets you accurately measure the processor performance and is intended to replace the older Dhrystone benchmark. Arm recommends using Coremark over Dhrystone.

For the best performance, compile as follows:

```
-O2 -DMULTITHREAD=4 -DUSE_PTHREAD -lpthread -O3 -funroll-all-loops  --param max-inline-insns-auto=550
-ftracer -falign-jumps=16 -ftree-loop-im -fivopts  -ftree-loop-ivcanon -fvect-cost-model -fvariable-
expansion-in-unroller  --param max-unrolled-insns=999999 --param max-average-unrolled-insns=99999999
--param iv-max-considered-uses=9999999 --param iv-consider-all-candidates-bound=99999  --param iv-
always-prune-cand-set-bound=999999   -fmodulo-sched  -fmodulo-sched-allow-regmoves -fgcse-lm -fgcse-
sm -fgcse-las -funsafe-loop-optimizations -freschedule-modulo-scheduled-loops  -ftree-vectorize -
DPERFORMANCE_RUN=1   -lrt
```

- The CPU frequency governor is set to *performance* (The CPU frequency is set to the maximum value).
- The DDRC clock for DDR4 is 600 MHz, for LPDDR4 is 800MHz

Table 13 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 13. Coremark

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	847.006	851.609	1.007	832.677	838.855
VDD_SOC_DRAM_GPU	0.858	455.887	391.335	0.956	510.245	487.999
NVCC_DRAM	1.202	119.759	143.907	1.098	31.732	34.854
Total power	—	—	1386.851			1361.708
Die Avg Temperature (**°C**)			54			53

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.4 GPU

These use-case scenarios were tested:

- MM07
- MM06
- GPU_Kanzi
- GPU_GLmark

MM07 and MM06 are 3D-gaming benchmarks. The graphics are loaded from the SD card into the DDR (Double Data Rate) memory, processed by GPU3D, and copied to a display buffer in the DDR memory. It is displayed on the1080p display (through MIPI-DSI).

- The CPU frequency governor is set to *performance* (The CPU frequency is set to the maximum value).
- The DDRC frequency DDR4 is 600 MHz, for LPDDR4 is 800MHz

4.4.1 GPU_MM07

Table 14 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 14. GPU_MM07

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	63.197	63.590	1.004	74.443	74.710
VDD_SOC_DRAM_GPU	0.859	651.783	559.740	0.958	891.305	854.253
NVCC_DRAM	1.204	273.439	329.106	1.098	260.480	286.039
Total power	—	—	952.436			1215.002
Die Avg Temperature (°C)			43			46

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.4.2 GPU_MM06

Table 15 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 15. GPU_MM06

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	57.333	57.604	1.004	75.834	76.117
VDD_SOC_DRAM_GPU	0.858	784.331	673.193	0.959	1057.341	1014.123
NVCC_DRAM	1.204	303.461	365.441	1.098	291.429	320.032
Total power	—	—	1096.238			1410.272
Die Avg Temperature (°C)			43			50

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.4.3 GPU_Kanzi

Table 16 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 16. GPU_Kanzi

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	76.983	77.382	1.004	90.448	90.809

Table continues on the next page...

Table 16. GPU_Kanzi (continued)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_SOC_DRAM_GPU	0.859	729.047	625.992	0.959	988.370	947.762
NVCC_DRAM	1.204	282.156	339.807	1.098	247.620	271.933
Total power	—	—	1043.182			1310.504
Die Avg Temperature (**°C**)			45			50

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.4.4 GPU_GLmark

Table 17 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 17. GPU_GLmark

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	62.524	62.781	1.004	79.756	80.072
VDD_SOC_DRAM_GPU	0.859	698.292	599.511	0.959	954.133	914.985
NVCC_DRAM	1.204	291.453	350.890	1.098	253.831	278.785
Total power	—	—	1013.182			1273.841
Die Avg Temperature (**°C**)			45			51

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.5 Heavy-load use cases

These use-case scenarios were tested:

- 4-core Dhryst + Taiji
- 4-core Memtest + Taiji
- 4-core Streamcpy + Taiji
- Coremark + Kanzi

The purpose of these use cases is to provide the power consumption for heavy-load use cases to show the power consumption in extreme conditions.

4.5.1 4-core Dhryst + Taiji

This use case runs Dhrystone (4.3.1) and GPU_MM07(4.4.1) in parallel.

- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 18 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 18. 4-core Dhryst + Taiji

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	1014.223	1019.457	1.009	1019.926	1028.962
VDD_SOC_DRAM_GPU	0.859	469.078	402.767	0.960	924.017	886.952
NVCC_DRAM	1.202	143.271	172.211	1.099	262.775	288.805
Total power	—	—	1594.435			2204.718
Die Avg Temperature (**°C**)			54			61

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.5.2 4-core Memtest + Taiji

This use case runs memtester (an effective user-space tester for stress-test the memory subsystem) and GPU_MM07(4.4.1) in parallel.

- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 19 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 19. 4-core Memtest + Taiji

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	528.751	532.109	1.006	553.244	556.790
VDD_SOC_DRAM_GPU	0.859	708.714	608.755	0.959	947.058	908.382
NVCC_DRAM	1.205	360.734	434.810	1.099	308.688	339.132
Total power	—	—	1575.674			1804.303
Die Avg Temperature (**°C**)			56			62

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.5.3 4-core Streamcpy + Taiji

This use case run streamcpy (4.6.3) and GPU_MM07(4.4.1) in parallel.

- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 20 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 20. 4-core Streamcpy + Taiji

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.006	512.234	515.512	1.006	542.940	546.261
VDD_SOC_DRAM_GPU	0.859	710.472	610.247	0.959	942.772	904.223
NVCC_DRAM	1.206	391.422	472.180	1.098	293.401	322.294
Total power	—	—	1597.939			1772.778
Die Avg Temperature (**°C**)			57			59

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.5.4 Coremark + Kanzi

This use case run Coremark (4.3.3) and GPU_Kanzi(4.4.3) in parallel.

- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 21 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 21. Coremark + Kanzi

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.005	853.686	858.370	1.008	855.214	861.772
VDD_SOC_DRAM_GPU	0.859	743.898	638.727	0.960	988.387	948.678
NVCC_DRAM	1.205	271.890	327.573	1.099	241.300	265.106
Total power	—	—	1824.670			2075.556
Die Avg Temperature (**°C**)			55			63

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.6 Memory

These use-case scenarios were tested:

- Memset
- Memcpy
- Stream

Memset and Memcpy are part of a perf-bench (a general framework for benchmark suites).

4.6.1 Memset

Memset is a suite for evaluating the performance of a simple memory set in various ways.

- The size of the memory buffers is set to 1024 MB.
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 22 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 22. Memset

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	201.707	202.488	1.004	194.289	195.011
VDD_SOC_DRAM_GPU	0.859	491.509	422.092	0.956	606.021	579.470
NVCC_DRAM	1.204	294.492	354.470	1.098	257.945	283.256
Total power	—	—	979.050			1057.738
Die Avg Temperature (**°C**)			45			45

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.6.2 Memcpy

Memcpy is a suite for evaluating the performance of a simple memory copy in various ways.

- The size of the memory buffers is set to 1024 MB.
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 23 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 23. Memcpy

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	220.024	220.877	1.004	251.600	252.607
VDD_SOC_DRAM_GPU	0.859	510.289	438.366	0.956	605.100	578.617

Table continues on the next page...

Table 23. Memcpy (continued)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
NVCC_DRAM	1.205	366.266	441.488	1.098	188.028	206.479
Total power	—	—	1100.731			1037.702
Die Avg Temperature (**°C**)			45			47

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.6.3 Stream

The Stream benchmark is a simple synthetic benchmark program that measures the sustainable memory bandwidth (in MB/s) and the corresponding computation rate for simple vector kernels.

- The stream array size is set to 102400000 elements.
- All phases are included (Copy, Scale, Add, and Triad).
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 24 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 24. Stream

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.007	520.879	524.288	1.006	549.927	553.125
VDD_SOC_DRAM_GPU	0.858	475.092	407.856	0.956	607.879	581.393
NVCC_DRAM	1.206	381.029	459.679	1.098	243.519	267.470
Total power	—	—	1391.823			1401.988
Die Avg Temperature (**°C**)			52			52

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.7 Storage – SD2.0 Card

These use-case scenarios were tested:

- DD_RD_SDCARD
- DD_WRT_SDCARD

4.7.1 DD_RD_SDCARD

- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.

(`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)

- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 25 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 25. DD_RD_SDCARD

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	87.117	87.481	1.003	86.552	86.850
VDD_SOC_DRAM_GPU	0.857	400.882	343.534	0.956	521.109	497.919
NVCC_DRAM	1.201	99.677	119.684	1.098	102.210	112.197
Total power	—	—	550.699			696.967
Die Avg Temperature (**°C**)			43			45

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.7.2 DD_WRT_SDCARD

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 26 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 26. DD_WRT_SDCARD

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	147.473	148.092	1.004	159.412	160.044
VDD_SOC_DRAM_GPU	0.857	398.188	341.245	0.956	514.659	491.793
NVCC_DRAM	1.201	103.084	123.776	1.098	71.391	78.370
Total power	—	—	613.113			730.207
Die Avg Temperature (**°C**)			40			45

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.8 Storage – eMMC

These use-case scenarios were tested:

- DD_RD_eMMC
- DD_WRT_eMMC

4.8.1 DD_RD_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 27 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 27. DD_RD_eMMC

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.003	175.012	175.620	1.004	206.847	207.644
VDD_SOC_DRAM_GPU	0.857	435.703	373.485	0.956	566.708	541.664
NVCC_DRAM	1.201	161.770	194.332	1.098	151.128	165.920
Total power	—	—	743.438			915.229
Die Avg Temperature (**°C**)			38			45

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.8.2 DD_WRT_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 28 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 28. DD_WRT_eMMC

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	150.963	151.545	1.004	265.863	266.935

Table continues on the next page...

Table 28. DD_WRT_eMMC (continued)

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_SOC_DRAM_GPU	0.857	404.231	346.321	0.956	539.934	516.057
NVCC_DRAM	1.200	102.394	122.904	1.098	101.038	110.929
Total power	—	—	620.771			893.921
Die Avg Temperature (°C)			41			44

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.9 Storage – USB 2.0

These use-case scenarios were tested:

- DD_RD_USB2.0
- DD_WRT_ USB2.0

4.9.1 DD_RD_USB2.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 29 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 29. DD_RD_ USB2.0

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	83.421	83.752	1.004	85.572	85.912
VDD_SOC_DRAM_GPU	0.858	460.495	395.175	0.956	522.137	499.175
NVCC_DRAM	1.201	125.954	151.302	1.098	75.359	82.761
Total power	—	—	630.229			667.848
Die Avg Temperature (°C)			42			43

1. The ambient temperature is approximately **20 °C.**

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

4.9.2 DD_WRT_ USB2.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (The CPU frequency is set to the maximum value).
- The DDRC frequency for DDR4 is set to 600 MHz, and for LPDDR4 is set to 800MHz

Table 30 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 30. DD_WRT_USB2.0

Supply domain	L4.14.98-MX8MN-DDR4			L5.4.24-MX8MN-LPDDR4		
	Voltage (V)	I (mA)	P (mW)	Voltage (V)	I (mA)	P (mW)
VDD_ARM	1.004	96.701	97.085	1.004	122.913	123.393
VDD_SOC_DRAM_GPU	0.858	460.861	395.503	0.956	523.387	500.271
NVCC_DRAM	1.201	129.063	155.037	1.098	69.382	76.188
Total power	—	—	647.625			699.852
Die Avg Temperature (°C)			42			42

1. The ambient temperature is approximately 20 0C.

`cat /sys/class/thermal/thermal_zone0/temp` was used to log the temperature while the benchmark is running.

5 Reducing Power Consumption

The overall system power consumption depends on both the software optimization and how the system hardware is implemented. The following is a list of suggestions that may help to reduce the system power consumption:

- Apply the clock gating whenever the clocks or modules are not used by configuring the CCGR registers in the Clock Controller Module (CCM).
- Reduce the number of operating PLLs: Applicable mainly in the Audio_Playback or Idle modes.

Core DVFS and system bus scaling: Applying the DVFS for ARM and scaling the frequencies of the NOC, AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDD_ARM and VDD_SOC domains.

Additionally, due to reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memory. This trade-off must be taken into account for each mode to quantify the overall effect on the system power consumption.

- Put the i.MX 8M Nano into the low-power modes (STOP) whenever possible. See Chapter “Clock Controller Module (CCM)” in the *i.MX 8M Nano Applications Processor Reference Manual* for details.
- DDR interface optimization:
  - Employ careful board routing of the DDR memories, maintaining the PCB trace lengths as short as possible.
  - Use as increased an ODT (On-Die Termination) setting as possible. The termination used greatly influences the power consumption of the DDR interface pins.
  - Use a proper output driver impedance for the DDR interface pins that provide good impedance matching. Select the lowest possible drive strength that provides the required performance to reduce the current flowing through the DDR I/O pins.

— The use of the DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps are shown below.

NOTE

All the programming steps below are performed in the Arm trusted firmware from the internal RAM.

5.1 Steps to be performed before entering Suspend (Deep-sleep) mode

1. Read the DBGCAM register in DDRC to make sure that the explicit transaction command queue is empty. Wait until the AXI port is idle.

Do the following:

- a) Put the DDR into self-refresh.
- b) Transition the DDR PHY into LP3/IO retention state by using the DFI frequency operation.
- c) Set the PwrOkIn signal in SRC to 0. This enables the data retention feature on the CKE and MEMRESET.
- d) Gate the DDRC's CORE clock and APB clock.
- e) Enable DDRMIX ISO to power-gate the DDRC and PHY.

Enter Suspend mode.

5.2 Steps to be performed after exiting Suspend mode

1. Restore all the settings for the DDRC and PHY to the required values.

The system proceeds to the Run mode.

6 Use-Case Configuration and Usage Guidelines

NOTE

Before running a use case, *<configuration_script>.sh* must be run to configure the environment. These are: *setup.sh, setup_default.sh, setup_video.sh, DDRC_266MHz_setup.sh(For DDR4 EVK Board) and DDRC_25MHz_setup.sh(For LPDDR4 EVK Board)* (see Section 6.12 for details).

6.1 Suspend mode

In this use case, all clocks and PLLs are turned off, except for the 32 kHz clock which is used to wake up the system:

1. Boot up the Linux image.
2. Run this command to put the system into the DSM mode:

```
echo mem > /sys/power/state
```

3. Measure the power and record the result.

6.2 System idle mode

NOTE

No display was connected to the platform.

6.2.1 IDLE_DEFAULT

6.2.1.1 Clock configuration

The clock configuration in Table 31 is aligned with release L4.14.98 andL5.4.24.

Table 31. IDLE_DEFAULT clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1200
DDRC	600 for DDR4 EVK 800 for LPDDR4 EVK

6.2.1.2 PLL configuration

The PLL configuration in Table 32 is aligned with release L4.14.98 and L5.4.24.

Table 32. IDLE_DEFAULT PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1200
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_500M	off
ENET_AXI_CLK	SYS_PLL1_266M	off
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	off
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_CLK_ROOT	67

6.2.1.3 System setup

Disconnect everything except for the SD card.

Make sure there are no displays connected to the platform.

1. Boot up the Linux OS.
2. Run *setup_default.sh* (Section 6.12 “Important commands”) to put the system to system idle mode.

Measure the power and record the result.

6.2.2 IDLE_DDRC_266MHz for DDR4 EVK Board

6.2.2.1 Clock configuration

The clock configuration in Table 33 is aligned with release L4.14.98.

Table 33. IDLE_DDRC_266MHz clock configuration

Clock name	Frequency (MHz)
NOC	120
AXI	24
AHB	22.2
CPU	1200
DDRC	266

6.2.2.2 PLL configuration

The PLL configuration in Table 34 is aligned with release L4.14.98.

Table 34. IDLE_DDRC_266MHz PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1200
NOC_CLK	SYS_PLL3_OUT	120
MAIN_AXI_CLK	OSC_24M	24
DISP_AXI_CLK	SYS_PLL2_500M	off
ENET_AXI_CLK	SYS_PLL1_266M	off
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	off
AHB_CLK_ROOT	SYS_PLL1_133M	22.2
IPG_CLK	AHB_CLK_ROOT	11.1
DRAM_CLK	PLL_DRAM_MAIN_CLK	266

6.2.2.3 System setup

Disconnect everything except for the SD card.

Make sure there are no displays connected to the platform.

1. Boot up the Linux OS.
2. Run *DDRC_266MHz_setup.sh* (Section 6.12 “Important commands”) to put the system to system idle mode.

Measure the power and record the result.

6.2.3 IDLE_DDRC_25MHz for LPDDR4 EVK Board

6.2.3.1 Clock configuration

The clock configuration in Table 35 is aligned with release L5.4.24.

Table 35. IDLE_DDRC_25MHz clock configuration

Clock name	Frequency (MHz)
NOC	120
AXI	24
AHB	22.2
CPU	1200
DDRC	25

6.2.3.2 PLL configuration

The PLL configuration in Table 36 is aligned with release L5.4.24.

Table 36. IDLE_DDRC_25MHz PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1200
NOC_CLK	SYS_PLL3_OUT	120
MAIN_AXI_CLK	OSC_24M	24
DISP_AXI_CLK	SYS_PLL2_500M	off
ENET_AXI_CLK	SYS_PLL1_266M	off
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	off
AHB_CLK_ROOT	SYS_PLL1_133M	22.2
IPG_CLK	AHB_CLK_ROOT	11.1
DRAM_CLK	PLL_DRAM_MAIN_CLK	25

6.2.3.3 System setup

Disconnect everything except for the SD card.

Make sure there are no displays connected to the platform.

1. Boot up the Linux OS.
2. Run *DDRC_25MHz_setup.sh* (Section 6.12 “Important commands”) to put the system to system idle mode.

Measure the power and record the result.

6.3 Audio_Playback

6.3.1 Clock configuration

The clock configuration in the following table is aligned with release L4.14.98 and L5.4.24.

Table 37. Audio_Playback clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.3.2 PLL configuration

The PLL configuration in the following table is aligned with release L4.14.98 and L5.4.24.

Table 38. Audio_Playback PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	off
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 800 for LDDDR4
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	off
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100

Table continues on the next page...

Table 38. Audio_Playback PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24
SPDIF_CLK	AUDIO1_PLL_OUT	246

6.3.3 Audio_Playback(gplay)

The audio file used was an mp3 file with a 128-kbps bitrate and a 44-kHz sample rate/s, played using the following options:

1. Boot up the Linux OS.
2. Run *setup.sh* (Section 6.13 “ Important commands”) .
3. Run *gplay_audio.sh* and measure:

```
audio_file='Mpeg1L3_44kHz_128kbps_s_Ed_Rush_Sabotage_mplayer.mp3'
gplay-1.0 $audio_file
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.3.4 Audio_Playback(gplay)_DDRC_266MHz on DDR4 EVK Board

The audio file used was an mp3 file with a 128-kbps bitrate and a 44-kHz sample rate/s, played using the following options:

1. Boot up the Linux OS.
2. Run *DDRC_266MHz_setup.sh* (Section 6.13 “ Important commands”) .
3. Run *gplay_audio.sh* and measure:

```
audio_file='Mpeg1L3_44kHz_128kbps_s_Ed_Rush_Sabotage_mplayer.mp3'
```

```
gplay-1.0 $audio_file
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.3.5 Audio_Playback(gplay)_DDRC_25MHz on LPDDR4 EVK Board

The audio file used was an mp3 file with a 128-kbps bitrate and a 44-kHz sample rate/s, played using the following options:

1. Boot up the Linux OS.
2. Run *DDRC_25MHz_setup.sh* (Section 6.13 “ Important commands”) .
3. Run *gplay_audio.sh* and measure:

```
audio_file='Mpeg1L3_44kHz_128kbps_s_Ed_Rush_Sabotage_mplayer.mp3'

gplay-1.0 $audio_file
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.3.6 Audio+Video_Playback(gplay)

For this use case, the MIPI-DSI port was connected to a 1080p TV display.

The video file used for playback is .mkv file format compressed with HEVC standard with full HD resolution at 29.97 fps and the audio encoding is AACL with a 44.1 kHz samples/s and 2-channel configuration.

Video file was locally played using gplay-1.0, with the following options:

1. Boot up the Linux OS.
2. Run *setup_video.sh* to put the system into system idle mode (*Section 6.13 Important commands*).
3. Run *gplay_videoplayback.sh* and measure:

```
path=`pwd`

FILE=HEVC_1920x1080_29.97fps_AACLC_44.1Khz_2ch.mkv

gplay-1.0 $path/$FILE
```

4. Start the die temperature recording (*Section 6.13 Important commands*).
5. Measure the power and record the result.

6.3.7 Audio+Video_Playback_Stream(gplay)

For this use case, the MIPI-DSI port was connected to a 1080p TV display.

The video file used for playback is .mkv file format compressed with HEVC standard with full HD resolution at 29.97 fps and the audio encoding is AACL with a 44.1 kHz samples/s and 2-channel configuration.

Video file was locally played using gplay-1.0, with the following options:

1. Boot up the Linux OS.
2. Run *setup_video_stream.sh* to (*Section 6.13 Important commands*).
3. Run *gplay_video_stream.sh* and measure:

```
video=HEVC_1920x1080_29.97fps_AACLC_44.1Khz_2ch.mkv server=ip or <server_hostname>

FILE=http://$server/$video

gplay-1.0 $FILE
```

4. Start the die temperature recording (*Section 6.13 Important commands*).

5. Measure the power and record the result.

6.4 Core Benchmark

NOTE

No display was connected to the platform.

6.4.1 Clock configuration

The clock configuration in Table 39 is aligned with release L4.14.98 and L5.4.24.

Table 39. Core Benchmark Tests Clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.4.2 PLL configuration

The PLL configuration in Table 40 is aligned with release L4.14.98 and L5.4.24.

Table 40. Core Benchmark Tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	off
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	off

Table continues on the next page...

Table 40. Core Benchmark Tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24

6.4.3 Core Dhrystone

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (Section 6.13 “ Important commands”) .
3. Run *dhrystone_loop.sh* and measure:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 ./dhrystone/gcc_dry2 &
sudo taskset -c 1 ./dhrystone/gcc_dry2 &
sudo taskset -c 2 ./dhrystone/gcc_dry2 &
sudo taskset -c 3 ./dhrystone/gcc_dry2
done
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.4.4 Core Whetstone

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (Section 6.13 “ Important commands”) .
3. Run *whetstone_loop.sh* and measure:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 ./whetsSP &
sudo taskset -c 1 ./whetsSP &
sudo taskset -c 2 ./whetsSP &
sudo taskset -c 3 ./whetsSP
done
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.4.5 Coremark

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (Section 6.13 “ Important commands”) .
3. Run *Coremark_loop.sh* and measure:

```
while true; do
./Coremark.exe > /dev/null 2>&1
done
```

4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Measure the power and record the result.

6.5 GPU

Two benchmarks were used for GPU power measurements. A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (See Section 6.13 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective GPU benchmark in a loop and start the power measurements and temperature logging at the desired time interval.

6.5.1 Clock Configuration

The clock configuration in Table 41 is aligned with release L4.14.98 and L5.4.24.

Table 41. GPU Test Clock Configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133

Table continues on the next page...

Table 41. GPU Test Clock Configuration (continued)

Clock name	Frequency (MHz)
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.5.2 PLL configuration

The PLL configuration in Table 42 is aligned with release L4.14.98 and L5.4.24.

Table 42. GPU Test PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	500
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	149
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off

Table continues on the next page...

Table 42. GPU Test PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24

6.5.3 GPU_MM07

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Run *gpu_mm07.sh* :

```
cd mm07/
while true; do
./fm_oes2_mobile_player
done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record the result.

6.5.4 GPU_MM06

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Run *gpu_mm06.sh* :

```
cd mm06/
while true; do
./fm_oes_player
done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record the result.

6.5.5 GPU_Kanzi

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Run *gpu_kanzi.sh* :

```
kanzi_dir=`pwd`"/Kanzi/KPA_1_0_1_137/linux-aarch64"
```

```
cd $kanzi_dir

./kanzi.sh
```

Where *kanzi.sh:*

```
export LD_LIBRARY_PATH="$PWD"

while true;do

./kpa.exe

done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record the result.

6.5.6 GPU_GLmark

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Run *gpu_glmark.sh* :

```
while true;do

glmark2-es2-wayland --fullscreen

done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record the result

6.6 Heavy-load use cases

Four use cases were used for power measurements. A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (see Section 6.13 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

6.6.1 Clock Configuration

The clock configuration in Table 43 is aligned with release L4.14.98 and L5.4.24.

Table 43. Heavy-load Test Clock Configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.6.2 PLL configuration

The PLL configuration in Table 44 is aligned with release L4.14.98 and L5.4.24.

Table 44. Heavy-load Test PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	500
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	149
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24

Table continues on the next page...

Table 44. Heavy-load Test PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24

6.6.3 4-core Dhryst + Taiji

A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (see Section 6.13 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Start 4 Dhrystone, each bind on separate CPU:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 ./Dhrystone/gcc_dry2 &
sudo taskset -c 1 ./Dhrystone/gcc_dry2 &
sudo taskset -c 2 ./Dhrystone/gcc_dry2 &
sudo taskset -c 3 ./Dhrystone/gcc_dry2
done
```

3. Start Taiji use case in a loop (Section 6.7.1 “MM07”).
4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Start power measurement and record data.

6.6.4 4-core Memtest + Taiji

A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (see Section 6.12 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Start 4 memtesters, each bind on separate CPU:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 memtester 200M &
sudo taskset -c 1 memtester 200M &
sudo taskset -c 2 memtester 200M &
```

```
sudo taskset -c 3 memtester 200M

done
```

3. Start Taiji use case in a loop (Section 6.7.1 “MM07”).
4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Start power measurement and record data.

6.6.5 4-core Streamcpy + Taiji

A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (see Section 6.12 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Start 4 streams, each bind on separate CPU:

```
while [ "1" == "1" ]

do

sudo taskset -c 0 stream -M 200M -N 1000 &

sudo taskset -c 0 stream -M 200M -N 1000 &

sudo taskset -c 0 stream -M 200M -N 1000 &

sudo taskset -c 0 stream -M 200M -N 1000

done
```

3. Start Taiji use case in a loop (Section 6.7.1 “MM07”).
4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Start power measurement and record data.

6.6.6 Coremark + Kanzi

A 1080p TV display was connected to the MIPI-DSI port. Before running any benchmark, the governor must be set to **performance** (see Section 6.12 for details):

```
cpufreq-set -g performance
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

1. Run *setup_video.sh* (Section 6.13 “ Important commands”) .
2. Start Coremark use case in a loop. (Section 6.6 “Coremark”)
3. Start GPU_Kanzi use case (Section 6.7.3 “GPU_Kanzi”).
4. Start the die temperature recording (Section 6.13 “ Important commands”) .
5. Start power measurement and record data.

6.7 Memory

NOTE

No display was connected to the platform.

Three use cases were used for power measurements. Before running any benchmark, the governor must be set to **performance** and the display must be turned off (see Section 6.12 for details):

```
cpufreq-set -g performance
```

```
echo 1 > /sys/class/graphics/fb0/blank
```

After setting the governor, run the respective use case in a loop and start power measurements and temperature logging at the desired time interval (recommended is 1 minute) according to Section 6.12.

6.7.1 Clock configuration

The clock configuration in Table 45 is aligned with release L4.14.98 and L5.4.24.

Table 45. Memory Tests Clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.7.2 PLL configuration

The PLL configuration in Table 46 is aligned with release L4.14.98 and L5.4.24.

Table 46. Memory Tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	off
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK

Table continues on the next page...

Table 46. Memory Tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	off
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24

6.7.3 Memset

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Run *memset_loop.sh*:

```
while true; do
perf bench -f simple mem memset -l110000 -s 1024MB
done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.7.4 Memcpy

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Run *memcpy_loop.sh*:

```
while true; do
perf bench -f simple mem memcpy -l10000 -s 1024MB
done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.7.5 Stream

Make sure stream libraries are added to *LD_LIBRARY_PATH*

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Run *streamcpy_loop.sh*:

```
export LD_LIBRARY_PATH=`pwd`:$LD_LIBRARY_PATH
while true; do
./stream
done
```

3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.8 Storage – SD2.0 Card

An SD card was used to run the benchmarks.

6.8.1 Clock configuration

The clock configuration in Table 47 is aligned with release L4.14.98 and L5.4.24.

Table 47. SD 2.0 Card Tests Clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.8.2 PLL configuration

The PLL configuration in Table 48 is aligned with release L4.14.98 and L5.4.24.

Table 48. SD 2.0 Card Tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	off
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	off
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98 SYS_PLL2_500M for L5.4.24	off
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24

Table continues on the next page...

Table 48. SD 2.0 Card Tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24

6.8.3 DD_RD_SDCARD

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_read_SD10.sh* on the SD card partition and run it (see below).
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

```
#!/bin/bash

# Since we're dealing with dd, abort if any errors occur

set -e

TEST_FILE=${1:-dd_ibs_testfile}

#if [ -e "$TEST_FILE" ]; then TEST_FILE_EXISTS=$?; fi

#TEST_FILE_SIZE=3221225472

#134217728

# Exit if file exists

#if [ -e $TEST_FILE ]; then

# echo "Test file $TEST_FILE exists, aborting."

# exit 1

#fi

#TEST_FILE_EXISTS=1

if [ $EUID -ne 0 ]; then

echo "NOTE: Kernel cache will not be cleared between tests without sudo. This will likely cause inaccurate
results." 1>&2

fi

# Create test file

#echo 'Generating test file...'

#BLOCK_SIZE=65536

#COUNT=$(($TEST_FILE_SIZE / $BLOCK_SIZE))

#dd if=/dev/urandom of=$TEST_FILE bs=$BLOCK_SIZE count=$COUNT conv=fsync > /dev/null 2>&1

# Header

PRINTF_FORMAT="%8s : %s\n"

printf "$PRINTF_FORMAT" 'block size' 'transfer rate'

# Block sizes of 512b 1K 2K 4K 8K 16K 32K 64K 128K 256K 512K 1M 2M 4M 8M 16M 32M 64M
```

```
for BLOCK_SIZE in 512 1024 2048 4096 8192 16384 32768 65536 131072 262144 524288 1048576 2097152 4194304
8388608 16777216 33554432 67108864

do

# Clear kernel cache to ensure more accurate test

[ $EUID -eq 0 ] && [ -e /proc/sys/vm/drop_caches ] && echo 3 > /proc/sys/vm/drop_caches

# Read test file out to /dev/null with specified block size

DD_RESULT=$(dd if=$TEST_FILE of=/dev/null bs=$BLOCK_SIZE 2>&1 1>/dev/null)

# Extract transfer rate

TRANSFER_RATE=$(echo $DD_RESULT | \grep --only-matching -E '[0-9.]+ ([MGk]?B|bytes)/s(ec)?')

printf "$PRINTF_FORMAT" "$BLOCK_SIZE" "$TRANSFER_RATE"

done
```

6.8.4 DD_WRT_SDCARD

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_write_SD10.sh* on the SD card partition and run it (see below).
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

```
#!/bin/bash

# Since we're dealing with dd, abort if any errors occur

set -e

TEST_FILE=${1:-dd_obs_testfile}

TEST_FILE_EXISTS=0

if [ -e "$TEST_FILE" ]; then TEST_FILE_EXISTS=1; fi

TEST_FILE_SIZE=3221225472

#134217728

if [ $EUID -ne 0 ]; then

echo "NOTE: Kernel cache will not be cleared between tests without sudo. This will likely cause inaccurate
results." 1>&2

fi

# Header

PRINTF_FORMAT="%8s : %s\n"

printf "$PRINTF_FORMAT" 'block size' 'transfer rate'

# Block sizes of 512b 1K 2K 4K 8K 16K 32K 64K 128K 256K 512K 1M 2M 4M 8M 16M 32M 64M

for BLOCK_SIZE in 512 1024 2048 4096 8192 16384 32768 65536 131072 262144 524288 1048576 2097152 4194304
8388608 16777216 33554432 67108864

do

# Calculate number of segments required to copy

COUNT=$(($TEST_FILE_SIZE / $BLOCK_SIZE))

if [ $COUNT -le 0 ]; then
```

```
echo "Block size of $BLOCK_SIZE estimated to require $COUNT blocks, aborting further tests."
break
fi
# Clear kernel cache to ensure more accurate test
[ $EUID -eq 0 ] && [ -e /proc/sys/vm/drop_caches ] && echo 3 > /proc/sys/vm/drop_caches
# Create a test file with the specified block size
DD_RESULT=$(dd if=/dev/zero of=$TEST_FILE bs=$BLOCK_SIZE count=$COUNT conv=fsync 2>&1 1>/dev/null)
# Extract the transfer rate from dd's STDERR output
TRANSFER_RATE=$(echo $DD_RESULT | \grep --only-matching -E '[0-9.]+ ([MGk]?B|bytes)/s(ec)?')
## Clean up the test file if we created one
#if [ $TEST_FILE_EXISTS -ne 0 ]; then rm $TEST_FILE; fi
# Output the result
printf "$PRINTF_FORMAT" "$BLOCK_SIZE" "$TRANSFER_RATE"
done
```

6.9 Storage – eMMC

A partition was created on eMMC and benchmarks were run on it. eMMC test clock and PLL configuration can refer to Table 47 and Table 48 in 6.8 Storage- SD 2.0 section.

6.9.1 DD_RD_eMMC

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_read_SD10.sh* on eMMC partition and run.
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.9.2 DD_WRT_eMMC

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_write_SD10.sh* on eMMC partition and run.
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.10 Storage – USB2.0

A USB 2.0 was used to run the benchmarks.

6.10.1 Clock configuration

The clock configuration in Table 49 is aligned with release L4.14.98 and L5.4.24.

Table 49. USB 2.0 Partitions Tests Clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1500
DDRC	600 for DDR4 800 for LPDDR4

6.10.2 PLL configuration

The PLL configuration in Table 50 is aligned with release L4.14.98 and L5.4.24.

Table 50. USB 2.0 Partitions Tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS_PLL3_OUT	600
MAIN_AXI_CLK	SYS_PLL2_333M	333
DISP_AXI_CLK	SYS_PLL2_1000M	off
ENET_AXI_CLK	SYS_PLL1_266M	266
NAND_USDHC_BUS_CLK	SYS_PLL1_266M	266
AHB_CLK_ROOT	SYS_PLL1_133M	133
IPG_CLK	AHB_ROOT_CLK	67
DRAM_CLK	PLL_DRAM_MAIN_CLK	600 for DDR4 EVK 800 for LPDDR4 EVK
DISP_PIXEL_CLK	VIDEO1_PLL_CLK	off
SAIx_CLK	24M OSC/AUDIO1_PLL_OUT	off
ENETx_REF_CLK	SYS_PLL2_125M	125
ENETx_TIME_CLK	SYS_PLL2_100M	100
ENET_PHY_REF_CLK	24M OSC	24
NAND_CLK	SYS_PLL1_400M for L4.14.98	off

Table continues on the next page...

Table 50. USB 2.0 Partitions Tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
	SYS_PLL2_500M for L5.4.24	
QSPI_CLK	SYS_PLL1_800M for L4.14.98 SYS_PLL1_400M for L5.4.24	off
USHDCx_CLK	SYS_PLL1_400M	400
I2Cx_CLK	24M OSC	24
UARTx_CLK	24M OSC	24
ECSPIx_CLK	24M OSC for L4.14.98 SYS_PLL2_200M for L5.4.24	off
PWMx_CLK	24M OSC	24
GPTx_CLK	24M OSC	24
TRACE_CLK	24M OSC	off
WDOG_CLK	24M OSC	24
USB_CORE_REF	24M OSC	off
USB_BUS_CLK	SYS_PLL2_500M	500
USB_PHY_REF	SYS_PLL1_100M	100

6.10.3 DD_RD_USB2.0

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_read_SD10.sh* on USB 2.0 partition and run.
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.10.4 DD_WRT_USB2.0

1. Run *setup.sh* (Section 6.13 “ Important commands”) .
2. Copy *dd_write_SD10.sh* on USB 2.0 partition and run.
3. Start the die temperature recording (Section 6.13 “ Important commands”) .
4. Start power measurement and record data.

6.11 Important commands

1. Before running a use case, *<configuration_script>.sh* must be run to configure the environment. These are: *setup.sh, setup_default.sh, setup_video.sh , setup_video_stream.sh, DDRC_266MHz_setup.sh, DDRC_25MHz_setup.sh* (see below) .

- *setup.sh:* The CPU frequency is set to the maximum value 1500 MHz to achieve the best performance. Disable the Ethernet, stop the Weston service, and blank the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.

```
#!/bin/bash

systemctl stop weston.service

cpufreq-set -g performance

echo 1 > /sys/class/graphics/fb0/blank

partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`

for partition in $partitions; do

echo 512 > /sys/block/$partition/queue/read_ahead_kb

done

eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`

for eth in $eth_int;do

ifconfig $eth down

done
```

- *setup_default.sh*: The CPU frequency is the default value 1200 MHz. Disable the Ethernet, stop the Weston service, and blank the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.

```
#!/bin/bash

systemctl stop weston.service

echo 1 > /sys/class/graphics/fb0/blank

partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`

for partition in $partitions; do

echo 512 > /sys/block/$partition/queue/read_ahead_kb

done

eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`

for eth in $eth_int;do

ifconfig $eth down

done
```

- *setup_video.sh*: The CPU frequency is set to the maximum value 1500 MHz to achieve the best performance. Disable the Ethernet, stop the Weston service, and awake the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.

```
#!/bin/bash

export WL_EGL_SWAP_INTERVAL=0

cpufreq-set -g performance

partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`

for partition in $partitions; do

echo 512 > /sys/block/$partition/queue/read_ahead_kb

done

eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`
```

```
for eth in $eth_int;do

ifconfig $eth down

done

echo 1 > /sys/class/graphics/fb0/blank

echo 0 > /sys/class/graphics/fb0/blank
```

- *setup_video_stream.sh*: The CPU frequency is set to the maximum value 1500 MHz to achieve the best performance. Open the Ethernet to play the video online. Stop the Weston service and awake the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB.

```
#!/bin/bash

export WL_EGL_SWAP_INTERVAL=0

cpufreq-set -g performance

partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`

for partition in $partitions; do

echo 512 > /sys/block/$partition/queue/read_ahead_kb

done

eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`

for eth in $eth_int;do

ifconfig $eth up

done

echo 1 > /sys/class/graphics/fb0/blank

echo 0 > /sys/class/graphics/fb0/blank
```

- *DDRC_266MHz_setup.sh*: It is used on DDR4 EVK Board. After running below shell scripts, you will see logs that the DDRC frequency switches between high bus mode 600 MHz and low bus mode 266 MHz, due to DDR DVFS. CPU frequency is set to the minimum value 1200 MHz. Both of DDR DVFS and CPU powersave are aimed at saving power. Disable the Ethernet, stop the Weston service, and blank the display.)

```
#!/bin/bash

systemctl stop weston.service

echo 1 > /sys/class/graphics/fb0/blank

cpufreq-set -g powersave

rmmod brcmfmac

#echo 8 > /proc/sys/kernel/printk;

eth_int=`ifconfig -a|grep 'eth\|can\|sit'|awk {'print $1'}`

for eth in $eth_int;do

ifconfig $eth down

done

sleep 5
```

- *DDRC_25MHz_setup.sh*: It is used on LPDDR4 EVK Board. After running below shell scripts, you will see logs that the DDRC frequency switches between high bus mode 800 MHz and low bus mode 25 MHz, due to DDR DVFS. CPU frequency is set to the minimum value 1200 MHz. Both of DDR DVFS and CPU powersave are aimed at saving power. Disable the Ethernet, stop the Weston service, and blank the display.)

```
#!/bin/bash

systemctl stop weston.service

echo 1 > /sys/class/graphics/fb0/blank

cpufreq-set -g powersave

rmmod brcmfmac

#echo 8 > /proc/sys/kernel/printk;

eth_int=`ifconfig -a|grep 'eth\|can\|sit'|awk {'print $1'}`

for eth in $eth_int;do

ifconfig $eth down

done

sleep 5
```

2. In the U-boot console:
   - `printenv`: displays the environment variables.
   - `setenv`: updates the environment variables.
   - `setenv <name> <value> ...`
   - Sets the environment variable “name” to “value ...”.
   - `setenv <name>`
   - Deletes the environment variable “name”.
   - `saveenv`: saves the updates to the environment variables.
   - `bootargs`: passes to the kernel, which are called kernel command lines.
3. In the Linux OS console:
   - `cat /proc/cmdline`: displays the command line.
   - `cat /sys/devices/virtual/thermal/thermal_zone0/temp`: prints the temperature to the screen (the chip should be calibrated).

   Note: The die temperature value was logged (written) externally, not on the SD card, for not impacting power consumption.
   - `cat /sys/kernel/debug/clk/clk_summary`: prints all clocks to the screen.

7 Revision History

Table 51 summarizes the changes done to this document since the initial release.

Table 51. Revision history

Revision number	Date	Substantive changes
0	10/2019	Initial release
1	07/2020	Update power data from latest SW release: DDR4 EVK – L4.14.98_2.3.3 LPDDR4 EVK – L5.4.24_2.1.0

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