AN10364

Opto-electrical isolation of the I²C-bus (operating the bus between points with different local ground potential)

Rev. 1 — 12 November 2010 Application note

Document information

Info	Content
Keywords	P82B96, PCA9600, PCA9601, RS-485, I2C-bus, Fast-mode Plus, CAN bus, opto-isolation, safety isolation, PoE
Abstract	This report discusses factors that need consideration when an I²C-bus is used to communicate between two points that do not share a common logic ground potential. I²C logic signals are referenced to a ground level and it is expected that connected devices share that reference. In practice, when an I²C-bus is extended to link devices that are separated by distances exceeding about 1 meter there can be many factors that cause differences in the local ground potential of those devices and that in turn affects the noise margins of the system and can lead to device ratings being exceeded. In other cases where an I²C-bus could provide an attractive data link there is no possibility for a shared ground reference. Examples include the need to provide safety isolation between the I²C control signals and AC mains power, telephone lines, or patient monitoring medical equipment. In other cases, such as Power over Ethernet, standards require isolation of the grounds. Solutions are provided to deal with ground differences ranging from less than 1 V up to kilovolt levels by using Opto or transformer isolators in the signal path. Key to all solutions is the availability of I²C buffers with the capability to split the bidirectional I²C signals into pairs of conventional uni-directional logic streams that can be then be handled using conventional methods. Solutions for links from 3 kHz to 1 MHz speeds are described.

Revision history

Rev	Date	Description
v.1	20101112	application note; initial release

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1. Introduction

The I²C-bus provides an attractive maintenance and control communication interface between parts of a system since it uses only two signal wires yet has powerful addressing and a reasonably fast, up to 1 MHz, bidirectional data handling capability.

I²C-bus logic signals are referenced to a common (ground) potential. Any potential difference between the grounds of different devices on an I²C-bus introduces a change in the logic signal level between the sending and receiving devices that is equivalent to noise-induced signal level disturbances on the bus wiring. It increases the possibility of communication errors or exceeding the voltage ratings of the connected devices. Most I²C-bus ICs have I/Os ratings that prohibit applying negative voltages greater than 0.3 V to 0.5 V. When one IC has a ground potential 1 V lower than another, then when that IC sends a LOW of, say, +0.4 V with respect to its ground the receiving input will be driven to −0.6 V relative to its ground and exceed its rating. Even when I²C components share a nominally common ground the possibility that large currents, sharing that ground, can cause significant differences in local potential should be considered.

Many systems that can benefit from the advantages of I²C-bus control are not allowed to share any common reference signal (ground) potential. To prevent any chance of electrocution, AC mains control and medical patient monitoring equipment require a safety isolation barrier, to kilovolt levels, between the system components. Regulations require isolation from telephone lines and Standards require isolation from Ethernet wiring, especially when power is also supplied by the Ethernet wiring (PoE). Techniques enabling reliable I²C communication while addressing these different requirements all require first splitting the normally bidirectional SDA/SCL signals into two uni-directional components and then applying conventional techniques to provide the necessary tolerance to difference in local ground potentials, or to provide total galvanic isolation.

The conventional techniques include:

- Increasing the logic signal amplitudes and limiting negative voltages using clamp diodes.
- Conversion to differential mode signals using CAN or RS-485 drivers or dedicated I²C parts
- Providing true galvanic isolation by including opto or magnetic/transformer signal couplers

Buffers that split the I²C-bus signal into uni-directional components and allow them to be simply re-combined by re-connecting them include P82B96, PCA9600 and PCA9601. They can all provide the drive signals to directly interface with the isolating ICs/devices while offering a range of I²C-bus interfacing speeds and drive levels including Fast-mode Plus (Fm+).

Figure 1 shows the separation of one I²C-bus signal (SDA or SCL) into two separate Send and Receive components and clamping negative voltages with Schottky diodes as in the ‘4-signal’ arrangement discussed in *AN10658* (Ref. 1). Operating as shown with a 5 V bus, it can operate between points having a ground potential difference of more than 2 V.

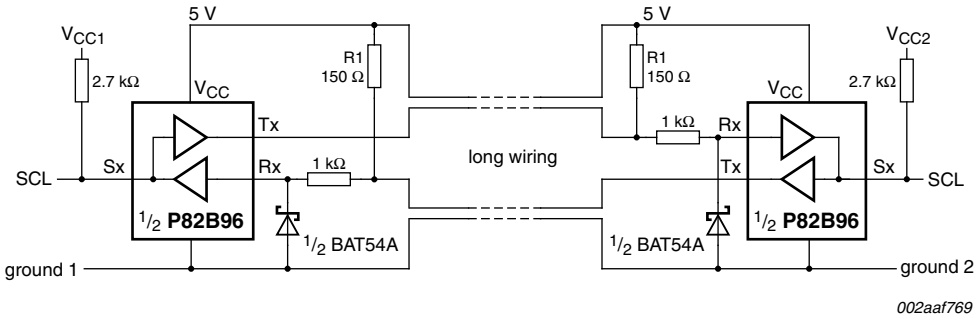


Fig 1. Tolerating moderate ground potential differences using separated uni-directional signals

2. Using a differential signal technique to carry the SDA and SCL signals

Figure 2 and Figure 3 show how I²C-bus signals can be carried as differential signals over either CAN bus hardware, that supports multi-drop bidirectional signals carried on a single twisted pair, or RS-485 hardware that uses separate transmit and receive paths and therefore requires using four twisted pairs to carry the two I²C signals. Both these arrangements provide the same common-mode immunity as offered by those systems, normally around ±7 V.

For Figure 2 duplicate this arrangement to distribute the SCL signal. Because CAN supports the bidirectional SCL/SDA signals only two twisted pairs are required.

For Figure 3 these differential drivers are uni-directional so four twisted pairs are required (e.g., Cat5 cable).

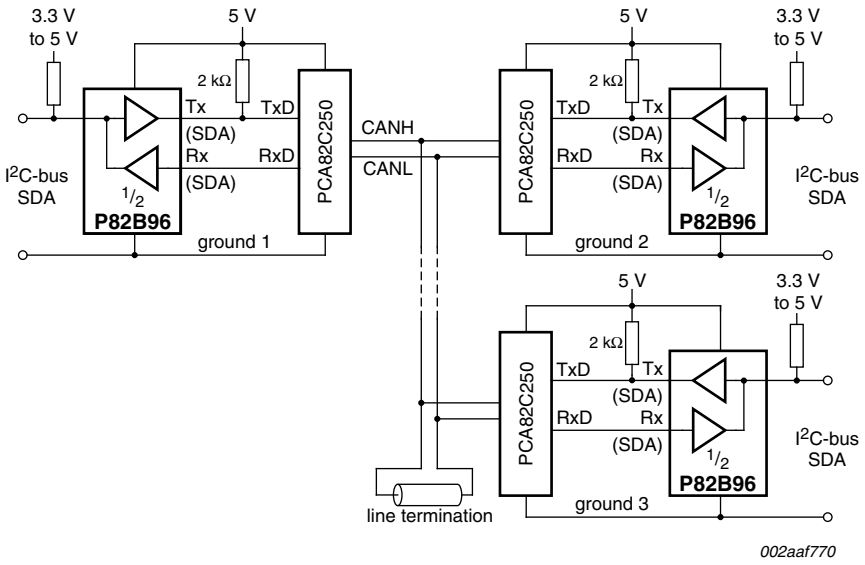


Fig 2. Transmitting one I²C signal as a differential signal using CAN bus hardware

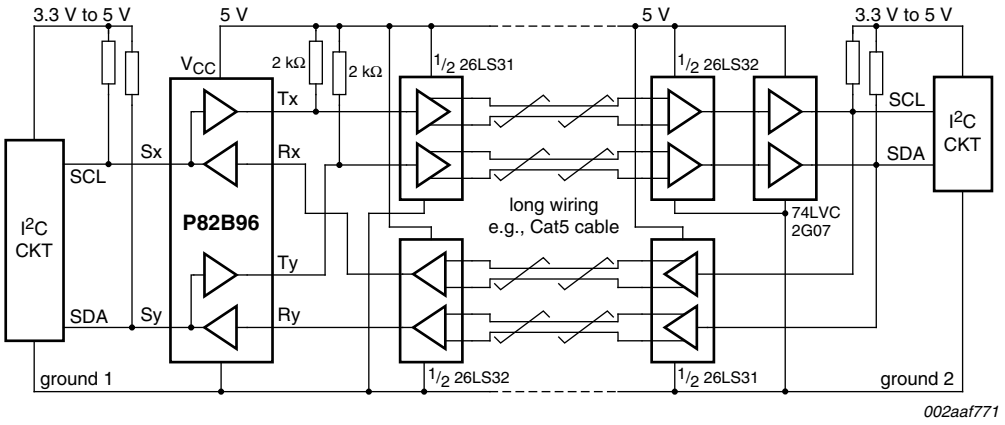


Fig 3. Transmitting the I²C signals as differential signals using RS-485 hardware

3. Opto-coupling supports very large ground differences

Figure 4 shows the simplest arrangement from application note *AN460* (Ref. 2) using P82B96 and using the lowest cost 4N36 opto-couplers to opto-isolate the I²C-bus signal. These couplers allow saturation of the photo-transistor in the opto-coupler, resulting in very long turn-off delays caused by charge storage effects in their output transistor. For the component values given in *AN460* the total switching delays will be around 50 μs and that will limit the bus speed of this simple circuit to around 5 kHz clock.

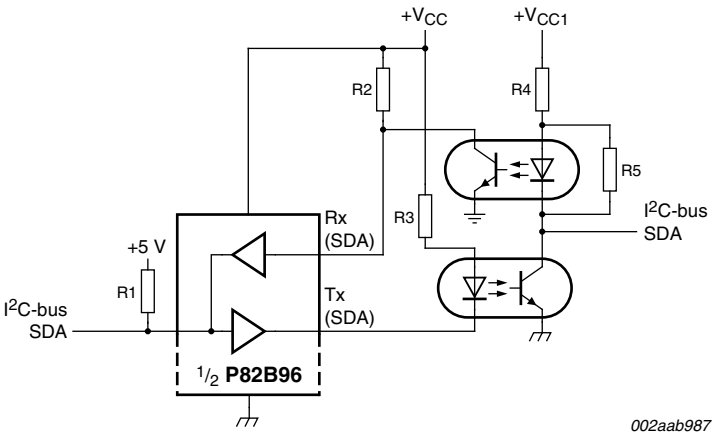


Fig 4. Simple 5 kHz opto-electrical isolation circuit

4. Achieving higher opto-coupled bus speeds: 100 kHz

The clock speed allowed for any I²C class is calculated by adding the delays introduced by the buffers and the opto-couplers to the minimum SCL 'LOW' period. The typical system performance will be found to be much faster when using components specified for a faster class. For example using Fast-mode (Fm) parts for their smaller maximum response delays in a Standard-mode system. Faster speeds require faster opto-couplers. Parts such as 6N137 use Schottky-clamped output transistors to reduce their switching delays to less than 100 ns (each coupler) when operating in the 5 V bus arrangement of Figure 5. They will ensure operation of Standard-mode systems to 100 kHz.

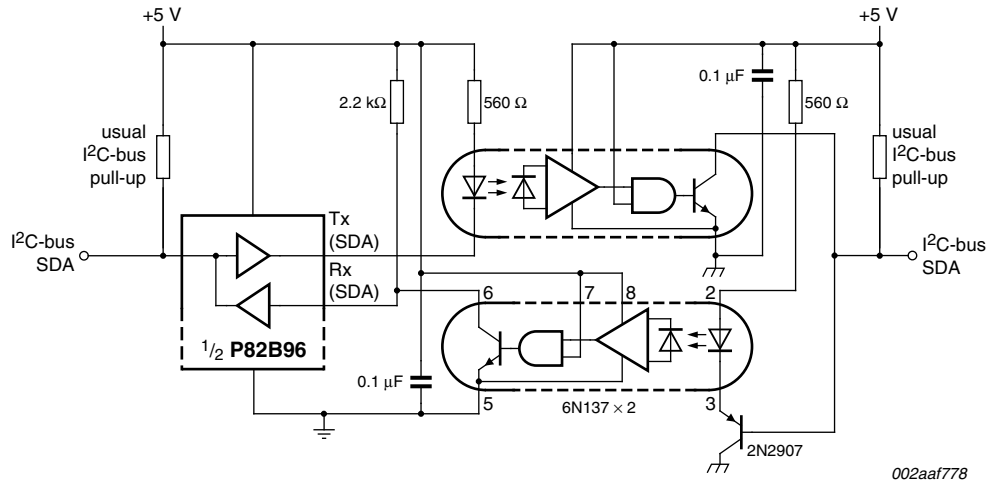


Fig 5. Use higher speed opto-couplers for full 100 kHz operation

5. Opto-couplers for 400 kHz

Because the original I²C specifications did not envisage the development of bus buffering components or the possibilities for signal propagation delays in the system, it is strictly not allowed to introduce any delays other than those anticipated in the bus rise and fall times unless the bus is operated at a speed lower than the maximum allowed for each class. When buffers and opto-couplers introduce delays into the clock and data lines the SCL LOW period should be increased by an amount equal to the sum of those delays. Because the buffers support 'clock stretching' some of that increase will happen automatically, without action by the designer. That is why a system programmed for a nominal 400 kHz will be observed to be running at a slightly slower frequency after buffers and opto-couplers are introduced.

In practice, typical I²C parts do not use up all of the allowed response time that can be calculated from the bus specifications. For example, the typical response time for ICs specified for 400 kHz application are mostly under 700 ns while the bus specifications allow for 1.2 µs delays. This means that in practice delays up to 500 ns can be tolerated. P82B96 introduces delays around 400 ns and fast couplers will have delays less than 100 ns, so in practical systems, when the designer checks the actual bus timings, 400 kHz opto-coupling can be achieved. A fast yet simple circuit, designed for interfacing

3.3 V bus components, is shown in Figure 6. The P82B96 data sheet also gives examples of modifying the duty cycle of the clock when attempting to reach the highest speeds and those techniques are also applicable to delays introduced by opto isolation.

In Figure 6 the reason to use the weakest pull-up on the P82B96 Sx pin is to provide the lowest output drive voltage (V_{OL}) at Sx and therefore the highest noise margin because the indicated bus voltage is 3.3 V. Substituting PCA9600 for the P82B96 and using a 0.3 mA pull-up will provide a guaranteed V_{OL} at 0.65 V and higher speed.

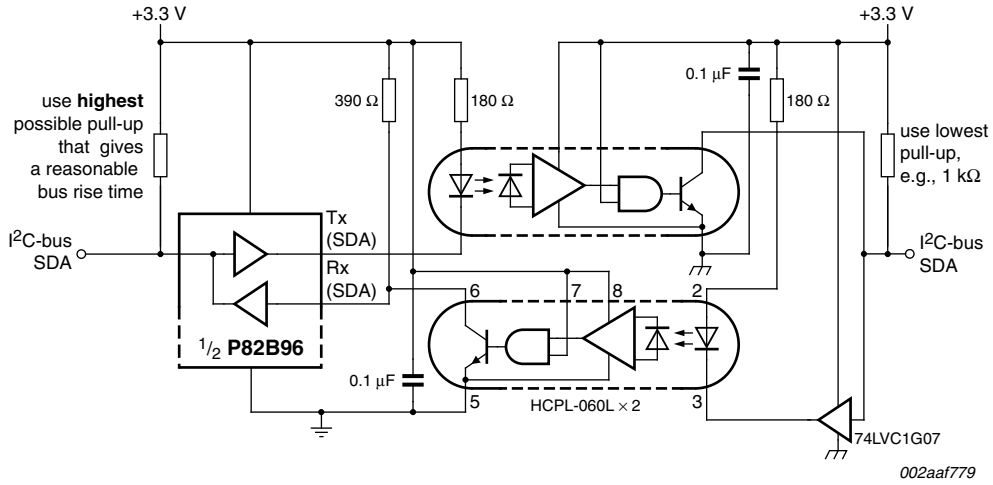


Fig 6. Simple circuit for applications up to 400 kHz (duplicate for SCL line)

6. Operating up to Fast-mode Plus speeds — 1 MHz

When the highest possible speed is required then all delays must be minimized and more care will be required when setting the master clock timing. There is a selection of opto-couplers with typical propagation delays in the range 40 ns to 50 ns, and some are as low as 16 ns. When driven by PCA9600, with its typical propagation delays 40 ns to 80 ns, the total propagation delay through each coupler path can be kept below 100 ns—considerably faster than competing '1 MHz' isolators using magnetic/transformer coupling.

Figure 7, Figure 9 and Figure 10 show applications all capable of a real 1 MHz clock frequency. 'Real' means the actual observed clock frequency, not the nominal frequency programmed into the master. Because the buffer/opto delays will cause the programmed clock LOW period to be stretched, even the fastest system in Figure 10 will stretch the clock LOW by about 130 ns and would slow a master, programmed for a nominal 1 MHz clock, to around a 'real' or observed 770 kHz. Achieving a 'real' 1 MHz is possible but the master must be programmed with new SCL timings that make allowance for the stretching of the clock LOW period. After allowing for the 'stretch' the actual LOW period must be set to 500 ns (minimum) to comply with the Fm+ specification.

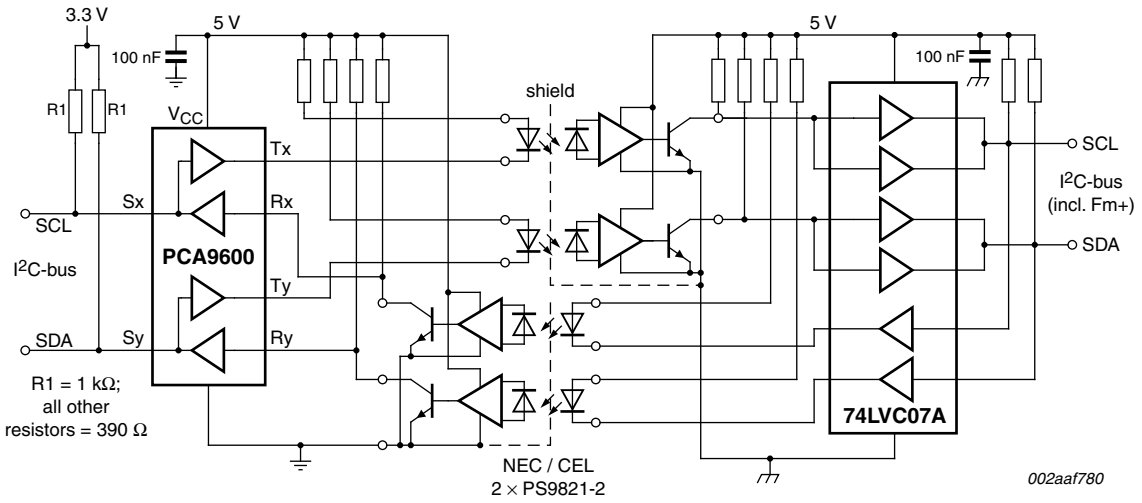
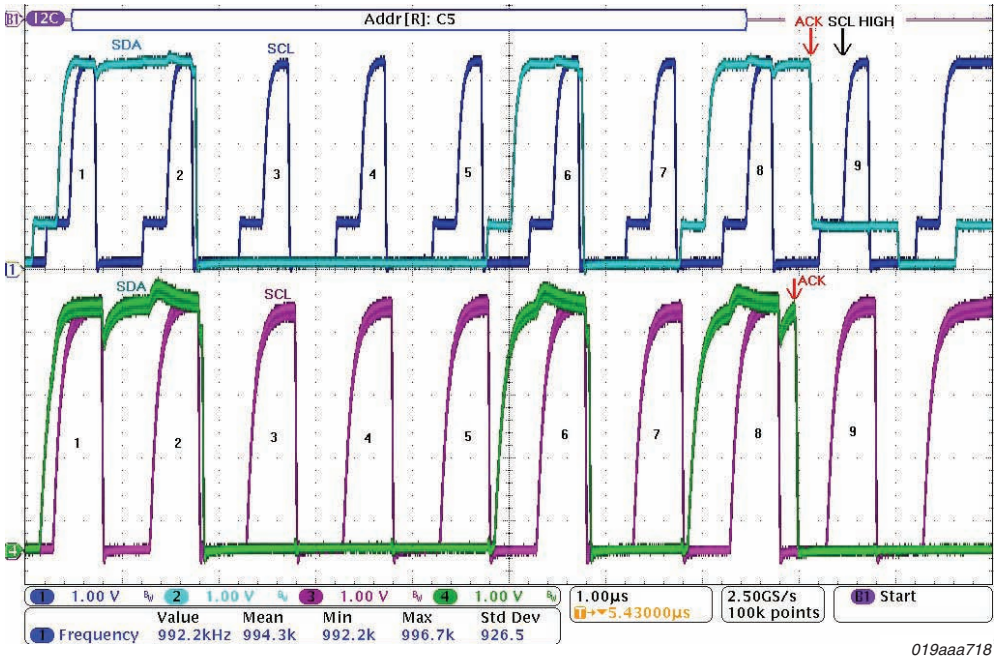


Fig 7. Circuit capable of Fm+ operation to 1 MHz (typical) using couplers with 50 ns (typical) delays

The example in Figure 7 uses couplers with typical delays of 50 ns and 'conventional' switching of the LED current using Tx, or the LVC gate, as a series switch to the ground. When turning off, the stray capacitance of the driver and LED input must be charged nearly to the supply before the LED current drops near zero. This increases the rise time delay in the coupler and accounts for some additional slowing of the clock. Still, by programming the nominal master SCL LOW to about 250 ns, to allow for 250 ns clock 'stretching' by PCA9600 with these 50 ns couplers, Figure 8 shows a correctly acknowledged address transmission at a 'true' 1 MHz.

In Figure 8 the top two traces show SCL/SDA at the terminals of a master connected on the left side while the lower traces show SCL/SDA at the terminals of an Fm+ slave connected on the right. The dark blue trace shows SCL at the master. When the master releases the Sx of PCA9600 the bus does not immediately rise to the V_{DD} at 3.3 V. It rises only to the LOW level output by Sx, about 0.65 V, until the Rx pin, shown by the lower magenta trace becomes HIGH and that HIGH at Rx propagates back through the PCA9600 to Sx and allows it to rise to 3.3 V. The time at which SCL actually achieves the HIGH level, starting the HIGH period of the ninth clock pulse, is indicated by the black arrow. The 'step' at 0.65 V just prior to that time represents a holding of the master clock LOW until the master's input HIGH has time to propagate to the slave and back to the master. In these traces the slave acknowledge is indicated by the red arrow on the green slave SDA trace. Above that, and slightly delayed, is the Acknowledge LOW as received by the master (red arrow on cyan trace). Note that LOW is valid even before the master SCL starts to rise and, after the step of clock stretch, at least 300 ns before the master SCL actually goes HIGH (black arrow).

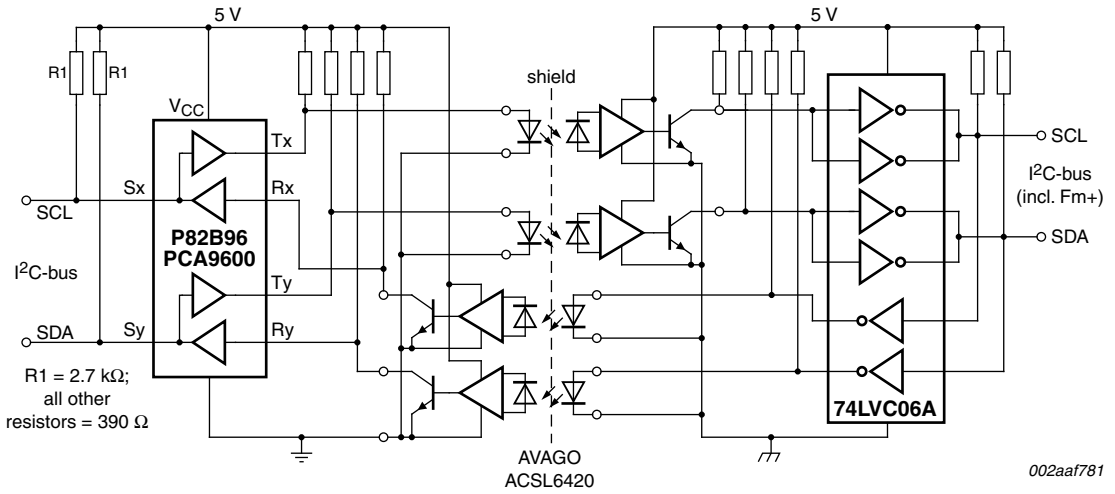


PCA9621 slave at the right. Top: waveforms at left; SCL dark blue; SDA cyan. Bottom: waveforms at right; SCL magenta; SDA green.

Remark: Nominal 5 V SMPS used was nearer to 4 V.

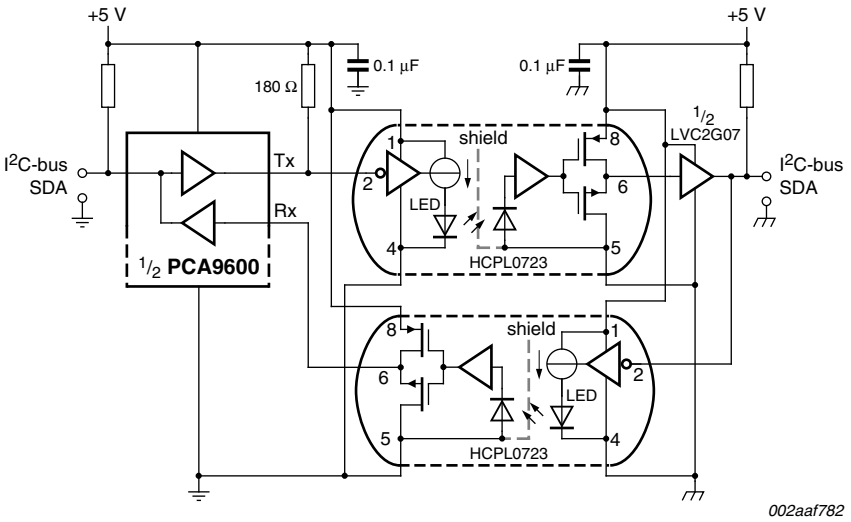
Fig 8. 1 MHz traces generated by arrangement as in Figure 7

An alternative LED drive method, suggested by Avago and applied in Figure 9, uses the Tx or gate output to short-circuit the LED when it is required to be off. The change in voltage across the LED is smaller, so operation may be faster but another advantage is that the supply current shows much smaller changes and that simplifies bypass requirements.



The 5 V supply current does not have large changes, it is reasonably constant because it is 'diverted' around the LEDs rather than being simply switched on/off. Used with PCA9600, this circuit will also typically operate to 1 MHz.

Fig 9. Avago's alternative LED drive arrangement for their quad coupler with 50 ns (typ) propagation delays



These Avago couplers have just 22 ns maximum propagation delay (16 ns typical).

This arrangement must be duplicated for the SCL bus signal, total 4 × HCPL0723 required.

Fig 10. Fastest arrangement; PCA9600 drives the highest speed opto-couplers

7. Multi-node opto-electrical isolation

The examples so far have considered only arrangements that connect a single isolated module to a normal bus. When more than one module must be isolated, or when a lower impedance or higher voltage distribution bus is required then care must be taken to run those distribution buses at normal logic signal levels. In particular the signal levels at the Sx/Sy pins must never be distributed because they have a relatively low noise margin and therefore lower tolerance to noise. That means the opto-coupler I/O side must always be connected to the distribution bus.

In all the figures above the I²C-bus connection on the right hand side of the schematic is a perfectly standard I²C-bus with full noise margins and so can be used as a distribution bus for connection of multiple opto-isolation modules.

In the higher speed examples Figure 7, Figure 9 and Figure 10, the right hand bus can be operated at the 20 mA or 30 mA Fm+ bus drive current levels that are generally suitable for driving quite long wiring or cables. Provided the additional delays are taken into account, all those Fm+ drive versions should easily drive 20 m cables. At lower speeds and on very long cables the use of higher bus voltages, e.g., 12 V to 15 V, can provide increased noise immunity.

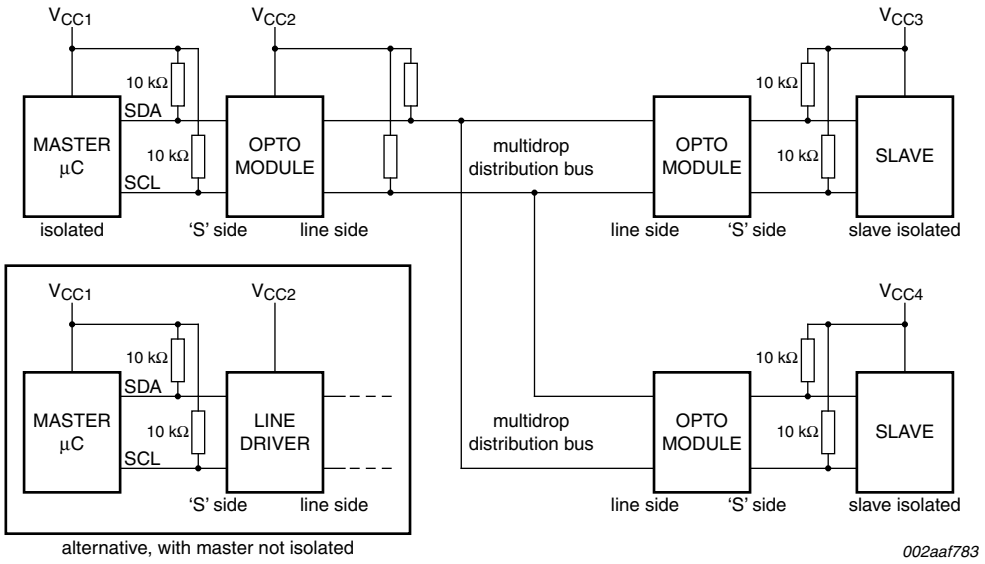


Fig 11. Suggested circuit for multipoint applications

Figure 11 shows a general arrangement for a multi-drop system in which isolated and non-isolated modules can be mixed as required. The coupler shown in the example in Figure 12 is the Darlington type HCPL-2731 with an 18 V rating and V_{OL} guarantees when sinking 24 mA. It can be used to directly drive lower impedance higher voltage distribution bus lines in exactly the same way that P82B96 is used. It can interface with other isolated modules or with a simple P82B96 line driver module as also shown in Figure 12 when isolation is not required. Both isolated and non-isolated modules can be used to connect the master(s) or any slaves to the distribution bus wiring. When many isolation modules are used in a system it is convenient to build the opto modules as shown in Figure 12 with a logic buffer (e.g. HEF4050B) driving the LED on the line side. That ensures each

module imposes no load on the distribution bus and saves making calculations about loading. When only a small number of modules is used then a buffer is not needed, but just remember to include the LED drive current when calculating the pull-up resistor(s) for the line side distribution bus to remain under 24 mA.

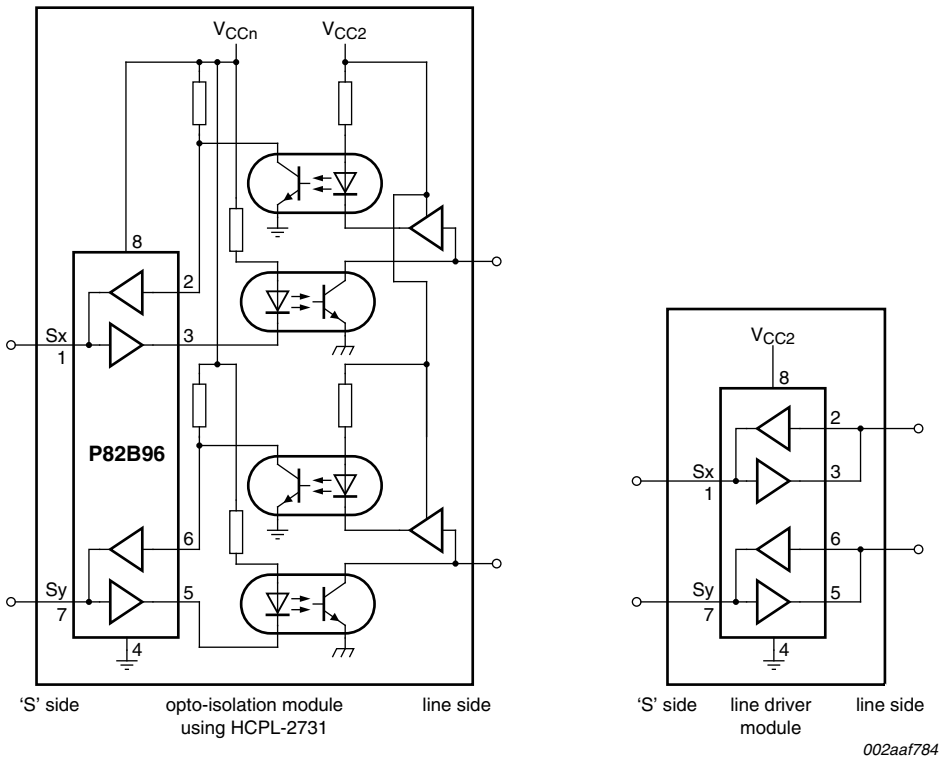
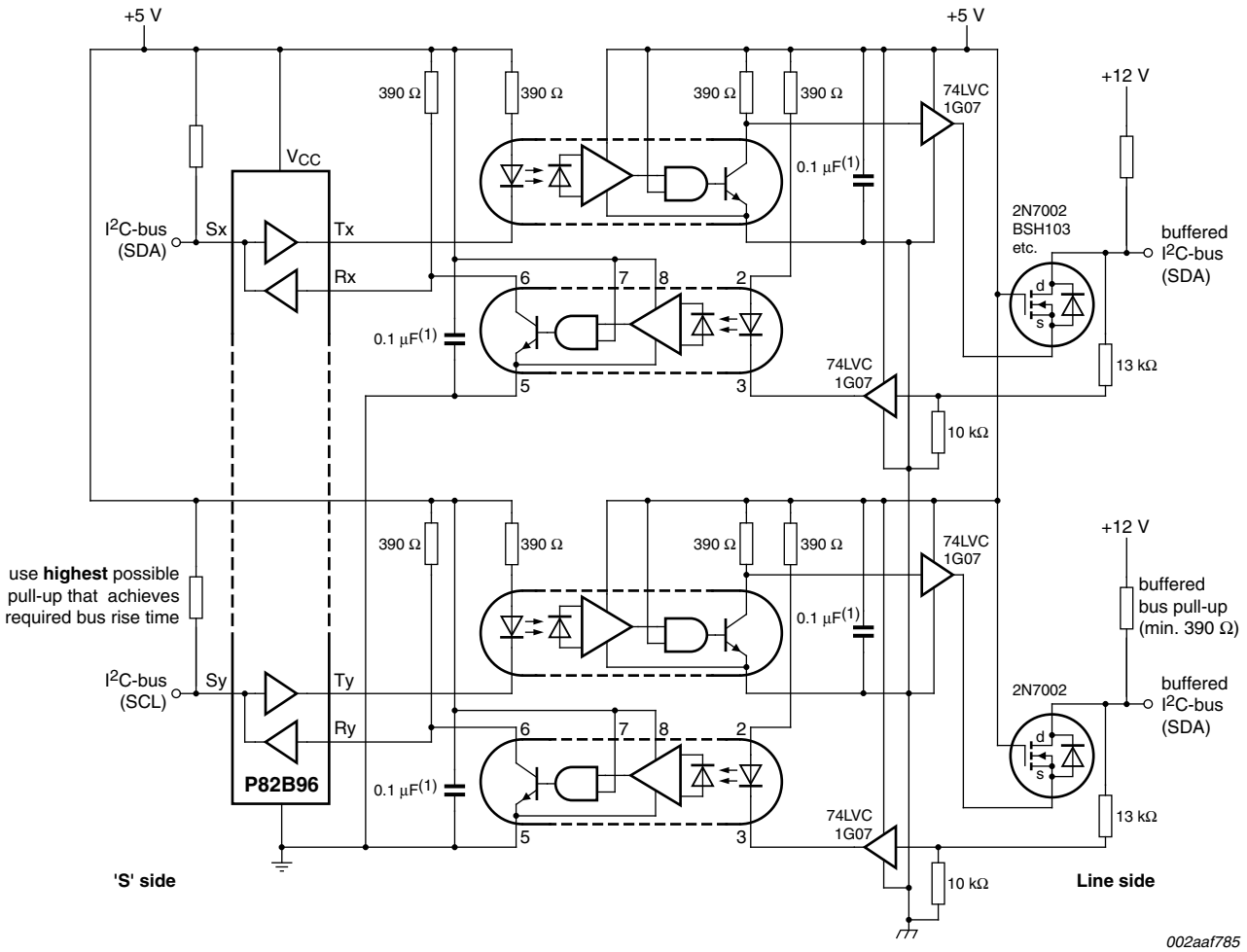


Fig 12. Suggested modules for use in the system of Figure 11

When using the HCPL-2731 the distribution bus pull-ups should be calculated for no more than the 24 mA guaranteed rating of that part. That still allows 510 Ω pull-ups to 12 V that will drive around 2 nF (or at least 20 meters) of wiring capacitance. For smaller bus capacitance it is not necessary to waste energy and larger resistance pull-ups can be used. The cheapest, simplest, opto interface as shown in Figure 12 is very slow and the warnings about a few kHz operation, as for Figure 4, should be taken seriously. It is wise to monitor the waveforms around the opto devices and check they are doing what the data sheet implies. Never connect the Sx sides of an opto module to a distribution bus because that interface has lower noise margins. The Sx interface is intended for connection only to standard I²C parts and not to other buffers. Adapting higher speed buses to higher voltages, while working with the lower voltage ratings of faster opto-couplers, will require some level shifting technique, for example an FET such as 2N7002 in common-gate configuration as the driver, and a resistive voltage divider on the receiver as shown in Figure 13. The resistive divider should be made high impedance, compared to the bus pull-up, to avoid any significant lowering of the bus 'HIGH' logic level. This divider technique obviously has limitations if very many modules are needed. Then an alternative is to replace the 74LVC1G07s by 3-state high voltage logic, e.g., HEF40244B, using the active LOW enable pins as the inputs.

Picogates are shown as the logic buffers in some schematics because they simplify layout. A hex device, 74LVC07A, would be lower cost but with gates effectively connected in series, care should then be taken with stray capacitance coupling between IC pins that could cause high frequency instability.



(1) 6N137 data suggests 0.1 µF mounted between pin 5 and pin 8.

Fig 13. Suggested 12 V / 100 kHz distribution bus module with isolation (30 mA driver)

8. Conclusion

Solutions have been presented, using P82B96 or PCA9600 to split the bidirectional I²C signals into uni-directional signals enabling them to be transmitted through various uni-directional logic signal devices including opto-isolators. The solutions range from simple but slow to the fastest Fm+ speed class and allow isolation of sections of an I²C-bus up to the limits of available couplers, at least several kV.

Details of the timing considerations for I²C buses and designing for the delays caused by buffers, cables, or opto-couplers can be found at the NXP web site www.nxp.com/i2c or at www.nxp.com/interface.

9. Abbreviations

Table 1. Abbreviations

Acronym	Description
CAN	Controller Area Network
FET	Field-Effect Transistor
I²C-bus	Inter-integrated Circuit bus
I/O	Input/Output
IC	Integrated Circuit
LED	Light-Emitting Diode
LVC	Low Voltage CMOS
PoE	Power over Ethernet
SMPS	Switched Mode Power Supply

10. References

[1] **AN10658, "Sending I²C-bus signals via long communication cables" —** www.nxp.com/documents/application_note/AN10658.pdf

[2] **AN460, "Using the P82B96 for bus interface" —** www.nxp.com/documents/application_note/AN460.pdf

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