

Initializing the TSEC Controller

by *Ahsan Kabir*
Digital Systems Division
Freescale Semiconductor, Inc.
Austin, TX

This application note describes how to initialize the MPC8560 TSEC controller. The software is written for the TSEC controller and it is tested on the MPC8560ADS board. The TSEC software, which is tested on the MPC8560ADS board, is available with this application note at the Freescale web site listed on the back cover of this document. The ID of the .zip file is AN2925SW.

To augment the comments embedded in the source code, this application note describes how the MAC loopback, PHY loopback, and external loopback work.

Contents

1. Introduction	2
2. Test Cases	3
3. Test Results	4
4. File Structure	4
5. Conclusion	4

1 Introduction

The TSEC controller has a wide variety of features. This application note focuses on important operational concepts in the test code.

1.1 Hardware Setup

The software is tested on MPC8560ADS RevA board, which has two Gigabit Ethernet PHY devices, one connected to TSEC1 and the other connected to TSEC2. These PHY devices are Alaska Ultra 88E1011S from Marvell.

Power-on reset configuration of these PHY devices depends on the J55 and J47 headers. J55 controls the configuration settings for TSEC1 and J47 controls the configuration settings for TSEC2. For instance, the PHY connected to TSEC1 has a different PHY address based on whether the configuration plug is placed on the J55 header. Without the configuration plug, the PHY address connected to TSEC1 is 0; with the configuration plug, it is 15. The software assumes that both J55 and J47 are without the configuration plugs.

To better understand how the power-on reset configuration values are determined for the PHY devices, refer to the schematic view of J55 and J47. Also, refer to Section 11.4 of the *MPC8560ADS User's Manual* and the PHY datasheet.

1.2 Software

Test code written to initialize the TSEC controller prepares 32 transmit and receive BDs. Enough embedded comments are provided in the source code for easy understanding of the code flow.

Following are the key features of the TSEC software:

- Individual address is used for the station (ADS). The MAC address for the station is 0x12345678ABCD. Note that assignAddresses() routine byte swaps this value and places the swapped value into two station address registers. The MAC address is swapped because it must be presented in Little-Endian format.
- Thirty-two BDs (transmit and receive) are defined in the BD rings. For transmit buffers, a static array of structure type TSEC_TXBUFFER is defined. As for the receive buffers, the code assumes that the start address of the receive buffer is 0xD00000. The prepareTxbufferBd() and prepareRxbufferBd() routines define the transmit BD ring, transmit buffer, receive BD ring, and receive buffer.
- When the user requests PHY Loopback, phyInit() routine initializes the Gigabit PHY connected to the TSEC. The software uses APIs to manage the read and write operations. In the PHY loopback mode, the control register (#0) is programmed to set the PHY in Gigabit mode and also to set the loopback mode.
- The test code provides polling and interrupts to check the status of frame transmission and reception. The default setting of this code has 32 BDs in the transmit and receive BD ring. Interrupt coalescing is enabled and, for every 16 frames transmitted, one interrupt is generated. For every 16 frames received, one interrupt is generated. The interrupt handler for transmit-tsec!TransmitIsr() increments a global variable upon exiting. This counter value

becomes 2 after the run. The receive path functions in much the same way. The interrupt service routines can be found in the `epic_handler.c` file. For interrupts, the PIC controller is also initialized.

2 Test Cases

The TSEC project is compiled and debugged using Codewarrior 8.6. Use the supplied `tsec.mcp` project and load this project in the CodeWarrior environment. For the `printf` statements to work, make sure that the CCB frequency of the MPC8560ADS board is set to 266MHz. Different clocks can be set up using the dip switch settings of the board, as described in the board user's manual for the MPC8560ADS RevA system.

For all test cases discussed, the common operation is to compare the received data with the trashiness data. The test passes when received data is same as transmitted data. Test cases are defined through the MACRO values in `tsec.h` file. For all test cases, the following MACRO should be undefined. These two MACROs are present and indicate work in progress, but they cannot be used for the current version of the software.

```
///define NORMAL_MODE /* transmitting to wires and receiving from wires */
```

Also, for each test case, the user can use the polling scheme or interrupt scheme to get the status of frame transmission and reception by uncommenting either of the following:

```
///define STATUS_POLLING  
#define STATUS_INTERRUPT
```

2.1 MAC Loopback

In MAC loopback mode, the loopback is performed within the TSEC MAC itself. The TSEC transmitter sends out data that is then looped back to the TSEC receiver. The PHY is not involved. Uncomment `MAC_INTERNAL_LOOPBACK` and comment out `PHY_LOOPBACK` in the `tsec.h` file.

Also, choose the interface for this loopback mode. Define `INTERFACE_MODE` as `GMII_INTERFACE`, `MII_INTERFACE`, or `TBI_INTERFACE`.

2.2 PHY Loopback

In PHY loopback mode, the TSEC MAC transmits data that is looped back by the PHY device to the receiver of the TSEC MAC. Uncomment `PHY_LOOPBACK` and comment out `MAC_INTERNAL_LOOPBACK` in the `tsec.h` file.

The interface for PHY loopback is always `GMII_INTERFACE`.

3 Test Results

The software sends 32 Ethernet frames and receives 32 frames. In the polling scheme, the `checkResults()` routine returns a value of `0xFFFFFFFF` when the receive frames match the transmitted frames. The transmitted frames are static arrays and these buffers can be checked using `debugger-transmitBuffer[]`. For the receive buffer, memory display starts at memory location `0xD00000`.

If the interrupt scheme is chosen, global variables `txbdCounter` and `rxbdCounter` should both be 2. These global variables are incremented from `tsec1TransmitIsr()` and `tsec1ReceiveIsr()`, respectively.

4 File Structure

- `main.c`: invokes a routine to initialize PIC and TSEC.
- `tsec.c`: initializes the TSEC controller.
- `mgmt.c`: contains APIs to manage initialization, reads, and writes.
- `marvell_phy.c`: contains minimal code for initializing the PHY.
- `epic.c`: contains initialization code for the PIC and other utility routines related to PIC.
- `epic_handler.c`: contains TSEC handlers.
- `tsec.h`: contains all MACROs for defining various test cases.
- `epic.h`: contains MACROs related to the PIC.

5 Conclusion

The TSEC software tests TSEC loopback mode for the MAC and PHY. In the future, it may connect the TSEC to the external tester.

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:

www.freescale.com

email:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
(800) 441-2447
303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The described product contains a PowerPC processor core. The PowerPC name is a trademark of IBM Corp. and used under license. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2004, 2005.

Document Number: AN2925
Rev. 0
11/2005