



LPC860: 32-Bit Arm® Cortex®-M0+-Based Low-Cost MCU with I3C Interface

LPC86X

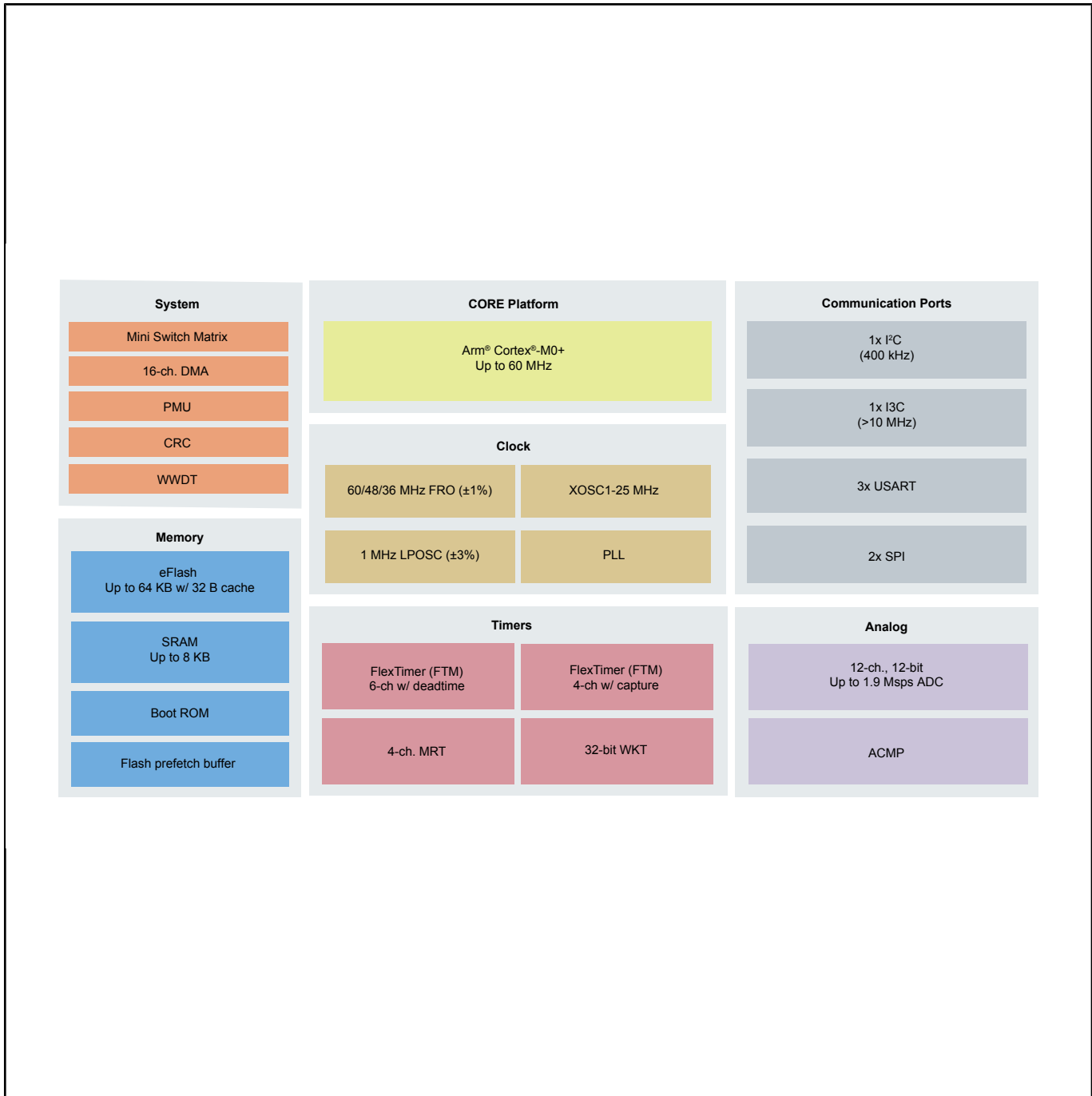
Last Updated: Apr 11, 2024

The LPC860 32-bit Arm Cortex-M0+ based cost effective MCUs are designed for Industrial and IoT applications. LPC860 operates at a frequency of up to 60 MHz and supports up to 64KB of flash memory and up to 8 KB SRAM. This family features a power-optimized core, small footprint in popular packages and level shifting options thanks to its separate power rails.

The peripheral complement of the LPC860 includes a CRC engine, I2C-bus interface, I3C-bus interface, up to three USARTs, two SPI interface, one multi-rate timer, self-wake-up timer, two FlexTimer with hardware dead-time insertion and quadrature decoding, one 12-bit ADC, one analog comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine and up to 54 general-purpose I/O pins.

The LPC860 family are supported by the [MCUXpresso ecosystem](#), which includes an SDK, a choice of IDEs, and secure provisioning and configuration tools to enable rapid development.

LPC86x MCUs Block Diagram



View additional information for [LPC860: 32-Bit Arm® Cortex®-M0+-Based Low-Cost MCU with I3C Interface.](#)

Note: The information on this document is subject to change without notice.

www.nxp.com

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. © 2024 NXP B.V.